EDOC137

EUROGAM PROJECT

EUROGAM DATA ACQUISITION SYSTEM

BGO Prototype Card
Register Layout Specification

Edition 2.0
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Here is the list of Controlable Parameters

1 Parameter Common to whole module

- Veto width: 8 bit DAC (1 per module) [w]
- Dead time discriminators width: 8 bit DAC (1 per module) [w]
- Sum I multiplicity width: 8 bit DAC (1 per module) [w]
- Fast trigger width (w1): 8 bit DAc (1 per module) [w]
- Validation (Sample Point) (w2): 8 bit DAC (1 per shield) [w]
- Start Readout width (w3): hard-fixed to 3 volts (i.e. 10 us) [r]
- PDS gate width: 8 bit Dac (1 per module) [w]
- Analogue Multiplexer control word: 16 bit (1 per module) [r/w]
- Digital Multiplexer control word: 16 bit (1 per module) [r/w]
- Voltage Inspection line Control: (1 per module) [r/w]
- CDF (Contrôle des Fenêtres) (1 per module) [r/w]
- Module Configuration Register (1 per module) [r/w]
- Test access to readout FIFO (write) (1 per module) [w]
- Test access to readout FIFO (read) (1 per module) [r]

2 Parameter for each of the 6 shields

- Discriminator threshold: 12 bit DAC (1 per shield) [w]
- Test generator: 12 bit DAC (1 per shield) [w]
- Channel Control Register(CCR): 11 bit register (1 per shiled) [r/w]
- ROCI ADC low threshold (3 per shield) [r/w]

- ROCI ADC Address (3 per shield) [r/w]
- ROCI ADC test read of ADC address and data (3 per shield) [r/w]
- ROCI Sliding scale enable register (1 per shield) [r/w]
- ROCI parameter readout enable/disable (1 per shield) [r/w]
- ROCI Sliding scale register (1 per shield) [r/w]
- ROCI test register (1 per shield) [w]

3 Address space Allocation

- 000-0FE Module parameters
- 100-1FE shield 1 parameters
- 200-2FE shield 2 parameters
- 300-3FE shield 3 parameters
- 400-4FE shield 4 parameters
- 500-5FE shield 5 parameters
- 600-6FE shield 6 parameters

4 Register layout

```
Name: Veto width  DAC                   Offset: @0000     write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00

+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  | msb                       lsb|
|   |   |   |   |   |   |   |   |  |  8 bit DAC for veto width    |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 100  ns
1111 = 1000 ns   1 bit = 4 ns


Name: Dead time discriminator width DAC    Offset: @0002   write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  | msb                      lsb|
|   |   |   |   |   |   |   |   |  | 8 bit DAC for dead time width |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 2  us
1111 = 20 us   1 bit = 80 ns
```

```
Name: Sum I multiplicity width DAC       Offset: @0004     write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  msb                       lsb|
|   |   |   |   |   |   |   |   |8 bit DAC for sum I mult. width|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 100 ns
1111 = 1000 ns   1 bit = 4 ns

Name: Fast trigger width DAC              Offset: @0006     write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  msb                        lsb|
|   |   |   |   |   |   |   |   |8 bit DAC for fast trigg. width|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 us
1111 = 2 us   1 bit = 8 ns

Name: Validation Sample Point             Offset: @0008     write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  msb                       lsb|
|   |   |   |   |   |   |   |   |8 bit DAC: Valid. sample point |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 us
1111 = 10 us   1 bit = 40 ns

Name: PDS gate width  DAC                 Offset: @000C    write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  msb                        lsb|
|   |   |   |   |   |   |   |   | 8 bit DAC for PDS gate width  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 us
1111 = 10 us   1 bit = 40 ns
```

```
Name: Analogue multiplexor Control      Offset: @0030    read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| Select Parameter  | Sel shield| Select Parameter  | Sel shield|
|    for Line 2     | for Line 2|     for Line 1    | for line 1|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: Digital multiplexor Control   Offset: @0032    read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| Select Parameter  | Sel shield| Select Parameter  | Sel shield|
|    for Line 2     | for Line 2|    for Line 1     | for line 1|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

Sel shield: (for Analogue and Digital Multiplexer)

000 = disconnected from inspection line	100 = channel 4 connected
001 = channel 1 connected	101 = channel 5 connected
010 = channel 2 connected	110 = channel 6 connected
011 = channel 3 connected	111 = not used ?

Select Parameter: (for Analogue and Digital Multiplexer)

Analogique	Logique	Select Parameter
Line Receiver BGO a	Discriminator Output BGO a	00
Line Receiver BGO b	Discriminator Output BGO b	01
Line Receiver BGO c	Discriminator Output BGO c	02
Line Receiver BGO d	Discriminator Output BGO d	03
Line Receiver BGO e	Discriminator Output BGO e	04
Line Receiver BGO f	Discriminator Output BGO f	05
Line Receiver BGO g	Discriminator Output BGO g	06
Line Receiver BGO h	Discriminator Output BGO h	07
Line Receiver BGO i	Discriminator Output BGO i	08
Line Receiver BGO j	Discriminator Output BGO j	09
TAC output	Start TAC	10
Shaping filter output	Fast Tigger in	11
Peak detector output	PDS GATE	12
Test generator output	Fast Trigger Sample Point	13
BGO j input	Validation Sample point	14
BGO i input	Local Trigger gate 3	15
BGO h input	Dead time discriminator Gate	16
BGO g input	OR (discriminator output)	17
BGO f input	Discriminator veto	18
BGO e input	Validation Ack	19
BGO d input	Encode commande	20
BGO c input	Validation in	21
BGO b input	INHIBIT	22
BGO a input	Reset Local trigger	23

```
Name: Voltage Inspection Line Control   Offset: @0034    read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |not|Selct Parameter| select Mux|
|   |   |   |   |   |   |   |   |usd|  (4 bits)     | (3 bits)  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Select Mux = 1 or 2

---------+-------+---------------------------------------------
Select   |Select |
Parameter|Mux    |                   Parameter
(4 bits) |(3bits)|
---------+-------+---------------------------------------------
  0      | 1     | DAC output: Fast Trigger Width
  1      | 1     | DAC output: SUM I Multiplicity
  2      | 1     | DAC output: Dead Time Discriminator Width
  3      | 1     | DAC output: Veto Width
---------+-------+---------------------------------------------
  4      | 1     | DAC output: Test Generator Shield 6
  5      | 1     | DAC output: Test Generator Shield 5
  6      | 1     | DAC output: Test Generator Shield 4
  7      | 1     | DAC output: Test Generator Shield 3
  8      | 1     | DAC output: Test Generator Shield 2
  9      | 1     | DAC output: Test Generator Shield 1
---------+-------+---------------------------------------------
  10     | 1     | DAC output: Discriminator threshold Shield 6
  11     | 1     | DAC output: Discriminator threshold Shield 5
  12     | 1     | DAC output: Discriminator threshold Shield 4
  13     | 1     | DAC output: Discriminator threshold Shield 3
  14     | 1     | DAC output: Discriminator threshold Shield 2
  15     | 1     | DAC output: Discriminator threshold Shield 1
---------+-------+----------------------------------------------
  16, 17 |       |                unused
---------+-------+----------------------------------------------
```

Select Parameter (4 bits)	Select Mux (3bits)	Parameter
18	2	Voltage measurement (Alim) +24 volts (not yet implemented)
19	2	Voltage measurement (Alim) -24 volts
20	2	Voltage measurement (Alim) -12 volts
21	2	Voltage measurement (Alim) -6 volts
22	2	Voltage measurement (Alim) -5.2 volts
23	2	Voltage measurement (Alim) -2 volts
24	2	Voltage measurement (Alim) +3 volts Reg
25	2	Voltage measurement (Alim) +5 volts ADC
26	2	Voltage measurement (Alim) +5 volts
27	2	Voltage measurement (Alim) +6 volts
28	2	Voltage measurement (Alim) +12 volts
29	2	DAC output: PDS Gate Width
30	2	DAC output: Start Readout Width (unused)
31	2	DAC output: Validation Sample Point

Note about parameter 18 to 28: After measurement, each voltage must be multiplied bye 10 because all the voltages are divided by 10 before they are measured. The voltages are divided by 10 because one can't drawn more than 12 vots through the multiplexer lines.

Note: For the definitive version of the BGO card, only the voltage +24 and -24 will be divided per 2 before the voltage measurement. The other voltages will not be divided.

```
Name: Controle des fenetres          Offset: @0036   read/write
      (will be implemented later)

  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |on/|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |off|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
(1=on, 0=off)
```

```
Name: Module Configuration       Offset: @0038   read/write
      Register

  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |End|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |mod|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
End mod = 1 (if last module)
End mod = 0 (if not last module)
```

```
Name: Test Write to readout FIFO      Offset: @003C     write only

31              23              15                07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|   |   |   |   |   |   |   |   |
|q q|A A A A A A A A A A A A A A|   |   |   |   |   |   |   |   |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

Writes will put data into the FIFO directly. That is, for write operation only D16 to D31 are needed.

```
Name: Test Read to readout FIFO      Offset: @003C    read only

31              23              15                07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|   |   |   |   |   |   |   |   |
|q q|A A A A A A A A A A A A A A|   |   |   |   |   |   |   |   |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
Read byte: D16-D31
```

```
Name: Discriminator threshold DAC      Offset: @0100 (shield 1) write only
                                               @0200 (shield 2)
                                               @0300 (shield 3)
                                               @0400 (shield 4)
                                               @0500 (shield 5)
                                               @0600 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   | msb                                       lsb|
|   |   |   |   | 12 bit DAC for Discriminator threshold       |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 volts
1111 = 5 volts    1 bit = 3 mv
```

Note: There is a divider (by 10) after the DAC. So, the value to be written in the DAC must be multiplied by 10 before writing it. Here is the effective range (after the division):

```
0000 = 0 volts
1111 = 0.5 volts    1 bit = 0.3 mv
```

exemple: to get 100 mv as the threshold one will write 1000 mv (1 volt) in the DAC.
But for the "Mesure de tension" operation the measurement is done before the value is divided: the measured value is the value written in the DAC.

```
Name: Test generator DAC              Offset: @0102 (shield 1) write only
                                              @0202 (shield 2)
                                              @0302 (shield 3)
                                              @0402 (shield 4)
                                              @0502 (shield 5)
                                              @0602 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   | msb                                       lsb|
|   |   |   |   | 12 bit DAC for Test Generator                |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 volts
1111 = 5 volts    1 bit = 3 mv
```

```
Name: Channel Control Register       Offset: @0120 (shield 1) read/write
            (CCR)                            @0220 (shield 2)
                                             @0320 (shield 3)
                                             @0420 (shield 4)
                                             @0520 (shield 5)
                                             @0620 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |ON/|ON/|ON/|ON/|ON/|ON/|ON/|ON/|ON/|ON/|ON/|
|   |   |   |   |   |OFF|OFF|OFF|OFF|OFF|OFF|OFF|OFF|OFF|OFF|OFF|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Shield Disable/Enable                      (bit 10) 1=disabled,   0=enabled

important: bit 0 to 10 allocation

1) Test mode: using Test Generator.

BG0a Disable/Enable                        (bit  0) 0=enabled,    1=disabled
BG0b Disable/Enable                        (bit  1) 0=enabled,    1=disabled
BG0c Disable/Enable                        (bit  2) 0=enabled,    1=disabled
BG0d Disable/Enable                        (bit  3) 0=enabled,    1=disabled
BG0e Disable/Enable                        (bit  4) 0=enabled,    1=disabled
BG0f Disable/Enable                        (bit  5) 0=enabled,    1=disabled
BG0g Disable/Enable                        (bit  6) 0=enabled,    1=disabled
BG0h Disable/Enable                        (bit  7) 0=enabled,    1=disabled
BG0i Disable/Enable                        (bit  8) 0=enabled,    1=disabled
BG0j Disable/Enable                        (bit  9) 0=enabled,    1=disabled

2) Normal mode: in normal mode, both bit 0 to bit 9 are set to 1 (i.e all channel
                disabled)

Name: ROCI ADC low threshold     Offset: @0140 (shield 1)  read/write
      (Pattern)                          @0240 (shield 2)
                                         @0340 (shield 3)
                                         @0440 (shield 4)
                                         @0540 (shield 5)
                                         @0640 (shield 6)
31              23             15              07             00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| Pattern ADC Lower Threshold   |                               |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC low trheshold          Offset: @0144 (shield 1)  read/write
      (TAC ADC)                               @0244 (shield 2)
                                              @0344 (shield 3)
                                              @0444 (shield 4)
                                              @0544 (shield 5)
                                              @0644 (shield 6)
31               23              15               07              00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| TAC ADC Lower Threshold       |                               |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC  low threshold    Offset: @0148 (shield 1)  read/write
      (Energy Shield)                    @0248 (shield 2)
                                         @0348 (shield 3)
                                         @0484 (shield 4)
                                         @0548 (shield 5)
                                         @0648 (shield 6)

31               23              15               07              00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| Energy Shield lower threshold |                               |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC Address      Offset: @0150 (shield 1)  write only
      (Pattern)                     @0250 (shield 2)
                                    @0350 (shield 3)
                                    @0450 (shield 4)
                                    @0550 (shield 5)
                                    @0650 (shield 6)

31 30          23                   15 .......................00
+-+-+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| | |ROCI Patrn ADC Address (14bits)|                           |
|q|q|-------------+-----------------|                           |
| | |Item(6bits)| Group(8bits)      |                           |
+-+-+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC Address       Offset: @0154 (shield 1)  write only
      (TAC ADC)                      @0254 (shield 2)
                                     @0354 (shield 3)
                                     @0454 (shield 4)
                                     @0554 (shield 5)
                                     @0654 (shield 6)

31 30          23                  15 .......................00
+-+-+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| | |ROCI TAC ADC Address (14 bits) |                           |
|q|q|---------+---------------------|                           |
| | |Item(6bits)| Group(8bits)      |                           |
+-+-+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC Address           Offset: @0158 (shield 1)  write only
      (Energy ADC)                       @0258 (shield 2)
                                         @0358 (shield 3)
                                         @0458 (shield 4)
                                         @0558 (shield 5)
                                         @0658 (shield 6)

31 30          23                  15 .......................00
+-+-+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| | |  Energy ADC Address (14 bits) |                           |
|q|q|---------+---------------------|                           |
| | |Item(6bits)| Group(8bits)      |                           |
+-+-+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI Test Read         Offset: @0160 (shield 1)  read only
       Pattern                       @0260 (shield 2)
                                     @0360 (shield 3)
                                     @0460 (shield 4)
                                     @0560 (shield 5)
                                     @0660 (shield 6)

31                             15    12                 03   00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls| 3    |   Pattern  data   |  3  |
|q q|A A A A A A A A A A A A A A|bits |D D D D D D D D D D|bits |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

10 Pattern bits: D03-D12
bits D13 to D15 and D01 to D02 not used

```
Name: ROCI Test Read         Offset: @0164 (shield 1)  read only
     (TAC ADC)                       @0264 (shield 2)
                                     @0364 (shield 3)
                                     @0464 (shield 4)
                                     @0564 (shield 5)
                                     @0664 (shield 6)

31             23             15               07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|ms  TAC  ADC  data word      ls|
|q q|A A A A A A A A A A A A A A|0 0 0 D D D D D D D D D D D D D|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Name: ROCI Test Read         Offset: @0168 (shield 1)  read only
      (ENERGY ADC)                   @0268 (shield 2)
                                     @0368 (shield 3)
                                     @0468 (shield 4)
                                     @0568 (shield 5)
                                     @0668 (shield 6)

31             23             15               07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|ms   Energy ADC data word    ls|
|q q|A A A A A A A A A A A A A A|0 0 0 D D D D D D D D D D D D D|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Name: ROCI Sliding scale     Offset: @0170 (shield 1)  read/write
      Enable Register                @0270 (shield 2)
                                     @0370 (shield 3)
                                     @0470 (shield 4)
                                     @0570 (shield 5)
                                     @0670 (shield 6)

31                                              19  18  17  16  15 ..... 00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+----------+
|   |   |   |   |   |   |   |   |   |   |   |   |   |ENE|TAC|PAT|          |
|   |   |   |   |   |   |   |   |   |   |   |   |   |RGY|   |TER|          |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+----------+
bit 16 (Pattern readout enable) must be set to 0.
```

```
Name: ROCI Parameter Readout    Offset: @0174 (shield 1)  read/write
      Enable Register                   @0274 (shield 2)
                                        @0374 (shield 3)
                                        @0474 (shield 4)
                                        @0574 (shield 5)
                                        @0674 (shield 6)
31                                               19  18  17  16  15 ..... 00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+----------+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |ENE|TAC|PAT|          |
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |RGY|   |TER|          |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+----------+


Name: ROCI Sliding scale     Offset: @0178 (shield 1)  read only
      Register                       @0278 (shield 2)
                                     @0378 (shield 3)
                                     @0478 (shield 4)
                                     @0578 (shield 5)
                                     @0678 (shield 6)

31                             15                             00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb       (16 bits)       lsb|                               |
|Sliding Scale register for ROCI|                              |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Name: ROCI test              Offset: @017C (shield 1)  write only
      Register                       @027C (shield 2)
                                     @037C (shield 3)
                                     @047C (shield 4)
                                     @057C (shield 5)
                                     @067C (shield 6)

31                             15                             00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb       (16 bits)       lsb|                               |
|        ROCI Test register    |                               |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```