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EUROGAM PROJECT

NSF DATA ACQUISITION SYSTEM

Ge prototype card Specification

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IPN Orsay and NSF Electronics Groups
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Ge Prototype Card Specification (Combined French and UK version)

Ian Lazarus and Alphonse Richard

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1 Introduction

This document describes the final specification in terms of features and system interfaces for the Eurogam Ge card. The specification relates to the phase one 'Common Deadtime' card with some suggestions as to what the phase 2 card will contain (Parallel operation, support for new detector geometries, ...).

Note for physicists, programmers and designers of other cards:
The Ge card design is now frozen; it is too late for comments or changes and this document describes what is now being built.

The document contains some explicit performance specifications; where performance is not stated explicitly it should be assumed that the ADC specs for accuracy and linearity determine the requirements for preceding components.

2 Overview of Ge card

The Ge card will be made up of six channels, each comprising several functional blocks implemented in SMT (CMS) or hybrids.

Each of the six channels will contain:

- Analogue Pulse Processing
  - Receiver and buffer
  - Shaping Amplifier (Unipolar)
  - Bipolar Amplifier
  - Ballistic deficit correction.
  - Timing Crossover detection (TCO)
  - Peak Detect and Hold
  - Timing Filter Amplifier (TFA)
  - Constant Fraction Discriminator (CFD)
  - Time to Amplitude Converter (TAC)
- Digitization
  - ADC

  - Sliding scale correction and serial to parallel conversion

- Readout
  - Channel Readout
  - Card Readout

- Local Trigger

- Diagnostics and Testing Facilities

In brief, the Eurogam Ge card works as follows. It accepts analogue inputs from Ge preamplifiers and produces 4 digitized outputs per input. The first three outputs are the main data: two energy outputs with low (20 MeV) and high (4 MeV) gain and one timing output which is derived from the timing of the Ge input relative to a common signal. In addition there is one output which times from CFD to a crossover detector for possible pileup recovery or maybe additional software charge deficit correction.

The internal pulse shaping is quasi-triangular with fixed gain and fixed time constant. In the future (but not during the Daresbury phase) it will be possible to change time constants, and perhaps gain too, by swapping hybrids. It is possible to replace the shaping amplifier with an external amplifier, for example a gated integrator.

Hardware ballistic deficit correction is provided on both 4 MeV and 20 MeV energy signals using the Hinshaw method.

The energy and timing outputs are only produced if a user defined global trigger condition is satisfied. In order to generate this trigger the Ge card sends information to and receives trigger signals from the system's master trigger unit. The digitized data are transferred to the crate readout controller after each event.

3 Analogue Pulse Processing

This is the section of the card which deals with the preamplifier input signal. It is the most noise sensitive in the card because of the low signal levels (typical preamplifier signal is around 200 mV for a 1 MeV gamma ray). DC level of the pre-amplifier signal is also important and will be a problem if it is over 50mV[1]. The receiver circuit buffers the preamplifier input to the shaping amplifiers and the TFA for energy and timing respectively. The shaping amplifiers are followed by the peak detect and hold circuit which holds the analogue input for the ballistic deficit correction and the digitizing sections of the card. The TFA is followed by the CFD and the TAC from which timing information is available.

3.1 Receiver and buffer

The receiver circuit will be implemented in part of a hybrid. It will accept a negative single ended signal. The input impedance is 1KΩ. Output level is 4V at 20 MeV. This is the best tradeoff between S/N ratio and pileup saturation.

[1] The initial hybrid designs are undergoing modification to reduce the effects of DC offset (Nov 1990)

3.2 Shaping Amplifier

The processing previously performed in a NIM shaping amplifier takes place in this section of the card. There are four stages of processing: firstly a differentiator with gain and PZ adjustment, secondly a quasi-triangular filter (or a semi-gaussian filter), thirdly a base line restore circuit and finally an output stage Each of these four stages will be implemented in a separate hybrid. Physicists have requested an 800 keV range. It is not clear that VXI noise levels are low enough to implement such a high gain amplifier with a very low input signal level. Initially it is proposed that the 800 keV range is provided externally (see section 3.3). When we have experience of implementing the 20 MeV and 4 MeV amplifiers in VXI we will be in a position to judge the feasibility of implementing the 800 keV range on the Ge card itself.

3.2.1 Gain Stage

The input stage will be implemented in the rest of the receiver and buffer hybrid. It will differentiate the signal ready for filtering and provide pole zero compensation. The gain will be fixed and will give a 10V output for a 20 MeV gamma ray. The gain stage will saturate at 15V (i.e. 25 MeV).

The pole zero adjustment will rely on the accuracy of the preamplifier decay time constant being under $\pm 8\%$, preferably under $\pm 5\%$, so that only a fine adjustment is needed (nominal value is $50\mu s$ time constant). Adjustment will be by a FET used as a variable resistor controlled by a DAC from software. Non-linearity will not be a problem due to the low voltage drop across the FET (few tens of mV).

3.2.2 Filter

This hybrid circuit will shape the analogue pulse using a fixed shaping time and a 6th order quasi-triangular shaping function. (FWHM $3.1\mu s$, i.e. τ approx $1.2\mu s$) The selection of quasi-triangular instead of semi-gaussian shaping is made by resistors outside the hybrid. The gain will be fixed at 1. The only way to change the time constant will be to change the module. The output level will be 10V for 20 MeV. There will also be a clipped output which can be switched to the monitoring line for PZ adjustment.

3.2.3 Output stage

The output stage takes the output from the filter and applies a baseline restoration correction. The uncorrected filter output is also used to derive bipolar 20 MeV and 4 MeV ouputs. The BLR corrected 20 MeV unipolar signal is fed out to an external relay which selects either this signal or the output of the external amplifier to become the low gain (20 MeV) unipolar output signal. 20 MeV unipolar output from the relay is also fed back into the output hybrid to a further gain stage which produces the 4 MeV unipolar output.

The 20 MeV unipolar output is a 0 to 10V signal which must be attenuated to 8V for the peak detection circuit and then to 3V for the ADC. The 4 MeV signal is a 0 to 8V signal which feeds the peak detection circuit without attenuation.

The final gain stage used to generate the 4 MeV output is a fast recovery amplifier (since it will be saturated by high energy gamma rays) and will have sufficiently high bandwidth to be used with gated integrators as external amplifiers.

3.2.4 Baseline restore

The BLR circuit is necessary to remove baseline shifts caused by counting rate or by low frequency noise. The BLR will be implemented in a hybrid which will work by using an automatic counting rate adjustment with a fixed threshold set at around 10 keV. The BLR circuit senses the output of the high gain stage to achieve the greatest accuracy. The compensation is applied to the 20 MeV output stage which of course feeds the high gain stage. The BLR correction will be disabled by the software command which switches to the external amplifier although the threshold detection will still be used for pileup detection. This will be achieved by disabling the comparator in the BLR sense circuit.

3.3 External Amplifier (Gated Integrator)

As an interim solution, until a miniature Gated Integrator is designed for Eurogam, it will be possible to bypass the shaping amplifier stages by cabling through[2] an external NIM module such as the Ortec 973 gated integrator. This will also allow the coverage of the 800 keV range externally should it prove difficult to achieve in VXI. The external input will be connected instead of the 20 MeV output stage, switched by a changeover relay contact under software control. The external input will be buffered by a unity gain buffer stage with a 1K input impedance accepting the normal 0 to +10V NIM amplifier output levels.

The external amplifier will feed both the 20 MeV PDS and 4 MeV gain stage so that if it is set to 20 MeV full scale then we get 20 MeV and 4 MeV outputs; if it is set to 4 MeV full scale then we get 4 MeV and 800 keV outputs.

Controllable parameters are determined by the functionality of the external amplifier or gated integrator.

3.4 Peak Detect and Hold

Both energy ranges will have their own peak detection circuit. This is a hybrid which tracks the pulse shaping output and holds the peak value for use by the ADC. It starts looking for a peak in the shaped signal when the CFD fires and stops just before the channel control logic indicates that the ADC should begin conversion.

The maximum input level will be around 8V for optimum S/N ratio. The output will pass through an attenuator to limit the maximum signal to 3V which is the limit of the ADC range.

3.5 Ballistic Deficit Correction

This small SMT PCB will correct the unipolar outputs by adding a voltage proportional to the difference between the bipolar and unipolar outputs of the shaping amplifier to compensate for ballistic deficit. This is the Hinshaw method[3]. The compensation is not adjustable because it relies on properties of the shaping amplifier and so will not vary with detector or pre-amp. The user can, however, choose to disable the BDC circuit and to collect uncorrected data. This is controlled by software.

[2] This requires that the preamplifier has two outputs; one for the GI and the other for the VXI Ge card's receiver stage which must still provide triggering and timing information.

[3] Hinshaw and Landis, IEEE-NS37 p374
Goulding, Landis and Hinshaw IEEE-NS37 p417

(There are adjustments for zero level and for fine gain which are controlled by variable resistors set during commissioning of the board.)

3.6 Timing Filter Amplifier (TFA)

The TFA will be made in a hybrid. 10ns integration and 100ns differentiation are used. To change time constants it will be necessary to change the entire module. PZ cancellation will not be adjustable and will be preset for the nominal 50μs time constant used in the preamplifiers.

The physicists request for a 1000:1 dynamic range in the CFD cannot be implemented, but the TFA will be built with a selectable gain, changeable by a fixed factor of 5, so that the CFD dynamic range requirement is reduced to 200:1 and can be met.

This is *not* a variable gain, but a factor of 5 which would be switched on or off from software.

The output will be a maximum of 5 v into 100Ω.

3.7 Constant Fraction Discriminator (CFD)

The CFD will be implemented in surface mount technology. The design will not include slow rise time rejection and so will behave like a leading edge discriminator at low energy[4]. The dynamic range requested by physicists of 1000:1 is not achievable; a realistic figure is between 200:1 and 300:1. The internal delay line will be of 50ns.

There will be several programmable parameters associated with the CFD:

- Threshold (8 bit DAC = 256 steps of 5 keV giving a range 0 to 1.25 MeV for high gain TFA setting and 0 to 5 MeV in 20 keV steps for low TFA gain.)
- Pulse Width (8 bit DAC = 256 steps over range 10 to 265ns in 1ns steps, common to all channels on a card.)[5]
- Additional output delay for time alignment of pulses. (8 bit DAC. 0 to 255 ns in 1 ns steps.) This is in addition to the CFD internal delay.

The CFD output will be available via the front panel as a differential ECL logic signal for rate monitoring or other operations required by users. The CFD output pulse will also switch a current source (1 mA/channel) onto the VXI analogue sumbuses for fast Ge multiplicity calculation (both raw and clean multiplicity).

3.8 Timing Crossover Detector

This is part of a small SMT (CMS) PCB which also contains some buffers, and monostables for LEDs and for pre-pulse pileup. The timing crossover circuit monitors the 20 MeV bipolar output by a comparator with hysteresis to detect the zero crossing having been armed by the rising edge of the pulse crossing a threshold of 5mV. The output from the detector stops the crossover timing TAC.

[4] A more complex design will be implemented later to improve low energy behaviour.

[5] The CFD pulse width defines the Ge coincidence window.

3.9 Time to Amplitude Converter (TAC)

The TAC will be implemented in a Thomson ceramic resistor/transistor array. The range is 0 to 2μs with a resolution of better than 1 ns. (Crossover timing TAC uses a different timing capacitor to run over a range of 200ns from a delayed CFD start to the crossover stop signal.) The TAC accepts start and stop inputs of $\geq$5ns. If it receives a start and no stop it will clear itself when it goes overrange. It also accepts a reset input with pulses $\geq$10ns.
Start will be a fixed input from the CFD pulse.
Stop will be a fixed input from the back edge of the fast trigger pulse, i.e. common stop[6].

Note that the present trigger specification allows for a worst case channel to channel skew of 5ns in the fast trigger signal (TAC stop). Within a single channel the successive pulses will all arrive with exactly the same delay relative to the generation of the fast trigger pulse so there is virtually no variation with time (except for drift with voltage or temperature), only from detector to detector. The effect would only be seen when superimposing spectra and would not have any effect on the shape of any single time spectrum. The channel to channel skew comes from the crate backplane, from the board to board variation and from cables which are not matched exactly. The problem is compounded by the fact that TAC chips will be matched to 2% from chip to chip, so typically 2% channel to channel misalignment will be introduced between spectra. Again, the shape is unaffected but there is a fixed shift in position from channel to channel.

4 Digitization

Implementation will be on a small pcb, combining DIL ADC and adder. The serial to parallel readout ASIC and the DAC will be mounted separately on the main pcb. The sliding scale circuit is required to obtain a differential non-linearity of better than $\pm$1%.

4.1 ADC

Each Ge channel will have 4 high resolution ADCs for the 2 energy ranges and the 2 TACs. The chosen ADC is the Burr Brown PCM78P 16 bit successive approximation ADC. Its input range is $\pm$3v, but it is intended to use only the negative half of this range unless resolution problems are encountered with this restricted range. The ADC will not be required to work to 16 bits of accuracy; the hardware removes the 3 lsbs and shifts the data down by 3 places so that a 16 bit word with the top 3 bits set to 0 followed by 13 bits of data is presented to the readout system by the readout FIFO. The PCM78P has no internal sample and hold stage, so the voltage for conversion must be held externally; in this system it will be in the Peak Detect and Hold circuit (section 3.4). The ADC converts in 4.25μs using an external clock of 4MHz. The ADC output is serial (MSB first), and emerges as it is generated during conversion. There are no user controllable parameters in this ADC although during commissioning the sliding scale and DC offset can be adjusted.

4.2 Sliding scale correction and serial to parallel conversion

The serial to parallel conversion of the high resolution ADC output and most of the sliding scale circuit are implemented in the readout ASIC, each chip handling 4 or 6 ADCs with

[6]This means that we start the TAC with the lower rate signal and stop with the higher rate signal since the coincidence rate will usually be greater than the singles rate.

a common sliding scale counter. (Strasbourg design handles 4 ADCs; the Grenoble design handles 6 ADCs.) The chip also provides a programmable digital lower threshold. (Grenoble design has upper threshold too.) This can be used to select certain energy or time ranges, and maybe could remove the 20 MeV ADC from readout for low energy gamma rays. The sliding scale counter and digital subtraction stages are in the ASIC and it provides a serial output to the external DACs generating the analogue value to be added to the ADC input. The ASIC also holds the 14 bit ADC address in a register, and reads in the 2 qualifier bits with every ADC word.

5 Readout

Readout within the card takes place in 2 phases: reading from ADCs to the readout ASIC and then into the readout FIFO.

Each readout ASIC handles 4 or 6 of the 16 bit ADCs, providing each ADC with serial to parallel conversion, sliding scale correction, a lower digital threshold and a register for the 14 bit ADC address plus the 2 qualifiers[7]. There is an internal daisy chained system for readout, enabling each of the 32 bit data words onto the internal bus into the readout FIFO. The Readout ASICs will contain a register to enable or to mask each parameter under software control so as to avoid wasting valuable readout time on parameters which are not required on all experiments.

The readout FIFO collects all the parameters from its card (i.e. up to 24) and allows fast readout of each card without having to switch different bus drivers on and off while selecting different readout chips etc. It also allows a faster mode of operation whereby the Ge card works in a simple pipelined mode by allowing the next event to start as soon as the data are in the Ge readout FIFO, so removing the card readout time from the system deadtime in Common deadtime operation. This mode of operation will only be possible if the noise generated does not degrade analogue performance and so should not be assumed by physicists to be definitely available. It requires that the Ge cards (and BGO cards) drive the Coding* line, each releasing it as soon as the data are all in the Ge readout FIFO ready for readout. In both cases the Reading* (Lecture*) line is driven by the Ge card to indicate to the ROCO that it wants to send data for event being read, and released to indicate that the data has been transmitted. (See EDOC063, Specification of VXI readout mechanism.)

6 Local Trigger

This is the section of the channel which controls its operation. It will be implemented as a sub-module using SMT on a small pcb. It contributes to the formation of the global fast trigger decision and acts on the results. It also detects and signals pileup.

A full description is given in a separate document describing the Eurogam Local Trigger. Briefly, the trigger system uses a fast trigger and a slower validation signal. The fast trigger is normally generated from multiplicity information collected via the sumbuses and will arrive typically 300ns after the CFD has fired. Its back edge stops the TAC and the level is sampled by the Ge card to determine whether to continue and code the event or to stop after pulse shaping. The second signal is the validation which is generated after the fast trigger. It may be either a coding validation (i.e. allow coding) if it is generated before peaking, or readout

[7]The qualifiers on the energy words indicate pre and post pulse pileup; those on the timing words will be set to 00 and reserved for allocation later.

validation if it is generated after peaking. In both cases it logically indicates that readout will take place if a validation pulse exists when sampled by the Ge card; if coding validation is used then there is no further explicit readout validation.

The local trigger has 4 programmable parameters; 3 are set across the whole board and one is set per channel. Each channel has its own validation sample point which may be adjusted to compensate for the variation in timing ramps between channels. The fast trigger sample point is common to all channels in a card. The other 2 common parameters are the PDS gate DAC and the Readout DAC. The PDS gate is automatically opened when the CFD fires, and is closed at a time determined by the PDS DAC. This time is also used to generate the Encode command to the ADCs. The Readout DAC determines when the ROCI chips should pass their data to the event data FIFO. It should be programmed to be between 4.5μs and 5μs after the end of the PDS gate.

Timing will be performed using ramp generators started by the CFD over ranges of 2μs (for fast trigger) and 10μs (for validation). Timing points will be defined by DAC/comparator combinations using 8 bit accuracy to resolve down to 8ns for the fast trigger and 40ns for validation (this might be improved in phase 2 by the use of offsets or different DACs; in phase 1 we are limited by the mis-matching of the timing ramps between local trigger modules which is between $\pm1\%$ and $\pm2\%$ maximum.) Note that the 10μs range limits the time we can wait for validations. The system trigger specification allows this time to be as long as required at the expense of deadtime, but this implementation of the Ge card will limit it to 10μs. The 10μs limit comes from the comparator having a 3V range and 3mV sensitivity which defines a theoretical 10 bit range. In fact we use an 8 bit DAC. We can then choose to run for 5μs with 20ns steps (too short), 10μs with 40ns steps (the selected mode of operation) or longer than 10μs with coarser resolution (not worthwhile to degrade step size to cater for tiny fraction of experiments).

6.1 Compton Suppression

Compton Suppression will be performed in hardware using individual suppression as a method of data rate reduction. Shared suppression will be implemented in software.

For anti-Comptoning, the Ge card will accept veto signals from its associated BGO shields by one of two possible routes; either via the VXI local bus or via a fast NIM front panel input. In both cases the timing is the same and the veto must completely overlap the Ge CFD output. The effect is to prevent the contribution of that channel to the clean multiplicity sumbus. Optionally (under software control) the veto may also disable the local trigger to prevent the Ge channel responding to a fast trigger arising from the event. This is controlled by the module control register mark/reject bit. Pileup can also be optionally used in generating clean multiplicity (see section 6.2). Using local bus obviously requires that the Ge and its associated shield are in adjacent VXI slots. The BGO card will be on the left of the Ge card when seen from the front panel, i.e. BGO is in lower numbered slot.

6.2 Pileup

Pre-pulse pileup is detected by using the Berkeley method of pileup detection rather than using the BLR threshold. This method of pileup detection allows pre pulse pileup as long as the preceding tail will not overlap the following peak (based on linear superposition)[8] It will

[8] Goulding, Landis and Madden IEEE-NS30 p301-310.

be implemented to increase throughput and will use a monostable to time the period when pulse may not arrive.

Post-pulse pileup is detected by looking for a second firing of the CFD during the time that the peak detection gate is open (i.e. from initial CFD pulse to peaking time).

The effect of pileup detection is to set one of the 2 qualifier bits in the top 2 bits of the 32 bit data word, bit 31 (msb) for pre-pulse and bit 30 (msb-1) for post-pulse pileup. It will also be possible to inhibit the channel on detecting pre-pulse pileup. This will be enabled and disabled from software on a per card basis although the user will only be able to set the entire array in reject mode or mark mode.

Pre-pulse pileup will also be used, under software control, in the generation of the clean Ge multiplicity along with the front panel veto signal. This will be enabled and disabled from software at the same time as selecting whether to use reject or mark mode for pileup respectively, i.e. in 'reject' mode we also include pileup in clean Ge multipicity, but not in 'mark' mode.

7 Diagnostics and Testing Facilities

The card will supply 3 types of testing and diagnostic information: the 2 analogue inspection lines, the 2 digital inspection lines and the front panel LEDs. It will also provide a test pulser which will simulate the tail pulses from the preamplifier.

Analogue monitoring points will be switched to one of two VXI local bus line for observation on an oscilloscope at the front panel of the RM (or by a simple DSO built into the RM and the display software). Each channel has 8 analogue monitoring points, which may be connected to either inspection line, thus permitting the comparison of any 2 signals from 1 or 2 channels.

- Shaping amplifier gain stage output (clipped) for PZ adjustment.
- 4 MeV output
- 20 MeV output
- TAC output
- TFA output
- TFA input
- BDC correction signal (4 MeV)
- BDC correction signal (20 MeV)

Logic inspection lines may similarly be connected by multiplexers under software control to one of the following points in a channel:

- CFD output before output delay (direct CFD output)
- CFD output after output delay
- Fast Trigger sample point
- Validation sample point

- Pileup monostable (pre-pulse)
- PDS gate (and Encode)
- ?
- ?

The logic inspection lines will also monitor the following 8 points on a per card basis, appearing to the software control like a 7th channel:

- Fast Trigger Pulse (delayed to compensate for track length)
- Validation pulse
- Readout gate (logical OR of all 6 readout gate signals)
- Data available signal from ROCI
- Data accepted signal from FIFO to ROCI
- ADC clock
- ?
- ?

There will be 7 front panel LEDs. 6 will be allocated to the 6 CFDs. The CFD will trigger a monostable driving a LED every time it fires, so the LEDs should appear to be constantly on in normal operation. The 7th LED will indicate errors in the readout FIFOs, in particular it will light if the 2 halves of the FIFO get out of synchronization.

There will also be a test input to each channel, isolated by a buffer and DMOS transistor, which provides pulses to the receiver hybrid in place of a preamplifier. The pulse amplitude will be programmable with 16 bit precision in each of 2 ranges. The pulses will be provided from a transistor chopper circuit synchronized to the VXI 'synchro test' line to simulate an event.

8 Setup

The setup of the system is described separately in a document called 'Setup using Eurogam Ge and BGO cards' by Bentley and Lazarus.

The Ge TACs are calibrated by taking spectra in them from a source with and without an accurate delay in the master trigger card. The shift in peak position when the delay is introduced corresponds to the delay length which can be measured to whatever accuracy is required.

Ge CFD current pulses are aligned at the master trigger card. This uses a TAC in the master trigger card started by the multiplicity for Ge being ≥ 1 and stopped by a delayed signal from a fast scintillator placed near the source. Each channel is aligned in turn using one as a reference spectrum.

9 Setup of Ge cards

9.1 Programmable Parameters

9.1.1 Parameters common to whole module

- CFD width adjust: 8 bit DAC (1 per module) [w]
- Fast trigger window start (sample point): 8 bit DAC (1 per module) [w]
- Validation (Sample Point) 8 bit DAC (1 per module) [w]
- Start Readout (8 bit DAC (1 per module) [w]
- Test generator: 16 bit DAC, (1 per module) [w]
- Analogue Multiplexer control word (1 per module) [r/w]
- Digital Multiplexer control word (1 per module) [r/w]
- Voltage Inspection Line Control (1 per module) [r/w]
- CDF Control (Contrôle des Fenêtres) (1 per module) [r/w]
- Module Configuration Register (1 per module) [r/w]
- Test generator attenuator on/off (1 per module) [w]
- Test access to readout FIFO (write) (1 per module) [w]
- Test access to readout FIFO (read) (1 per module) [r]

9.1.2 Parameters for each of the 6 channels

- CFD threshold: 8 bit DAC (1 per channel) [w]
- CFD Output delay: 8 bit DAC (1 per channel) [w]
- Pole zero adjustment: 8 bit DAC (1 per channel) [w]
- PDS gate: 8 bit DAC (Start Coding) (1 per channel) [w]
- ROCI ADC low threshold (4 or 6 per channel) [w]
- ROCI ADC Address (4 or 6 per channel) [w]
- ROCI test read of ADC address and data (4 or 6 per channel) [r/w]
- ROCI Sliding scale enable register (1 per channel) [r/w]
- ROCI parameter readout enable/disable (1 per channel) [r/w]
- ROCI Sliding scale register (1 per module) [r]
- ROCI test register (1 per module) [w]
- Channel Control Register (CCR) (1 per channel) [r/w]:

- Channel inhibit/enable: (1 bit per channel) (in CCR)
- Test Mode on/off (1 bit per channel) (in CCR)
- Internal/External amplifier selected. (1 bit per channel) (in CCR)
- Ballistic Deficit correction on/off (1 bit per channel) (in CCR)
- TFA gain (1 bit per channel) (in CCR)
- Disable VXI Local bus Veto signals (1 bit per channel) (in CCR)

9.1.3 Address space Allocation

Starting from the VXI offset address the Ge card will have 7 address spaces, each 256 bytes long. Space 0 contain module parameters and spaces 1-6 will contain channel parameters. So we have:

- 000-0FE Module parameters
- 100-1FE Channel 1 parameters
- 200-2FE Channel 2 parameters
- 300-3FE Channel 3 parameters
- 400-4FE Channel 4 parameters
- 500-5FE Channel 5 parameters
- 600-6FE Channel 6 parameters

The Ge card will conform to the VXI configuration and operational register scheme as set out in section C of the VXI specification. (see section 11).

10 Mechanical and Electrical Specification

This section defines the electrical and mechanical interface for all signals which will pass through either the front panel or the VXI bus.

10.1 Mechanical Interface

- All VXI connections are fully defined mechanically in the VXI bus Specification and require no further definition.
- Front panel connectors are used for inputs from preamplifiers, external shaping amplifiers (GI) and BGO vetos and for outputs from the CFDs.
  - All signals from preamplifiers will come into the unit via BNC sockets, 1 per preamplifier (differential operation not supported). Total 6 BNC sockets. *It is not clear if BNC sockets will be floating instead of grounded. The first prototype will have some channels with floating BNCs and some grounded to evaluate the noise performance with both types of grounding arrangements.*
  - All external amplifier outputs will come into the unit via BNC sockets, one per channel. Total 6 BNC sockets.

- All BGO veto signals will come into the unit via Lemo 00 sockets, total 6 Lemo 00 sockets.
- All front panel CFD outputs will go through IDC ribbon cable connectors (e.g. 3M M50 system) from a 16 way latched header with 6 differential signal pairs and four grounds, 2 on each edge of the cable.

10.2 Electrical Interface

All VXI signals will conform to the VXI bus specification. VXI Local Bus signals will all be in the range ± 5.5V (class3, Analog Low). Some will, in fact, be logic signals using TTL or ECL. (See section 10.3)
Where LBUS lines are bussed, the VXI cards will link LBUSnA to LBUSnC; the backplane will not be modified.
Analog sumbus will receive 1 mA per active Ge channel.
Front panel CFD outputs will be differential ECL.
Front panel Veto inputs will be fast NIM levels.

10.2.1 Terminations

Terminations will be provided for the STARX always.

When the card is driving the analogue inspection lines (LBUS2,3) it will also switch in a series termination. At other times it will switch a relay contact to short the a and c rows of the connector and provide a bus connection to the modules further down the crate.

The sumbus, event number and contrôle des fenêtres lines must be terminated at both ends. This is easy for the slot 0 end, but the other end varies depending on how many cards are in the crate. The Ge card which is furthest to the right (the highest MODID line number) must terminate these signals on lines LBUS0,1,5 and LBUS8-11 (sumbuses, Contrôle des fenêtres and event number assignment). Of course the Ge card must be told whether to switch these terminations in or out by software in the resource manager. This is achieved by setting a bit in the module configuration register.

Details of LBUS terminations will be found in the document 'Utilisation des lignes VXI' by Alphonse Richard; all other terminations are specified in the VXIbus specification and the VMEbus specification.

10.3 Use of VXI lines

The following VXI lines are available to the Ge card:

- STARX (Fast trigger input) [Differential ECL]
- STARY *not used (fast trigger output)*
- ECLTRIG0 (Validation) [Single ended ECL]
- ECLTRIG1 (Synchronise triggers in test mode) [Single ended ECL]
- ECLTRIG2 *not used in Common Deadtime (Inhibit_req)*
- ECLTRIG3,4 (2) (Logic Inspection) [Single ended ECL]
- ECLTRIG5 *not used (Validation 2)*
- TTLTRIG0 *not used (Codage*)*
- TTLTRIG1* (Lecture*) [Open collector TTL]
- TTLTRIG2* *not used (Mémorisation échelles*)*
- TTLTRIG3* (Init*) [single ended TTL]
- TTLTRIG4* (Marche*) [single ended TTL]
- TTLTRIG5* *not used (Rejet d'évènement*)*
- TTLTRIG6* *not used (validation 3*)*
- TTLTRIG7* Inhibit_Action* [singled ended TTL]
- SUMBUS (Raw Ge multiplicity) [1mA per active channel]
- LBUS0 (Clean Ge multiplicity) [same electrical specification as SUMBUS; 1mA per active channel]
- LBUS1 *not used (BGO multiplicity)*
- LBUS2-3 (2) Analogue inspection(2) [analogue, 50Ω series, ±5V maximum]
- LBUS4 REN daisy chain for readout [Single ended TTL]
- LBUS5 Contrôle des fenêtres [50Ω current summing bus]
- LBUS6 Mesure de tensions (±5V maximum using attenuators)
- LBUS8-11 (4) (Event number assignment) [single ended ECL]
- LBUS12-17 (6) (BGO Veto inputs) [Single ended ECL]
- all VME lines (readout and setup)

11 Software Interface

Each board, i.e. 6 Ge channels, will occupy one VXI Logical Address. The board will provide configuration registers within the 256 byte area allocated to its Logical Address in accordance with the VXI specification relating to Register based devices. Dynamic configuration will be supported.

Some of the configuration information is device specific and so the following information should be taken together with the appropriate parts of the VXI specification document. The Ge card will contain a PROM with the following information:

- Manufacturer ID (offset 00)
- Model Code (4 bits revision level, 8 bits board type) in Device type reg (Offset 02)
- Serial number (16 bits) (offset 08)
- Modification level (16 bits) (offset 10)

This PROM will also contain the program for the RAM based LCA chip which will control the VME interface to the Ge card. All the PROM parameters will be read only and so cannot be changed from software.

All VME accesses for setup will be 16 bits wide, using D0 to D15. The only 32 bit access will be reading the ROCI for testing, and read/write access to the FIFO for testing. No DACs will be readable. Control registers will have full read/write access except in the ROCI registers for ADC address which are write only but may be read back via the test read addresses.

Appendix Register layout

The VXI configuration registers are defined by the fact that this is a register based device. The offset register points to the start of the first of 7 memory spaces containing the parameters common to the whole module in the first space and the parameters for each of the 6 channels in the next 6 spaces. Each memory space is 256 bytes long.

The following table uses addresses which will be used in software; in hardware the A0 line does not exist, the DS0* and DS1* being used to select either or both bytes within a memory half word address. The lack of the A0 is hidden from software by the VME hardware, so the following table will be written assuming an address offset defined by A10-A00. This is largely academic since the accesses are all 16 bits (apart from ROCI test reads and FIFO accesses which are 32 bits) so A0 is always 0 (i.e. both DS0* and DS1* are driven). This address field is subdivided as follows:

- A10, A09, A08 define the address space (channel)
- A07, A06, A05 define the function inside the channel (DACs, ROCI etc.)
- A04, A03, A02, A01, A00 identify the exact register within the function (selects a DAC such as Fast Trigger timing or a particular mux control word.)

Some addresses may not be fully decoded in hardware, so some registers might be repeated in unused addresses.

Note that the required memory field in the Device type register must force the offset register to be on a 64Kbyte boundary (m=12 in the VXI specifications).

```
Name: CFD Width DAC                       Offset: @0000  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   | 8 bit DAC for CFD output width|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Name: Fast Trigger Sample point DAC (W1)  Offset: @0002  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   | 8 bit DAC for FT sample point |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0us
1111 = 2us     1 bit = 8ns

Name: Validation Sample point (W2)      Offset: @0004  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   | 8 bit DAC for Val. Sam. point |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0us
1111 = 10us   1 bit = 40ns

Name: Start Readout DAC (W3)             Offset: @0006  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   | 8 bit DAC for Start of Readout|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0us
1111 = 10us   1 bit = 40ns
Note: This DAc is fixed by hard or to be set at 3 volts ( 10 us)
```

```
Name: Test Generator DAC              Offset: @0010  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|msb       16 bit DAC for test generator output level       lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: Analog Multiplexer Control      Offset: @0030  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|Select Parameter   |Sel Channel|Select Parameter   |Sel Channel|
| Inspection line 2 |for line 2 | Inspection line 1 |for line 1 |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
Sel Channel:
000 = disconnected from inspection line    100 = channel 4 connected
001 = channel 1 connected                  101 = channel 5 connected
010 = channel 2 connected                  110 = channel 6 connected
011 = channel 3 connected                  111 = not used.
```

Only 3 of the 5 parameter selection lines are used, the other 2 are left at 00 and are included for compatibility with the BGO card registers.

Select Parameter: (Code allocation will take place after routing board:done)

Parameter	code	Parameter	code
PZ adjustment	0	TFA output	5
4 MeV unipolar output	1	TFA input	6
20 MeV unipolar output	2	BDC correction (4 MeV)	4
TAC output	3	PDS 4 MeV out	7

```
Name: Digital Multiplexer Control       Offset: @0032  read/write
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|Select Parameter   |Sel Channel|Select Parameter   |Sel Channel|
| Inspection line 2 |for line 2 | Inspection line 1 |for line 1 |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
Sel Channel:
000 = disconnected from inspection line    100 = channel 4 connected
001 = channel 1 connected                  101 = channel 5 connected
010 = channel 2 connected                  110 = channel 6 connected
011 = channel 3 connected                  111 = other mux connected
                                                 (``Channel 7'')
```

Only 3 of the 5 parameter selection lines are used, the other 2 are left at 00 and are included for compatibility with the BGO card registers.

Select Parameter (channels 1 to 6): (Codes to be allocated after pcb routing: done)

Parameter	code	Parameter	code
Direct CFD output	3	Validation sample	5
Delayed CFD output	0	Pileup monostable (pre-pulse)	1
PDS gate (Encode/start conversion)	2	Reset Local Trigger	6
Fast Trigger sample	4	Encode commande	7

Select Parameter (``Channel 7''): (Codes to be allocated after pcb routing: done)

Parameter	code	Parameter	code
Fast Trigger Pulse	0	ROCI data acknowledge	3
Validation Pulse	1	ADC Clock	5
Readout gate (OR of ch1-6)	?	EOC (End of Coding)	2
ROCI data ready	4	Last Pass	6
OR TM (OR Temps Motr codage)	7		

```
Name: Voltage Inspection Line Control    Offset: @0034  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |Select input to    |  Select   |
|   |   |   |   |   |   |   |   | multiplexer       |Multiplexer|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

The Ge card has only three 16:1 multiplexers, but the additional selection bits are included for compatibility with the BGO card and for future enhancements.

Register	Channel	Select Mux	Select Input
deconnexion	-	0	-
CFDThresh	1	1	0
CFDDelay	1	1	1
PZAdj	1	1	2
PDSGate	1	1	3
CFDThresh	2	1	4
CFDDelay	2	1	5
PZAdj	2	1	6
PDSGate	2	1	7
CFDThresh	3	1	8
CFDDelay	3	1	9
PZAdj	3	1	10
PDSGate	3	1	11
CFDThresh	4	1	12
CFDDelay	4	1	13
PZAdj	4	1	14
PDSGate	4	1	15
CFDThresh	5	2	0
CFDDelay	5	2	1
PZAdj	5	2	2
PDSGate	5	2	3

CFDThresh	6		||	2	4
CFDDelay	6		||	2	5
PZAdj	6		||	2	6
PDSGate	6		||	2	7
TstGen	7	(*)	||	2	8
CFDWidth	7	(*)	||	2	9
FTSample (W1)	7	(*)	||	2	10
ValSample (W2)	7	(*)	||	2	11
StRdOut (W3)	7	(*)	||	2	12

(*) all channels common

œ

VOLTAGE	SELECT_MUX	SELECT_INPUT
VREF DAC	3 0	
- 24	3	1
- 18	3	2
- 12	3	3
- 6	3	4
- 5,2	3	5
- 2	3	6
		7 not used
0	3	8
5 VA	3	9
5	3	10
6	3	11
12	3	12
18	3	13
20	3	14
24	3	15

```
Name: Controle des fenetres           Offset: @0036  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |on/|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |off|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
(1=on, 0=off)
The controle des fenetres output generates current pulses from
certain combinations of logic inspection lines such as
fast trigger pulse on logic inspection line 1 and
fast trigger sample point on logic inspection line 2.
The output will be rubbish unless the logic inspection lines are set
correctly.


Name: Module Configuration register    Offset: @0038  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|emp|   |   |   |   |   |   |   |   |   |   |   |   |   |acc|End|
|fifo   |   |   |   |   |   |   |   |   |   |   |   |   |rej|mod|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
End Module (End mod) set by RM software  1 = last module
(Controls terminators)                   0 = not last module

Accept/Reject: Action on detecting       0 = accept event
Pileup or Compton scattering             1 = reject event
(For Compton scattering, this bit disables (if=1) Veto input only)
(For Pileup this bit says mark with qualifier (if =1) or reject (=0))

empty fifo bit : indicates if the readout FIFO is empty or not :
       if empty fifo = 0 ... the readout FIFO is empty
       if empty fifo = 1 ... the readout FIFO is not empty


Name: Test Generator Attenuator        Offset: @003A  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |on/|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |off|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
Switches attenuator in and out to reduce test pulse height
1 = attenuator used
0 = attenuator not used
```

```
Name: Test Write to readout FIFO       Offset: @003C   write only

31              23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|   |   |   |   |   |   |   |   |
|q q|A A A A A A A A A A A A A A|   |   |   |   |   |   |   |   |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

Writes will put data into the FIFO Directly : D16-D31, long word addressing.
This facility allows testing of the fast readout mechanism independently of the analogue part of the board and of the trigger system.

```
Name: Test Read from readout FIFO      Offset: @003C   read only

31              23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|   |   |   |   |   |   |   |   |
|q q|A A A A A A A A A A A A A A|   |   |   |   |   |   |   |   |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: CFD Threshold DAC        Offset: @0100 (channel 1)   write only
                                       @0200 (channel 2)
                                       @0300 (channel 3)
                                       @0400 (channel 4)
                                       @0500 (channel 5)
                                       @0600 (channel 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   |  8 bit DAC for CFD threshold  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 keV
1111 = 1.28 MeV   1 bit= 5 keV   for high gain TFA setting

0000 = 0 keV
1111 = 5 MeV      1 bit = 20 keV for low gain TFA setting
```

```
Name: CFD Additional
     Output Delay DAC         Offset: @0102 (channel 1)   write only
                                      @0202 (channel 2)
                                      @0302 (channel 3)
                                      @0402 (channel 4)
                                      @0502 (channel 5)
                                      @0602 (channel 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   | 8 bit DAC for CFD output delay|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0ns
1111 = 255ns      1 bit= 1ns


Name: PZ adjustment DAC       Offset: @0104 (channel 1)   write only
                                      @0204 (channel 2)
                                      @0304 (channel 3)
                                      @0404 (channel 4)
                                      @0504 (channel 5)
                                      @0604 (channel 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   |  8 bit DAC for PZ adjustment  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: PDS gate (Start Coding)
                               Offset: @0106 (channel 1) write only
                                       @0206 (channel 2)
                                       @0306 (channel 3)
                                       @0406 (channel 4)
                                       @0506 (channel 5)
                                       @0606 (channel 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |msb                         lsb|
|   |   |   |   |   |   |   |   |       8 bit PDS Gate DAC      |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

0000 = 0 us
1111 = 10 us      1 bit = 40ns
```

ROCI registers shown for Strasbourg chip to illustrate the type of parameters which must be controlled and how we might do it. Order of 20 MeV, 4 MeV, FT TAC and CO TAC will be determined when the board has been tracked to allow optimal tracking.

```
Name: ROCI 20 MeV ADC low threshold
                               Offset: @0140 (channel 1)   write only
                                       @0240 (channel 2)
                                       @0340 (channel 3)
                                       @0440 (channel 4)
                                       @0540 (channel 5)
                                       @0640 (channel 6)


31              23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|20 MeV ADC digital low threshol|                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI 4 MeV ADC low threshold
                              Offset: @0144 (channel 1)   write only
                                      @0244 (channel 2)
                                      @0344 (channel 3)
                                      @0444 (channel 4)
                                      @0544 (channel 5)
                                      @0644 (channel 6)


31             23             15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|4 MeV ADC digital low threshold|                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+



Name: ROCI ADC low threshold   Offset: @0148 (channel 1)   write only
      (Fast Trigger TAC ADC)          @0248 (channel 2)
                                      @0348 (channel 3)
                                      @0448 (channel 4)
                                      @0548 (channel 5)
                                      @0648 (channel 6)

31             23             15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|FT ADC digital lower threshold |                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+


Name: ROCI ADC low threshold   Offset: @014C (channel 1)   write only
       (Crossover TAC ADC)            @024C (channel 2)
                                      @034C (channel 3)
                                      @044C (channel 4)
                                      @054C (channel 5)
                                      @064C (channel 6)

31             23             15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|CO ADC digital lower threshold |                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI ADC Address         Offset: @0150 (channel 1)   write only
      (20 MeV ADC)                     @0250 (channel 2)
                                       @0350 (channel 3)
                                       @0450 (channel 4)
                                       @0550 (channel 5)
                                       @0650 (channel 6)

31             23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
| | |20 MeV ADC Address(14 bits)|                               |
|q|q|-----------+---------------|                               |
| | |Item(6bits)| Group (8bits) |                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI ADC Address         Offset: @0154 (channel 1)   write only
      (4 MeV ADC)                      @0254 (channel 2)
                                       @0354 (channel 3)
                                       @0454 (channel 4)
                                       @0554 (channel 5)
                                       @0654 (channel 6)

31             23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
| | |4 MeV ADC Address (14 bits)|                               |
|q|q|-----------+---------------|                               |
| | |Item(6bits)| Group (8bits) |                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI ADC address         Offset: @0158 (channel 1)   write only
      (Fast Trigger TAC ADC)           @0258 (channel 2)
                                       @0358 (channel 3)
                                       @0458 (channel 4)
                                       @0558 (channel 5)
                                       @0658 (channel 6)

31              23              15              07              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
| | | FT ADC Address (14 bits)  |                               |
|q|q|-----------+---------------|                               |
| | |Item(6bits)| Group (8bits) |                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI ADC address         Offset: @015C (channel 1)   write only
       (Crossover TAC ADC)             @025C (channel 2)
                                       @035C (channel 3)
                                       @045C (channel 4)
                                       @055C (channel 5)
                                       @065C (channel 6)

31              23              15              07              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
| | | CO ADC Address (14 bits)  |                               |
|q|q|-----------+---------------|                               |
| | |Item(6bits)| Group (8bits) |                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI Test Read           Offset: @0160 (channel 1)   read only
      (20 Mev ADC)                     @0260 (channel 2)
                                       @0360 (channel 3)
                                       @0460 (channel 4)
                                       @0560 (channel 5)
                                       @0660 (channel 6)

31              23              15              07              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|                               |
|q q|A A A A A A A A A A A A A A|                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI Test Read          Offset: @0164 (channel 1)   read only
      (4 Mev ADC)                     @0264 (channel 2)
                                      @0364 (channel 3)
                                      @0464 (channel 4)
                                      @0564 (channel 5)
                                      @0664 (channel 6)

31             23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|                               |
|q q|A A A A A A A A A A A A A A|                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Name: ROCI Test Read          Offset: @0168 (channel 1)   read only
      (FT TAC ADC)                    @0268 (channel 2)
                                      @0368 (channel 3)
                                      @0468 (channel 4)
                                      @0568 (channel 5)
                                      @0668 (channel 6)

31             23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|                               |
|q q|A A A A A A A A A A A A A A|                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Name: ROCI Test Read          Offset: @016C (channel 1)   read only
      (CO TAC ADC)                    @026C (channel 2)
                                      @036C (channel 3)
                                      @046C (channel 4)
                                      @056C (channel 5)
                                      @066C (channel 6)

31             23              15              07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|                               |
|q q|A A A A A A A A A A A A A A|                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI Sliding Scale       Offset: @0170 (channel 1)   read/write
      Enable Register                  @0270 (channel 2)
                                       @0370 (channel 3)
                                       @0470 (channel 4)
                                       @0570 (channel 5)
                                       @0670 (channel 6)

 31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15........0
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+-----------+
|   |   |   |   |   |   |   |   |   |   |   |   |CO |FT |4  |20 |           |
|   |   |   |   |   |   |   |   |   |   |   |   |TAC|TAC|MeV|MeV|           |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+-----------+

Name: ROCI Parameter Readout   Offset: @0174 (channel 1)   read/write
      Enable register                  @0274 (channel 2)
                                       @0374 (channel 3)
                                       @0474 (channel 4)
                                       @0574 (channel 5)
                                       @0674 (channel 6)

 31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15........0
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+-----------+
|   |   |   |   |   |   |   |   |   |   |   |   |CO |FT |4  |20 |           |
|   |   |   |   |   |   |   |   |   |   |   |   |TAC|TAC|MeV|MeV|           |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+-----------+

Name: ROCI Sliding Scale Reg   Offset: @0178 (channel 1)   read only
                                       @0278 (channel 2)
                                       @0378 (channel 3)
                                       @0478 (channel 4)
                                       @0578 (channel 5)
                                       @0678 (channel 6)

 31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15.........0
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+-----------+
|       Sliding Scal  Register for ROCI                         |           |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+-----------+
```

```
Name: ROCI Test Register       Offset: @017C (channel 1)   write only
                                       @027C (channel 2)
                                       @037C (channel 3)
                                       @047C (channel 4)
                                       @057C (channel 5)
                                       @067C (channel 6)

31             23             15             07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|       ROCI Test Register     |                               |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+



Name: Channel Control Register Offset: @0120 (channel 1)   read/write
                                       @0220 (channel 2)
                                       @0320 (channel 3)
                                       @0420 (channel 4)
                                       @0520 (channel 5)
                                       @0620 (channel 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |Ch |TST|BDC|TFA|V  |Ext|
|   |   |   |   |   |   |   |   |   |   |dis|   |   |   |   |amp|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Channel Control Register contains:

Channel Disable        (bit 5)  0=disabled, 1=enabled
Test Mode Enable       (bit 4)  1=test mode, 0=normal
BDC on/off             (bit 3)  1=BDC on, 0=BDC off
TFA Gain (x1 or x5)    (bit 2)  1=low gain, 0=high gain
Veto from LBUS/Lemo    (bit 1)  1=Lemo, 0=VXI LBUS
Int/Ext amplifier      (bit 0)  1=External, 0=Internal
```