EDOC132

EUROGAM PROJECT

EUROGAM DATA ACQUISITION SYSTEM

ROCO Card Register Layout Specification

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ROCO Card Register Layout Specification

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This document has been written by P. Kadionik (CENBG) from the reference document : EDOC077, ROCO VXI Unit Specifications by J.L. Pedroza.

Here is the list of Controlable Parameters :

1 Controlable Parameters :

VXI standard registers (VXI norme 1.3) :

- ManID register : 16 bits [rw]
- Device type/Model code : 16 bits [r]
- Status/Control register : 16 bits [rw]
- Offset register : 16 bits (unused)

VXI user specified registers :

- Serial number register : 16 bits [r]
- Modification level register : 16 bits [r]

VXI device dependant registers :

- Endsubevent register : 32 bits [rw]
- ROCO control/status register : 16 bits [rw]
- Word count register : not accessible via the VME bus
- Data fifo test register : 32 bits [w]
- Event number test register : 4 bits [w]
- Event number register : not accessible via the VME bus
- Time outs register : 16 bits [w]
- Interrupt/bus request register : 8 bits [w]

2 Address space allocation :

- 000-03F Module parameters

The ROCO card is a A16 VXI "register based" device.
The VXI A16 base address of the ROCO card is fixed by the VXI autoconfiguration software.

3 Register layout :

Note : bits fields or bits without label are undefined or unused.

```
Name: VXI ID Register                   Offset: @0000     read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|                               |       Logical Address         | write
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|Dev Typ|Add Spa|               Manufacturer ID                 | read
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Add Spa = 0x3 : Address Space is A16 only
Dev Typ = 0x3 : Device Type is "register based" device

Name: VXI Device Type register          Offset: @0002     read

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|                         Model Code                            |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Model Code = 0x0100 (256) for the ROCO card
```

```
Name: VXI Control/Status register       Offset: @0004     read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|                                                           |Res| write
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |Mod|                                       |Rea|Pas|   |Res| read
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Control bits (write) :
Res : Reset is set by writing a 1 and is cleared by writing 0, or by
      SYSRESET*
Status bits (read) :
Res : reflect of Reset bit in control register
Pas = 0x1 : Passed set to 1
Rea = 0x1 : Ready set to 1
Mod       : Modid*

Name: VXI Offset register              Offset: @0006     read
Unused

Name: Serial Number register           Offset: @0008     read

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|                         Serial Number                         |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Name: Modification Level register      Offset: @000A     read

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|                      Modification Level                       |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: Endsubevent register              Offset: @000C     read/write

31              23             15                07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|err|ROCO number|End Sub Event  |                               | write
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|err|ROCO number|End Sub Event  |   Word Count          |Evt Nbr| read
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

The D16-D31 bits are written from the VME, but the bit D31 is set
by a ROCO card if there is a Event Number Fault (ENF).
The D00-D15 bits are generated by the ROCO card.

```
Name: Data Fifo Test register          Offset: @0010     write

31              23             15                07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|                      Data Fifo Test                           |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

Writing in this register causes the data to be pushed in the data
fifo if the TEST bit of control register is enable.

```
Name: Event Number Test register       Offset: @0014     write

31              23             15                07             00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|                                                       |Evt Nbr|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

Writing in this register causes the 4 bits data to be pushed in the
Event Number fifo if the TEST bit of control register is enable.

```
Name: ROCO Control/Status register     Offset: @0016     read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|ENF|TOR|       |DTP|               |EDTS|Int|Int|IRF|Tst|Res|Ena| write
|   |   |       |   |               |    |TO |ENF|   |   |   |ROC|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|ENF|TOR|           |DFF|EFF|FE |                       | 0 |   | read
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

See the EUROGAM document EDOC077 for more details.

```
Name: Time Outs register              Offset: @0018     write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|                               |   Time Out 1  |   Time Out 2  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Time Out 1 : 128 micro seconde max, step 8 micro seconde
     Time Out for the readout (TOR)
Time Out 2 : 1 micro seconde max, step 62 nano seconde
     Time Out for the BLTACK*

Name: Interruption/Bus Request register Offset: @001A    write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|                               |BR Lev |           |Int Level  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

BR Level  : Bus Request Level from 0 to 3
Int Level : Interrupt Request Level from 0 to 7
```