EDOC127

EUROGAM PROJECT

EUROGAM DATA ACQUISITION SYSTEM

BGO Card Register Layout Specification

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BGO Card Register Layout Specification

This document is aggreeded by G. BOSSON, N. KARKOUR

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Here is the list of Controlable Parameters

1 Parameter Common to whole module

- Veto width: 8 bit DAC (1 per module) [w]
- Dead time discriminators width: 8 bit DAC (1 per module) [w]
- Sum I multiplicity width: 8 bit DAC (1 per module) [w]
- Fast trigger width (w1): 8 bit DAc (1 per module) [w]
- Validation (Sample Point) (w2): 8 bit DAC (1 per shield) [w]
- Start Readout width (w3): hard-fixed to 3 volts (i.e. 10 us) [r]
- PDS gate width: 8 bit Dac (1 per module) [w]
- Analogue Multiplexer control word: 16 bit (1 per module) [r/w]
- Digital Multiplexer control word: 16 bit (1 per module) [r/w]
- Voltage Inspection line Control: (1 per module) [r/w]
- CDF (Contrôle des Fenêtres) (1 per module) [r/w]
- Module Configuration Register (1 per module) [r/w]
- Test access to readout FIFO (write) (1 per module) [w]
- Test access to readout FIFO (read) (1 per module) [r]

2 Parameter for each of the 6 shields

- Discriminator threshold: 12 bit DAC (1 per shield) [w]
- Test generator: 12 bit DAC (1 per shield) [w]
- Channel Control Register(CCR): 11 bit register (1 per shiled) [r/w]
- ROCI ADC low threshold (3 per shield) [r/w]

- ROCI ADC Address (3 per shield) [r/w]
- ROCI ADC test read of ADC address and data (3 per shield) [r/w]
- ROCI Sliding scale enable register (1 per shield) [r/w]
- ROCI parameter readout enable/disable (1 per shield) [r/w]
- ROCI Sliding scale register (1 per shield) [r/w]
- ROCI test register (1 per shield) [w]

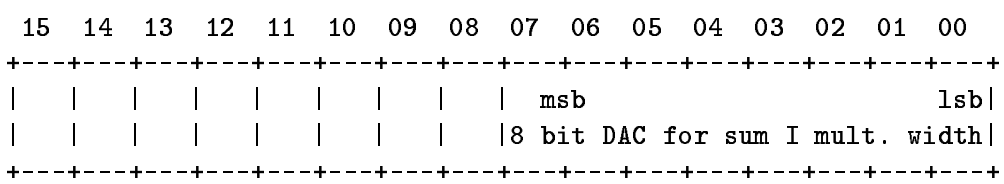
3 Address space Allocation

- 000-0FE Module parameters
- 100-1FE shield 1 parameters
- 200-2FE shield 2 parameters
- 300-3FE shield 3 parameters
- 400-4FE shield 4 parameters
- 500-5FE shield 5 parameters
- 600-6FE shield 6 parameters

4 Register layout

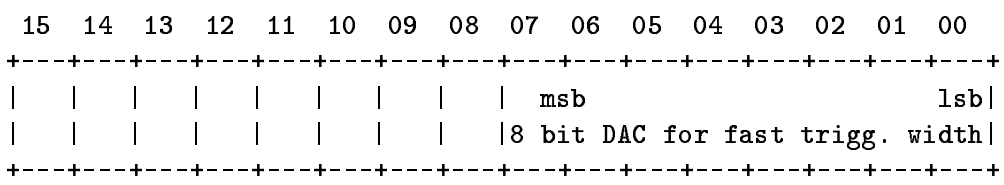
```
Name: Veto width  DAC                    Offset: @0000     write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00

+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  msb                      lsb|
|   |   |   |   |   |   |   |   |   8 bit DAC for veto width    |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 100  ns
1111 = 1000 ns   1 bit = 4 ns


Name: Dead time discriminator width DAC    Offset: @0002   write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |  msb                      lsb|
|   |   |   |   |   |   |   |   | 8 bit DAC for dead time width |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 2  us
1111 = 20 us   1 bit = 80 ns
```

Name: Sum I multiplicity width DAC Offset: @0004 write only



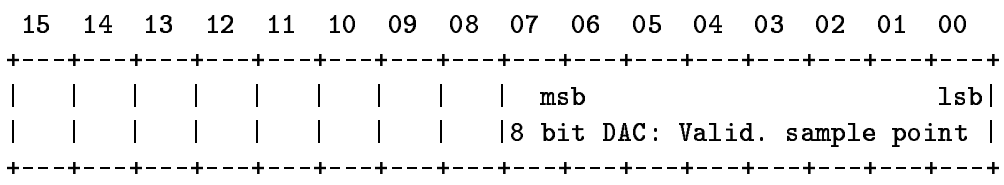
0000 = 100 ns
1111 = 1000 ns 1 bit = 4 ns

Name: Fast trigger width DAC Offset: @0006 write only



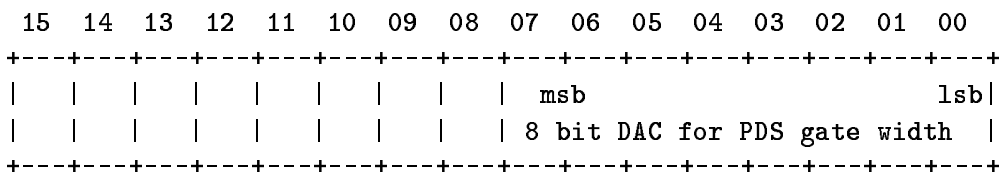
0000 = 0 us
1111 = 2 us 1 bit = 8 ns

Name: Validation Sample Point Offset: @0008 write only



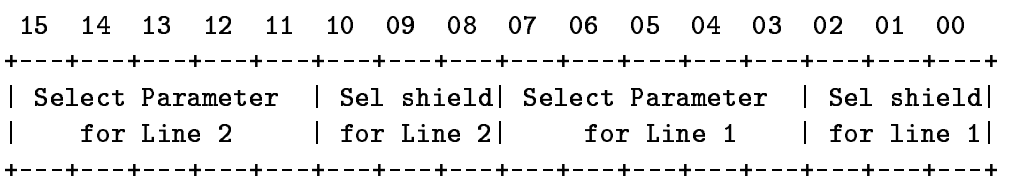
0000 = 0 us
1111 = 10 us 1 bit = 40 ns

Name: PDS gate width DAC Offset: @000B write only



0000 = 0 us
1111 = 10 us 1 bit = 40 ns

Name: Analogue multiplexor Control Offset: @0030 read/write



Name: Digital multiplexor Control Offset: @0032 read/write

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Select Parameter for Line 2							Sel shield for Line 2		Select Parameter for Line 1					Sel shield for line 1	

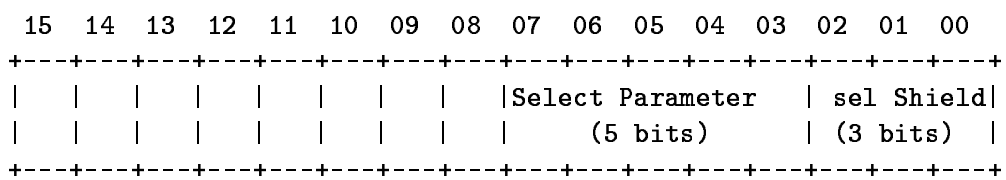
Sel shield: (for Analogue and Digital Multiplexer)

000 = disconnected from inspection line	100 = channel 4 connected
001 = channel 1 connected	101 = channel 5 connected
010 = channel 2 connected	110 = channel 6 connected
011 = channel 3 connected	111 = not used ?

Select Parameter: (for Analogue and Digital Multiplexer)

Analogique	Logique	Select Parameter
Line Receiver BGO a	Discriminator Output BGO a	00
Line Receiver BGO b	Discriminator Output BGO b	01
Line Receiver BGO c	Discriminator Output BGO c	02
Line Receiver BGO d	Discriminator Output BGO d	03
Line Receiver BGO e	Discriminator Output BGO e	04
Line Receiver BGO f	Discriminator Output BGO f	05
Line Receiver BGO g	Discriminator Output BGO g	06
Line Receiver BGO h	Discriminator Output BGO h	07
Line Receiver BGO i	Discriminator Output BGO i	08
Line Receiver BGO j	Discriminator Output BGO j	09
TAC output	Start TAC	10
Shaping filter output	Fast Tigger	11
Peak detector output	PDS GATE	12
Test generator output	Fast Trigger Window	13
BGO j input	Validation Sample point	14
BGO i input	Local Trigger gate 3	15
BGO h input	Dead time discriminator Gate	16
BGO g input	OR (discriminator output)	17
BGO f input	Discriminator veto	18
BGO e input	Validation Ack	19
BGO d input	Encode commande	20
BGO c input	Valid 2	21
BGO b input	INHIBIT	22
BGO a input	Reset Local trigger	23

Name: Voltage Inspection Line Control Offset: @0034 read/write



Note: Select Shield is set to 0.

Select Parameter (5 bits)	Parameter
0	DAC output: Fast Trigger Width
1	DAC output: SUM I Multiplicity
2	DAC output: Dead Time Discriminator Width
3	DAC output: Veto Width
4	DAC output: Test Generator Shield 6
5	DAC output: Test Generator Shield 5
6	DAC output: Test Generator Shield 4
7	DAC output: Test Generator Shield 3
8	DAC output: Test Generator Shield 2
9	DAC output: Test Generator Shield 1
10	DAC output: Discriminator threshold Shield 6
11	DAC output: Discriminator threshold Shield 5
12	DAC output: Discriminator threshold Shield 4
13	DAC output: Discriminator threshold Shield 3
14	DAC output: Discriminator threshold Shield 2
15	DAC output: Discriminator threshold Shield 1
16, 17, 18	unused
18	Voltage measurement (Alim) +24 volts (not yet implemented)
19	Voltage measurement (Alim) -24 volts
20	Voltage measurement (Alim) -12 volts
21	Voltage measurement (Alim) -6 volts
22	Voltage measurement (Alim) -5.2 volts
23	Voltage measurement (Alim) -2 volts
24	Voltage measurement (Alim) +3 volts Reg
25	Voltage measurement (Alim) +5 volts DAC
26	Voltage measurement (Alim) +5 volts
27	Voltage measurement (Alim) +6 volts
28	Voltage measurement (Alim) +12 volts
29	DAC output: PDS GAte Width
30	unused
31	DAC output: Start readout Width

Note about parameter 18 to 28: After measurement, each voltage must be multiplied bye 10 because all the voltages are divided by 10 before they are measured. The voltages are divided by 10 because one can't drawn more than 12 vots through the multiplexer lines.

```
Name: Controle des fenetres          Offset: @0036   read/write
      (will be implemented later)

  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |on/|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |off|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
(1=on, 0=off)


Name: Module Configuration       Offset: @0038   read/write
      Register

  15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |End|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |mod|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
End mod = 1 (if last module)
End mod = 0 (if not last module)


Name: Test Write to readout FIFO      Offset: @003C     write only

31              23              15               07              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|   |   |   |   |   |   |   |   |
|q q|A A A A A A A A A A A A A A|   |   |   |   |   |   |   |   |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Writes will put data into the FIFO directly. That is, for write
operation only D16 to D31 are needed.


Name: Test Read to readout FIFO      Offset: @003E    read only

31              23              15               07              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|   |   |   |   |   |   |   |   |
|q q|A A A A A A A A A A A A A A|   |   |   |   |   |   |   |   |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
Read byte: D16-D31
```

```
Name: Discriminator threshold DAC      Offset: @0100 (shield 1) write only
       @0200 (shield 2)
       @0300 (shield 3)
       @0400 (shield 4)
       @0500 (shield 5)
       @0600 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   | msb                                       lsb|
|   |   |   |   | 12 bit DAC for Discriminator threshold       |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 volts
1111 = 5 volts    1 bit = 3 mv
```

Note: There is a divider (by 10) after the DAC. So, the value to be written in the DAC must be multiplied by 10 before writing it. Here is the effective range (after the division):

```
0000 = 0 volts
1111 = 0.5 volts    1 bit = 0.3 mv
```

exemple: to get 100 mv as the threshold one will write 1000 mv (1 volt) in the DAC.
But for the "Mesure de tension" operation the measurement is done before the value is divided: the measured value is the value written in the DAC.

```
Name: Test generator DAC              Offset: @0102 (shield 1) write only
      @0202 (shield 2)
      @0302 (shield 3)
      @0402 (shield 4)
      @0502 (shield 5)
      @0602 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   | msb                                       lsb|
|   |   |   |   | 12 bit DAC for Test Generator                |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0000 = 0 volts
1111 = 5 volts    1 bit = 3 mv
```

Name: Channel Control Register (CCR)
Offset: @0120 (shield 1) read/write
@0220 (shield 2)
@0320 (shield 3)
@0420 (shield 4)
@0520 (shield 5)
@0620 (shield 6)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
					ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF

Shield Disable/Enable (bit 10) 1=disabled, 0=enabled

important: bit 0 to 10 allocation

1) Test mode: using Test Generator.

BG0a Disable/Enable (bit 0) 1=enabled, 0=disabled
BG0b Disable/Enable (bit 1) 1=enabled, 0=disabled
BG0c Disable/Enable (bit 2) 1=enabled, 0=disabled
BG0d Disable/Enable (bit 3) 1=enabled, 0=disabled
BG0e Disable/Enable (bit 4) 1=enabled, 0=disabled
BG0f Disable/Enable (bit 5) 1=enabled, 0=disabled
BG0g Disable/Enable (bit 6) 1=enabled, 0=disabled
BG0h Disable/Enable (bit 7) 1=enabled, 0=disabled
BG0i Disable/Enable (bit 8) 1=enabled, 0=disabled
BG0j Disable/Enable (bit 9) 1=enabled, 0=disabled

2) Normal mode: in normal mode, both bit 0 to bit 9 are set to 0 (i.e all channel
disabled)

```
Name: ROCI ADC low threshold     Offset: @0140 (shield 1)  read/write
      (Pattern)                          @0240 (shield 2)
 @0340 (shield 3)
 @0440 (shield 4)
 @0540 (shield 5)
 @0640 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb                                                       lsb|
|                 Pattern ADC Lower Threshold                  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC low trheshold           Offset: @0142 (shield 1)  read/write
      (TAC ADC)                                @0242 (shield 2)
       @0342 (shield 3)
       @0442 (shield 4)
       @0542 (shield 5)
       @0642 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb                                                       lsb|
|                    TAC ADC Lower Threshold                   |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

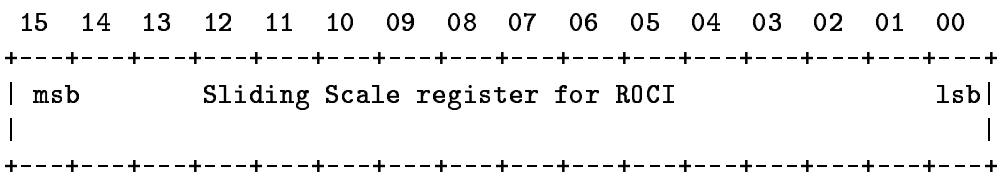
```
Name: ROCI ADC  low threshold    Offset: @0144 (shield 1)  read/write
      (Energy Shield)                    @0244 (shield 2)
 @0344 (shield 3)
 @0444 (shield 4)
 @0544 (shield 5)
 @0644 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb                                                       lsb|
|                    Energy Shield lower threshold             |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC Address      Offset: @0148 (shield 1)  write only
      (Pattern)                     @0248 (shield 2)
    @0348 (shield 3)
    @0448 (shield 4)
    @0548 (shield 5)
    @0648 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb                                                       lsb|
|                 ROCI ADC Address  (Pattern)                   |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC Address       Offset: @014A (shield 1)  write only
      (TAC ADC)                     @024A (shield 2)
     @034A (shield 3)
     @044A (shield 4)
     @054A (shield 5)
     @064A (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb                                                       lsb|
|                    TAC ADC Address                            |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI ADC Address           Offset: @014C (shield 1)  write only
      (Energy ADC)                       @024C (shield 2)
 @034C (shield 3)
 @044C (shield 4)
 @054C (shield 5)
 @064C (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb                                                       lsb|
|                     Energy ADC Address                        |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: ROCI Test Read         Offset: @0150 (shield 1)  read only
       Pattern                       @0250 (shield 2)
     @0350 (shield 3)
     @0450 (shield 4)
     @0550 (shield 5)
     @0650 (shield 6)

31              23              15    12                3       00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls| 2 | Pattern  data     | 3 bit |
|q q|A A A A A A A A A A A A A A|bit|D D D D D D D D D D|       |
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
10 Pattern bits: D12-D3
bits D14 to D13 and D2 to D1 not used


Name: ROCI Test Read         Offset: @0152 (shield 1)  read only
     (TAC ADC)                     @0252 (shield 2)
     @0352 (shield 3)
     @0452 (shield 4)
     @0552 (shield 5)
     @0652 (shield 6)

31              23              15                07              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|ms  TAC  ADC  data word      ls|
|q q|A A A A A A A A A A A A A A|0 0 0 D D D D D D D D D D D D|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+


Name: ROCI Test Read         Offset: @0154 (shield 1)  read only
      (ENERGY ADC)                   @0254 (shield 2)
     @0354 (shield 3)
     @0454 (shield 4)
     @0554 (shield 5)
     @0654 (shield 6)

31              23              15                07              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|qfy|ms ADC Address (14 bits) ls|ms   Energy ADC data word    ls|
|q q|A A A A A A A A A A A A A A|0 0 0 D D D D D D D D D D D D|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: ROCI Sliding scale     Offset: @0158 (shield 1)  read/write
      Enable Register               @0258 (shield 2)
     @0358 (shield 3)
     @0458 (shield 4)
     @0558 (shield 5)
     @0658 (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |ENE|TAC|PAT|
|   |   |   |   |   |   |   |   |   |   |   |   |   |RGY|   |TER|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
bit 0 (Pattern readout enable) must be set to 0.


Name: ROCI Parameter Readout    Offset: @015A (shield 1)  read/write
      Enable Register                   @025A (shield 2)
@035A (shield 3)
@045A (shield 4)
@055A (shield 5)
@065A (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |ENE|TAC|PAT|
|   |   |   |   |   |   |   |   |   |   |   |   |   |RGY|   |TER|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: ROCI Sliding scale     Offset: @015C (shield 1)  read only
      Register                      @025C (shield 2)
     @035C (shield 3)
     @045C (shield 4)
     @055C (shield 5)
     @065C (shield 6)

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| msb        Sliding Scale register for ROCI                lsb|
|                                                              |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

Name: ROCI test Register
Offset: @015E (shield 1) @025E (shield 2) write only
@035E (shield 3)
@045E (shield 4)
@055E (shield 5)
@065E (shield 6)