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EUROBALL Project

A.P. Description & Memory Map For

General Interface Readout Master Trigger

Ver 0.1 (**Draft** version for Master Trigger Board)

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1. AP Description. This paragragh details the signals of **Table1**.

• 1.1) AP1 :

- DCLK : Clock signal to load the *DAC*s, this signal is common for all the *DAC*s (see fig. *Dacs connections*).

- DDIN : serial data signal to load the *DACs*, this signal is common all the *DAC*s (see fig. *Dacs connections*).

- DCS*n* : Chip Select signal to load the *DAC*s, there is one signal per *Dac*, *n* = 1 to 7 (see fig. *Dacs connections*).

- SCR-signal **:** System Control Register, each signal enable or disable a function on the *Master Trigger*:

SCR-Clear ==> set/reset* the *VXI Clear* Line.
SCR-TSync ==> set/reset* the *VXI Trigger Sync Pulse* Line.
SCR-vxiGo ==> set/reset* the *VXI Go/Stop* Line.
SCR-CDT ==> en/dis* Deadtime or Parallel/Pipelined mode.
SCR-Complet ==> select Source for 'Readout Complete' in CDT mode. (0= Readout)
SCR-Scalers ==> en/dis* the *VXI* Transfer Scalers to shadow register.

- BCR1-signal**:**Board Control Register1, each signal enable or disable a function on the *Master Trigger*:

BCR1-enbS*n* ==> en/dis* Sumbus *n* (*n* = 1 to 4).
BCR1-rdoS*n* ==> en/dis* Sumbus *n* for Readout (*n* = 1 to 4).
BCR1-ftval ==> en/dis* Fast Trigger and Validation Pattern for Readout.
BCR1-fttac ==> en/dis* Fast Trigger *TAC* for Readout.
BCR1-evlsb ==> en/dis* Event Number *LSB* for Readout.
BCR1-evmsb ==> en/dis* Event Number *MSB* for Readout.

- CLKProm: Clock signal of the serial E²Prom X25C02 on the *Master Trigger*.

- DProm_Write: Data write to the E²Prom X25C02 on the *Master Trigger*.

- CSProm : Chip Select signal of the serial E²Prom X25C02 on the *Master Trigger*.

- DProm_Read: Data to be read out of the E²Prom X25C02 on the *Master Trigger*.
(see E²Prom connection figure).

- BCR2-signal**:**Board Control Register2, each signal enable or disable a function on the *Master Trigger*:

BCR2-sel[1..0] ==> select Validation Line
00 ==> not used, 01 ==> Validation 1.
10 ==> Validation 2, 11 ==> Validation 3.
BCR2-clrScal ==> Clear all Scalers on the card, n = Clear.
BCR2-LCA[2..0]==> *FT/VAL LCA* mode controls.
BCR2-clrfifo ==> Reset Triggers FIFOs, and States Machines.
Enable-TAC-ADC==> TAC-ADC enable
TAC-Start-Sel[1..0]==> Select Start TAC
TAC-Stop-Sel[1..0]==> Select Stop TAC
Tref enable ==> Enable Tref
Sum-Comp-Sel[1..0]==> Select Sumbus Comparator

- SBSR-signal **:** System/Board Status Register, each signal is a status of an action on the Analog part :

SBSR-vxiGo ==> status of the *VXI Go/Stop* Line.
SBSR-inh-req ==> status of the *VXI Inhibit Request* Line.
SBSR-inh-act ==> status of the *VXI Inhibit Action* Line.
SBSR-prog[4..1]==> status of the good programmation of the *LCAs*.
SBSR-prog 1 : Xilinx_Done
SBSR-prog2 : Rdo_Xil_Done
SBSR-prog3 : Scaler1_Prog_Done
SBSR-prog4 : Scaler2_Prog_Done
SBSR-fifo[1..0] ==> status of the ADC FIFO Flags.
SBSR-fifo0 : TT_Fifo_FF
SBSR-fifo1 : TT_fifo_EF

- SCR-signal **:** Scaler Control Register :

SCR-enb*n* ==> en/dis* Scaler Control *n* (*n* = 1 to 8).

- SSR-signal **:** Scaler Status Register :

SSR-ovf*n* ==> Status of Scaler Overflow *n* (*n* = 1 to 8).

- FT-VAL-sel : Chip select for the *FT/VAL* LCA register area (0x400 to 0x5FE).

- FTV-lca-din : Serialised data for the *LCA*. (register address 0x300)

- FTV-lca-clk : Clock for serial slave programming mode. (register address 0x300)

- ADD[7..1] : this is the lowest byte of the *VME* Address bus, it is enabled by the *LCA DECOD1*.

- Spare : these signals are not used in the *Euroball Master Trigger* card, they are controlled by the *LCA DECOD1*. They can be used for future upgrades.

- VPTAT1 : Voltage Proportional To Absolute Temperature signal of the sensor 1 from the *Master Trigger* and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER1 : high level temperature signal of the sensor 1 from the *Master Trigger*.

- UNDER1 : low level temperature signal of the sensor 1 from the *Master Trigger*.

- LED Temp: display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel for the temperature Alarm. Color : **RED**. **(Led connection figure will be added!)**.

• 1.2) AP2 :

- BCR2_LCA_Spare : spare signal for the loading of the FTV LCA.

- WP_Prom: en/dis*Enable or disable the protection on the Identification serial prom.

- 16 MHz: buffered *VME* System Clock signal.

- ADD8 : bit 8 of the *VME* Address bus, it is enabled by the *LCA DECOD1*.

- AIn **:** Analogue Inspection Lines, n is the inspection line indicator.

- DIn **:** Digital Inspection Lines (must not be charge because they are driven 50 Ω to -2V on thr *GIR*), n is the inspection line indicator. If the lignes are inactive, the level **MUST BE 0 logic *ECL***.

- VI : Voltage Inspection Line.

- DATA[15..0] : these are the lower sixteen bits of the *GIR* Data bus.

- RDO-EVTIN[3..0] : these lines are the current event number, they are sent by the *MASTER Trigger* via the *VXI Local* bus to the Analog cards (LBus [11..8]).

- RDO-Dtready : data ready given by the *MASTER Trigger Readout Interface* when a data is ready to be latched in the *FIFO*.

- RDO-DTack : buffered data acknowledge signal for each data word of the *MASTER Trigger Readout Interface* during a Readout cycle.

- RDO-Renin : start Readout cycle of the *MASTER Trigger Readout Interface*.

- RDO-LPASS : Last PASS, done signal of the *MASTER Trigger Readout Interface* at the end of the internal Readout cycle.

- GLOBAL RESET : buffered global Reset signal of all the *Master Trigger*.

- R/W_buf : buffered *VME* read-write signal.

-StartReadout : the rising edge of this signal starts the internal Readout cycle.

- LT_Reset : buffered Reset signal witch tells the Master Trigger that readout is finished.

- Clk25MHz

- Read Spare : these signals are dedicated for Readout interface and are not used in the *Euroball MASTER Trigger* card, they are controlled by the *LCA READOUT*. They can be defined for future applications.

- Spare : these signals are not used in the *Euroball MASTER Trigger* card, they are controlled by the *LCA DECODE2*. They can be defined for future applications.

- VPTAT2 : Voltage Proportional To Absolute Temperature signal of the sensor 2 from the Analog part and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER2 : high level temperature signal of the sensor 2 from the *Master Trigger*.

- UNDER2 : low level temperature signal of the sensor 2 from the *Master Trigger*.

- FIFO-ERROR : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel It indicates the FIFO Event Error. Color : **RED**. **(Led connection figure will be added!)**.

• 1.3) AP3 :

- DATA[31..16] : these are the sixteen higher bits of the *GIR* Data bus.

- RDO-evtout[3..0] : these lines are the event number that are sent with the data during acquisition mode, and are written in the *FIFO*.

- DSPFLAG1, 2, 3 : not used by the Master Trigger

- DONE-LED : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel This signal indicates that the G.I.R. LCAs are fully programmed, or Done LCAs is all High. Color: **GREEN (Led connection figure will be added!)**.

- Read Spare : these signals are dedicated for Readout interface and are not used in the *Euroball Master Trigger* card, they are controlled by the *LCA READOUT*. They can be defined for future applications.

- **Val_buf :** buffered *Validation* signal from the *MASTER Trigger* (on the *VXI* back plane).

All the signals below are controlled by the *LCA DECODE2*.

- RGI-select : Chip select for the *RGI* register, which is latched with the *STROBE-reg*.

- RGI-Read : enable RGI datas on the bus.

- SCALER-sel : select the Scaler address range, which is latched with the *STROBE-reg.*

- SCALER-en : enable the Scaler datas on the bus.

- DigOeA : enable signal of the digital multiplexers for the Digital Inspection Line 1.

- DigOeB : enable signal of the digital multiplexers for the Digital Inspection Line 2.

- DigStrobe1 : Latch the data of the digital multiplexers for the digital inspection line 1.

- DigStrobe 2 : Latch the data of the digital multiplexers for the digital inspection line 2.

- AnaSelAn **:** select signal of the Analog multiplexers for the Analog Inspection Line 1, *n* is the multiplexer select bit. n=0,1,2.

- AnaSelBn **:** select signal of the Analog multiplexers for the Analog Inspection Line 2, *n* is the multiplexer select bit. n=0,1,2.

- AnEnA : enable signal of the Analog multiplexers for the Analog Inspection Line 1.

- AnEnB : enable signal of the Analog multiplexers for the Analog Inspection Line 2.

- Anastrobe: load signal of all the Analog multiplexers.

- VSel[3..0] : select bus of the voltage multiplexers. These signals must be common to all voltage multiplexers.

- Venablen **:** enable signal of the voltage multiplexers.n=1,2,3.

- Vstrobe: load signal of all the voltage multiplexers.

- STROBE-reg: Data Strobe signal for the *Master Trigger card* registers.

- XilinxSel : Selects between 63 direct signals and Xilinx signals.

- FTV_Xilinx_Init : Status of Init Signal for the FTV Xilinx LCA.

- RDO_Xilinx_Init : Status of Init Signal for the RDO Xilinx LCA.

Pinouts of the AP Connector for the Master Trigger Card: (Table 1):

	AP1 Connector			AP2 Connector			AP3 Connector			
PIN NO.	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	PIN NO.
1	+5 V	VPTAT1	+5 V	+5 V	VPTAT2	+5 V	+5v	FreeFLAG1	+5v	1
2	+5 V	+5 V	+5 V	+5 V	+5v	+5 V	+5v	+5v	+5v	2
3	DCLK	OVER1	DDIN	Spare	OVER2	BCR2-LCA-Spare	DATA 16	Free FLAG2	DATA 17	3
4	DCS 1	UNDER1	DCS 2	Spare	UNDER2	Spare	DATA 18	Free FLAG3	DATA 19	4
5	DCS 3	LED Temp	DCS 4	WP-PROM	FIFO-ERROR	Spare	DATA 20	DONE-LED	DATA 21	5
6	DCS 5	GND	DCS 6	16 Mhz	GND	Spare	DATA 22	GND	DATA 23	6
7	DCS 7	GND	SCR-Clear	GND	GND	Spare	GND	GND	GND	7
8	SCR-TSync	GND	SCR-vxiGo	ADD 8	GND	Spare	DATA 24	GND	DATA 25	8
9	SCR-CDT	GND	SCR-Complet	Spare	GND	Spare	DATA 26	GND	DATA 27	9
10	SCR-Scalers	GND	BCR1-enbS1	Spare	GND	Spare	DATA 28	GND	DATA 29	10
11	BCR1-enbS2	GND	BCR1-enbS3	Spare	GND	Spare	DATA 30	GND	DATA 31	11
12	BCR1-enbS4	GND	BCR1-rdoS1	Spare	GND	Spare	GND	GND	GND	12
13	BCR1-rdoS2	GND	BCR1-rdoS3	Spare	GND	Spare	RDO-evtout0	GND	RDO-evtout1	13
14	BCR1-rdoS4	GND	BCR1-ftval	Spare	GND	Spare	RDO-evtout2	GND	RDO-evtout3	14
15	BCR1-fttac	GND	BCR1-evlsb	Spare	GND	Spare	Read Spare	GND	Read Spare	15
16	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	16
17	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	17
18	BCR1-evmsb	GND	Clk Prom	Spare	GND	Spare	Spare	GND	LC 2	18
19	DProm_Write	GND	CS Prom	Spare	GND	Spare	Spare	GND	Read Spare	19
20	DProm_Read	GND	BCR2-sel0	AI 1	GND	GND	GND	GND	Spare	20
21	BCR2-sel1	GND	BCR2-clrScal	GND	GND	GND	Spare	GND	Spare	21
22	BCR2-LCA0	GND	BCR2-LCA1	AI 2	GND	GND	VAL_buf	GND	ft_VAL_sel	22
23	BCR2-LCA2	GND	BCR2-clrfifo	GND	GND	DI 1	RGI-select	GND	RGI-read	23
24	En-Tac-Adc	GND	Tac-Start-Sel0	DI 2	GND	GND	SCALER-sel	GND	SCALER-en	24
25	Tac-Start-Sel1	GND	Tac-Stop-Sel0	Spare	GND	VI	Spare	GND	Spare	25
26	Tac-Stop-Sel1	GND	Tref-enable	Spare	GND	Spare	Spare	GND	Spare	26
27	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	27
28	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	28
29	Sum-comp-Sel0	GND	Sum-comp-Sel1	DATA 0	GND	DATA 1	DigOeA	GND	DigOeB	29
30	SBSR-vxiGo	GND	SBSR-inh-req	DATA 2	GND	DATA 3	DigStrobe 1	GND	DigStrobe 2	30
31	SBSR-inh-act	GND	SBSR-prog1	DATA 4	GND	DATA 5	AnaSelA 0	GND	AnaSelA 1	31
32	SBSR-prog2	GND	SBSR-prog3	DATA 6	GND	DATA 7	AnaSelA 2	GND	AnaSelB 0	32
33	SBSR-prog4	GND	SBSR-fifof0	GND	GND	GND	AnaSelB 1	GND	AnaSelB 2	33
34	SBSR-fifofl1	GND	SCR-enb1	DATA 8	GND	DATA 9	AnaEnA	GND	AnaEnB	34
35	SCR-enb2	GND	SCR-enb3	DATA 10	GND	DATA 11	AnaStrobe	GND	VSel 0	35
36	SCR-enb4	GND	SCR-enb5	DATA 12	GND	DATA 13	VSel 1	GND	VSel 2	36
37	SCR-enb6	GND	SCR-enb7	DATA 14	GND	DATA 15	Vsel 3	GND	Venable 1	37
38	SCR-enb8	GND	SSR-ovf1	RDO-EVTIN0	GND	RDO-EVTIN1	Venable 2	GND	Venable 3	38
39	SSR-ovf2	GND	SSR-ovf3	RDO-EVTIN2	GND	RDO-EVTIN3	VStrobe	GND	Spare	39
40	SSR-ovf4	GND	SSR-ovf5	RDO-Dtready	GND	Read Spare	Spare	GND	Spare	40
41	SSR-ovf6	GND	SSR-ovf7	Read Spare	GND	Read Spare	Strobe_Reg	GND	Spare	41
42	SSR-ovf8	GND	FT-VAL-sel	Read Spare	GND	Read Spare	Spare	GND	Spare	42
43	Spare	GND	FTV-lca-din	RDO-Dtack	GND	RDO-Renin	Xilinxsel	GND	Spare	43
44	FTV-lca-clk	GND	Spare	Read Spare	GND	RDO-LPASS	FTV-Xilinx-Init	GND	Spare	44
45	Latch Card	GND	ADD 1	GlobalReset	GND	R/W_buf	Rdo-Xilinx-Init	GND	Spare	45
46	ADD 2	GND	ADD 3	Spare	GND	StartReadout	Spare	GND	Spare	46
47	ADD 4	GND	ADD 5	LT_Reset	GND	Read Spare	Spare	GND	Spare	47
48	ADD 6	GND	ADD 7	Clk 25MHz	GND	Spare	Spare	GND	Spare	48
49	+5 V	GND	+5 V	+5 V	GND	+5 V	+5 V	GND	+5 V	49
50	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	50
51	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	51
52	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	52
53	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	53
54	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	54
55	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	55
56	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	56

Signal Polarity:

This table describes the signal polarity between the G.I.R. and the Master Trigger:

Note that active high is +4volts, and Active low is 0 volts.

SIGNAL NAME	Polarity
RDO-Dtready	Active HIGH
RDO-Dtack	Active HIGH
GlobalReset	Active Low
VALACK	Active HIGH
LT_Reset	Active Low
RDO-Renin	Active HIGH
RDO-LPASS	Active HIGH
R/W_buf	Write low/ Read High
StartReadout	Active HIGH
Coding	comes from M.T.
RGI-select	Active HIGH
SCALER-sel	Active HIGH
RGI-read	Active HIGH
SCALER-en	Active HIGH
Strobe_Reg	Active HIGH
Xilinxsel	Active HIGH

2. Memory Map of the G.I.R. for the Master Trigger Card

2.1 VXI Configuration Registers: (Inside the G.I.R.)

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11). To Identify the Trigger card is **0x940** in the Device type register

VXI Base Address *(slot 1)*	***Description***	***DATA Format***
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM (0x940 for M.T.)
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8a	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

2.2 DAC Memory Map:

Address Offset	Bus Width	Read/ Write	DAC Parameter Name
Select DAC 1 Parameters			
0x 100	16	w	Sumbus 1: Multiplicity 1:Delay
0x 102	16	w	Sumbus 1: Multiplicity 1:Width
0x 104	16	w	Sumbus 1: Multiplicity 2:Delay
0x 106	16	w	Sumbus 1: Multiplicity 2:Width
0x 108	16	w	Sumbus 1: Multiplicity 3:Delay
0x 10A	16	w	Sumbus 1: Multiplicity 3:Width
0x 10C	16	w	Sumbus 1: Multiplicity 4:Delay
0x 10E	16	w	Sumbus 1: Multiplicity 4:Width
Select DAC 2 Parameters			
0x 110	16	w	Sumbus 2: Multiplicity 1:Delay
0x 112	16	w	Sumbus 2: Multiplicity 1:Width
0x 114	16	w	Sumbus 2: Multiplicity 2:Delay
0x 116	16	w	Sumbus 2: Multiplicity 2:Width
0x 118	16	w	Sumbus 2: Multiplicity 3:Delay
0x 11A	16	w	Sumbus 2: Multiplicity 3:Width
0x 11C	16	w	Sumbus 3: Multiplicity 1:Delay
0x 11E	16	w	Sumbus 3: Multiplicity 1:Width
Select DAC 3 Parameters			
0x 120	16	w	Sumbus 1: Multiplicity 1: Threshold
0x 122	16	w	Sumbus 1: Multiplicity 2: Threshold
0x 124	16	w	Sumbus 1: Multiplicity 3: Threshold
0x 126	16	w	Sumbus 1: Multiplicity 4: Threshold
0x 128	16	w	Sumbus 2: Multiplicity 1: Threshold
0x 12A	16	w	Sumbus 2: Multiplicity 2: Threshold
0x 12C	16	w	Sumbus 2: Multiplicity 3: Threshold
0x 12E	16	w	Sumbus 3: Multiplicity 1: Threshold
Select DAC 4 Parameters			
0x 130	16	w	Sumbus 3: Multiplicity 2: Threshold
0x 132	16	w	Sumbus 4: Multiplicity 1: Threshold
0x 134	16	w	not used
0x 136	16	w	not used
0x 138	16	w	Sumbus 3: Multiplicity 2:Delay
0x 13A	16	w	Sumbus 3: Multiplicity 2: Width
0x 13C	16	w	Sumbus 4: Multiplicity 1: Delay
0x 13E	16	w	Sumbus 4: Multiplicity 1: Width
Select DAC 5 Parameters			
0x 140 -> 0x 14E ????	16	w	Logic Input Reference Level
Select DAC 6 Parameters			
0x 150	16	w	Logic Input 1: Delay
0x 152	16	w	Logic Input 1 : Width
0x 154	16	w	Logic Input 2: Delay
0x 156	16	w	Logic Input 2 : Width
0x 158	16	w	Logic Input 3: Delay
0x 15A	16	w	Logic Input 3 : Width
0x 15C	16	w	Logic Input 4: Delay

0x 15E	16	w	Logic Input 4 : Width
Select DAC 7 Parameters			
0x 160	16	w	Fast Trigger Output Pulse:Delay
0x 162	16	w	Fast Trigger Output Pulse:Width
0x 164	16	w	Fast Trigger to Validation Pulse : Delay
0x 166	16	w	Fast Trigger to Validation Pulse : Width
0x 168	16	w	Validation Output pulse: Delay
0x 16A	16	w	Validation Output pulse : width
0x 16C	16	w	Inhibit Output Pulse : Delay
0x 16E	16	w	Inhibit Output Pulse : Width

2.3 Common Area Addresses

2.3.1 Common Registers:

Global Addresses	Bus Width	Read/ Write	Function
0x 40 -> 0x 5E	16	r only	Board Identification Registers (in DAC EEPROM ?????????)
0x 60 -> 0x 7E	16	r /w	DAC buffer EEPROM read and write defaults
0x 80 -> 0x 9E	16	w only	DAC buffer volatile read/write
0xA0--0xBE	16/32	r/w	G.I.R. Readout Memory Map
Master Trigger Register Area Address			
0x 200	16	r/w	System Control Register
0x 202	16	r/w	Board Control Register 1
0x 204	16	r/w	Board Control Register 2
0x 206	8	r/w	Scaler Control register.
0x 208	16	r only	System/Board Status register
0x 20A	8	r only	Scaler Status register
Inspection Lines Area Address			
0x 220	16	r/w	Logic Inspection Line 1 Channel Select
0x 222	16	r/w	Logic Inspection Line1 Source Select
0x 224	16	r/w	Logic Inspection Line2 Channel Select
0x 226	16	r/w	Logic Inspection Line2 Source Select
0x 228	16	r/w	Analogue Inspection Line 1 Channel Select
0x 22A	16	r/w	Analogue Inspection Line 1 Source Select
0x 22C	16	r/w	Analogue Inspection Line 2 Channel Select
0x 22E	16	r/w	Analogue Inspection Line 2 Source Select
0x 230	16	r/w	Voltage Inspection Line Channel Select
0x 232	16	r/w	Voltage Inspection Line Source Select
0x 234	16	r only	Status of Xilinx_Init Select
0x 236	16	r/w	Module Control Register (MCR)
0x 300	16	w only	FT/VAL programming register
RGI Area Address			
0x 320	16	r/w	Sumbus1 Peak Value: Group and Item number
0x 322	16	r/w	Sumbus2 Peak Value: Group and Item number
0x 324	16	r/w	Sumbus3 Peak Value: Group and Item number
0x 326	16	r/w	Sumbus4 Peak Value: Group and Item number
0x 328	16	r/w	Trigger TAC ADC: Group and Item number
0x 32A	16	r/w	FT/LCA Pattern: Group and Item number
0x 32C	16	r/w	Event Number LSB: Group and Item number
0x 32E	16	r/w	Event Number MSB: Group and Item number
0x 400 -> 0x 600	16	r/w	**Fast Trigger/Validation LCA Area Address**
0x 1000->0x 101C	32	r/w	**Scaler Register Area**

2.3.1.1 Board Identification Register: VME base Address : 0x40 -> 0x5E

Address Offset	*Description*	*DATA Format*
	In Read mode: Status Register **OR** In Read Mode this is the Man. ID	d15 to d0 **OR** D7..D0 from XCPROM ***code CLRC***
	Write mode: Control Register	d15 to d0
	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

2.3.1.2 DAC Buffer EPROM: VME base Address : 0x60 -> 0x7E

Base Addresses	Bus Width	Read/ Write	Function
	16	r/w	Default DAC Buffer **1** values from XCProm
	16	r/w	Default DAC Buffer **2** values from XCProm
	16	r/w	Default DAC Buffer **3** values from XCProm
	16	r/w	Default DAC Buffer **4** values from XCProm
	16	r/w	Default DAC Buffer **5** values from XCProm
	16	r/w	Default DAC Buffer **6** values from XCProm
	16	r/w	Default DAC Buffer **7** values from XCProm

2.3.1.3 DAC Buffer volatile R-W: VME base Address : 0x80 -> 0x9E

Base Addresses	Bus Width	Read/ Write	Function
	16	write only	Change Default DAC Buffer **1** mode in XCProm
	16	write only	Change Default DAC Buffer **2** mode in XCProm
	16	write only	Change Default DAC Buffer **3** mode in XCProm
	16	write only	Change Default DAC Buffer **4** mode in XCProm
	16	write only	Change Default DAC Buffer **5** mode in XCProm
	16	write only	Change Default DAC Buffer **6** mode in XCProm
	16	write only	Change Default DAC Buffer **7** mode in XCProm

2.3.1.4 System Control Register: VME base Address : 0x200

Bit Number	Meaning when = 0	Meaning when = 1
0	Level of VXI Clear line	Level of VXI Clear line
1	Level of VXI Trigger Sync Pulse line	Level of VXI Trigger Sync Pulse line
2	Level of VXI Go/Stop line. (**Stop**)	Level of VXI Go/Stop line. (**Go**)
3	Common Deadtime	Parallel/Pipelined mode
4	Select for 'Readout Complete' in CDT mode. (**Readout**)	Select Source for 'Readout Complete' in CDT mode. (**???????**)
5	Level of VXI Transfer Scalers to shadow register	Level of VXI Transfer Scalers to shadow register
	Not Allocated	Not Allocated

2.3.1.5 Board Control Register 1: VME base Address : 0x202

Bit Number	Meaning when = 0	Meaning when = 1
0	Disable Sumbus 1.	Enable Sumbus 1.
1	Disable Sumbus 2	Enable Sumbus 2
2	Disable Sumbus 3.	Enable Sumbus 3.
3	Disable Sumbus 4.	Enable Sumbus 4
4	Disable Sumbus 1 for readout	Enable Sumbus 1 for readout.
5	Disable Sumbus 2 for readout.	Enable Sumbus 2 for readout.
6	Disable Sumbus3 for readout	Enable Sumbus 3 for readout.
7	Disable Sumbus 4 for readout.	Enable Sumbus 4 for readout.
8	Disable Fast Trigger and Validation Pattern for readout.	Enable Fast Trigger and Validation Pattern for readout.
9	Disable Fast Trigger TAC for readout.	Enable Fast Trigger TAC for readout.
10	Disable Event Number LSB for readout.	Enable Event Number LSB for readout.
11	Disable Event Number MSB for readout.	Enable Event Number MSB for readout.
?? -> ??	Not Allocated	Not Allocated

2.3.1.6 Board Control Register 2: VME base Address : 0x204

Bit Number	Meaning when = 0	Meaning when = 1
0..1	Select Validation Line. 0 = not used	1 = Validation 1, 2 = Validation 2, 3 = Validation 3.
2	Don't Clear all scalers on the card.	Clear all scalers on the card.
5...3	FT/VAL LCA mode controls.	FT/VAL LCA mode controls.
6	Don't Reset Trigger FIFOs , and State Machines.	Reset Trigger FIFOs , and State Machines.
7	Disable TAC ADC	Enable TAC ADC
8	Disable TAC Start Select 0	Enable TAC Start Select 0
9	Disable TAC Start Select 1	Enable TAC Start Select 1
10	Disable TAC Stop Select 0	Enable TAC Stop Select 0
11	Disable TAC Stop Select 1	Enable TAC Stop Select 1
12	Disable Tref	Enable Tref
13	Disable Sumbus Comparator 0	Enable Sumbus Comparator 0
14	Disable Sumbus Comparator 1	Enable Sumbus Comparator 1
15	BCR2_LCA_Spare	BCR2_LCA_Spare

2.3.1.7 Scaler Control Register : VME base Address : 0x206

Bit Number	Meaning when = 0	Meaning when = 1
7:0	Scaler Disable control	Scaler Enable control

2.3.1.8 System/Board Status Register : VME base Address : 0x208

Bit Number	Meaning when = 0	Meaning when = 1
0	VXI **Stop** signal	VXI **Go** signal
1	Level of VXI Inhibit Request signal	Level of VXI Inhibit Request signal
2	Level of VXI Inhibit Action signal	Level of VXI Inhibit Action signal
3	LCAs programmed 1	LCAs programmed 1
4	LCAs programmed 2	LCAs programmed 2
5	LCAs programmed 3	LCAs programmed 3
6	LCAs programmed 4	LCAs programmed 4
7	ADC FIFO Flags status	ADC FIFO Flags status
8	ADC FIFO Flags status	ADC FIFO Flags status
	Not Allocated	Not Allocated

2.3.1.9 Scaler Status Register : VME base Address : 0x20A

Bit Number	Meaning when = 0	Meaning when = 1
7:0	Scaler Normal	Scaler Overflow

2.3.2 Inspection Lines:

2.3.2.1 Digital inspection lines:

Digital Inspection line 1 : VME base Address : 0x220 (channel Select), and 0x222 (Source Select)
To Disable the Digital inspection Line 1 write 0x00 at address 0x220.
Digital Inspection line 2 : VME base Address : 0x224 (channel Select), and 0x226(parameter Select).
To Disable the Digital inspection Line 2 write 0x00 at address 0x224.

parameters Line1 = Line2 =	Xilinx SEl	Data5	GIR Control Lines to Analogue Card DIGOEA DIGOEB	Data Value for Channel Address	Data Value for Source Address [5:0]
Disable	**0**	**x**	**0x0**	0x00	xx
Enable Master Trigger Direct Lines	0	x	0x1	0x1	0x1 to 0x3F
Enable FTV_LCA Signals	1	0	0x1	0x1	0x40 to 0x5F
Enable RDO_LCA Signals	1	1	0x1	0x1	0x60 to 0x7F

G.I.R. Global Parameters	GIR Control Lines	channel Data Value	Parameter Data Value	
Disable		*0x20*	*0x000*	
Fast_Trigger	0x001	0x20	0x001	
Inhibit_buf (M.T.)	0x002	0x20	0x002	
Validation	0x003	0x20	0x003	
Spare	0x004	0x20	0x004	
Valack	0x005	0x20	0x005	
enable address 0xAA with bit 0 of RCR =1 a write = LastPass read=Renin	0x006	0x20	0x006	
Readout Signals between G.I.R. & M.T.				
StartReadout	0x007	0x20	0x007	
Renin	0x008	0x20	0x008	
DTready	0x009	0x20	0x009	
Spare	0x00A	0x20	0x00A	
Spare	0x00B	0x20	0x00B	
Spare	0x00C	0x20	0x00C	
SIROPDTack_buf	0x00D	0x20	0x00D	
Spare	0x00E	0x20	0x00E	
Spare	0x00F	0x20	0x00F	
Spare	0x010	0x20	0x010	
Spare	0x011	0x20	0x011	
SIROPLPASS	0x012	0x20	0x012	
G.I.R. FIFO Signals When data are written in				
CSA *(FifoChipSelect_A)	0x013	0x20	0x013	
CLKA(FifoClock_A)	0x014	0x20	0x014	
ENA(Fifo Enable Port_A)	0x015	0x20	0x015	
Readout Signals between G.I.R. &Readout Controller				
AS* (VME)	0x016	0x20	0x016	
DS (DS0* and DS1*) (VME)	0x017	0x20	0x017	
R/W* (VME)	0x018	0x20	0x018	
ModRoco	0x019	0x20	0x019	
CardRenin *(From ROCO)	0x01A	0x20	0x01A	
BLTACK (Card)	0x01B	0x20	0x01B	
BLTACK (Bus)	0x01C	0x20	0x01C	
OE_Ident*	0x01D	0x20	0x01D	Address 0xA0 readout (32 bits).
G.I.R. FIFO Signals When data are read out				
CSB* (FifoChipSelect_B)	0x01E	0x20	0x01E	
CLKB (FifoClock_B)	0x01F	0x20	0x01F	
ENB (Fifo Enable Port_B)	0x020	0x20	0x020	
OR_fifo (EmptyFlag)	0x021	0x20	0x021	
FDTACK (G.I.R. Readout LCA Dtack)	0x022	0x20	0x022	
DTACK* (VME)	0x023	0x20	0x023	
CardRenout(Bus Renout)	0x024	0x20	0x024	
SysClk (16 MHz)	0x025	0x20	0x025	
LT_Reset*(end of event)	0x026	0x20	0x026	
Readout_evt_match	0x027	0x20	0x027	
Reset_Fifo*	0x028	0x20	0x028	
DecodeSel(CardChipSelect)	0x029	0x20	0x029	
Strobe_Dec2	0x02A	0x20	0x02A	
Dclk	0x02B	0x20	0x02B	
DCS*	0x02C	0x20	0x02C	
DDin	0x02D	0x20	0x02D	
Coding_Bus	0x02E	0x20	0x02E	
Spare	0x02F	0x20	0x02F	
Readout Event Fault more than 1	0x030	0x20	0x030	
Readout Event Fault	0x031	0x20	0x031	
Vme Address 1	0x032	0x20	0x032	
Vme Address 2	0x033	0x20	0x033	
Vme Address 3	0x034	0x20	0x034	
Vme Address 4	0x035	0x20	0x035	
Vme Address 5	0x036	0x20	0x036	
Not Used (DI Disable)	Disable	valus not = 0x20	xxxx	

2.3.2.2 Analog inspection lines:

Analog Inspection line 1 : VME base Address: 0x228 (channel Select), & 0x22A (Source Select).
To Disable the Analog inspection Line 1 write 0x00 at address 0x228.
Analog Inspection line 2 : VME base Address : 0x22C (channel Select), and 0x22E (Source Select).
To Disable the Analog inspection Line 2 write 0x00 at address 0x22C.

parameters Line1 = Line2 =	GIR Control Lines to Analogue Card AI 1 :AnaSelA [2..0] AI 2 :AnaSelB [2..0]	GIR Control Lines to Analogue Card AI 1: AnaEnA AI 2: AnaEnB	Data Value for Channel Address	Data Value for Source Address
Disable	**xx**	**0**	***0x00***	**xx**
??????	000	1	1	000
??????	001	1	1	001
??????	010	1	1	010
??????	011	1	1	011
??????	100	1	1	100
??????	101	1	1	101
??????	110	1	1	110
??????	111	1	1	111

2.3.2.3 Voltage inspection line:

VME base Address : 0x230 (channel select), and 0x232 (Source select).
To Disable the Voltage Inspection line : write 0x00 at address 0x230.

parameters	GIR Control Lines to Analogue Card VSel [3..0]	GIR Control Lines to Analogue Card Venable[2..0]	Data Value for Channel Address	Data Value for Parameter Address
Disable	xxxx	000	***0x00***	xx
??????	0000	001	1	0x00
??????	0001	001	1	0x01
??????	0010	001	1	0x02
??????	0011	001	1	0x03
??????	0100	001	1	0x04
??????	0101	001	1	0x05
??????	0110	001	1	0x06
??????	0111	001	1	0x07
??????	1000	001	1	0x08
??????	1001	001	1	0x09
??????	1010	001	1	0x0A
??????	1011	001	1	0x0B
??????	1100	001	1	0x0C
??????	1101	001	1	0x0D
??????	1110	001	1	0x0E
??????	1111	001	1	0x0F
??????	see above	010	1	0x10 to 0x1F
??????	see above	100	1	0x20 to 0x2F

2.3.3 Global Registers:

2.3.3.1 Xilinx Init Select Status Register: VME base Address : 0x234

Bit Number	Meaning when = 0	Meaning when = 1
0	Disable FT/VAL Xilinx Init .	Enable FT/VAL Xilinx Init .
1	Disable Readout Xilinx Init.	Enable Readout Xilinx Init.

2.3.3.2 Module Control Register: VME base Address : 0x236

Bit Number	Meaning when = 0	Meaning when = 1
0 to 3	Not Allocated	Not Allocated
4	Analog Card PROM Write Disable	Analog Card PROM Write Enable
5to7	Not Allocated	Not Allocated
8	Reset FIFO Disable	Reset FIFO
9	Reset G.I.R. Disable	G.I.R. Reset
10	Not Last Card	Last Card (use terminators)
11	Invert SAROC data in run mode	use normal buffers for SAROC data in run mode
12 TO 15	Not Allocated	Not Allocated

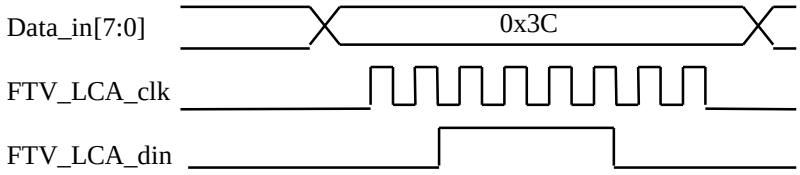
2.3.3.3 FT/VAL Programming Register : VME base Address : 0x300

Bit Number	Meaning when = 0	Meaning when = 1
0	Disable FT/VAL Data in.	Enable FT/VAL Data in.
1	Disable FT/VAL clock.	Enable FT/VAL clock.
?? -> ??	Not Allocated	Not Allocated

LCA programming by VXI bus.

Before downloading LCAs, the bits [5:3] *FTA VAL LCA mode control* of BCR2 register must be initialized.

By writing datas at address 0x300, LCA is directly downloaded. The 8 bits data bus is converted parallele to serial. Serial datas are on the AP1 C43 : FTV_LCA_DIN (LSB first). Each data is latched with the positive edge of the FTV_LCA_CLK : AP1 A44. Setup time = 60 ns (data stable before the rising edge) hold time = 60 ns (data stable after the rising edge of the clock).



2.3.4 Group and Item number Register Area : VME base Address : 0x320 to 0x32E.

0x 320	16	r/w	Event Number LSB: Group and Item number
0x 322	16	r/w	Event Number MSB: Group and Item number
0x 324	16	r/w	FT/LCA Pattern: Group and Item number
0x 326	16	r/w	Trigger TAC ADC: Group and Item number
0x 328	16	r/w	Sumbus1 Peak Value: Group and Item number
0x 32A	16	r/w	Sumbus2 Peak Value: Group and Item number
0x 32C	16	r/w	Sumbus3 Peak Value: Group and Item number
0x 32E	16	r/w	Sumbus4 Peak Value: Group and Item number

2.3.5 Scaler Register Area : VME base Address : 0x1000 to 0x101C.

0x 1000	32	r/w	Scaler 1
0x 1004	32	r/w	Scaler 2
0x 1008	32	r/w	Scaler 3
0x 100C	32	r/w	Scaler 4
0x 1010	32	r/w	Scaler 5
0x 1014	32	r/w	Scaler 6
0x 1018	32	r/w	Scaler 7
0x 101C	32	r/w	Scaler 8

2.3.6 G.I.R. Readout Memory Map : VME base Address : 0xA0 to 0xBE.

Base Addresses	Bus Width	Read/ Write	Function
0xA0	16	r/w	G.I.R. Event Counter Load Register
0xA2	16	r/w	Item + Group no. of the G.I.R. Event Counter Register
0xA0	32	read only	Item + Group no. (16MSB) + Event Counter (16LSB) for the G.I.R. Event Counter Register
0xA4	32	r/w	Fifo Test Enable (Read and Write into the G.I.R. FIFO)
0xA8	16	r/w	G.I.R. Readout Control Register
0xAA	N.A.	read write	Send Renin to M.T. in test mode (bit0 of RCR must =1) Send LastPass in test mode (bit0 of RCR must =1)
0xAC	16	r only	Readout, Temperature Status Register (see sec
0xAE	16	r/w	Valack Timeout Register (multiple of 62.5 ns) (100 <t< 4 sec.) (active when bit2 of RCR is 1) e.g. to have 100 us timeout write the value 0x640 (1600).
0xB0	32	r only	Qstat1,Qstat0 counter (16 bit each). The Qstat1 counter is to count the number of event faults difference more than one. Qstat0 counter for the number of event faults. Qstat1 value in 16 MSB, Qstat0 value is in 16 LSB

0xB4to 0xBE	N.A.	r/w	Not yet Implemented

2.3.6.1 G.I.R. Readout Control Register (RCR): VME base Address : 0xA8

Bit Number	Meaning when = 0	Meaning when = 1
0	Run mode for SIROP readout	Test mode for SIROP readout
1	Run mode for External readout	Test mode for External readout
2	Disable Valack Timeout Reset	Enable Valack Timeout Reset
3	Enable Readout from G.I.R.	Disable Readout from G.I.R. (card is bypass)
4	Not yet defined	Not yet defined
5	no pipelining at all (dead until VXI Readout ends) LT_Reset asserted at the end of external Readout	Pipeline Readout stage (dead until data are in FIFO) (N.A.Y.) LT_Reset asserted at the end of internal Readout
6	Event Number Readout on	Event Number Readout off
7	Common Deadtime Readout mode (Eurogam I & II)	Euroball Readout mode
8	not used	not used
9	not used	not used
10	not used	not used
11	Use Event Number Q = 00 given by 0xa2 register	Use Event Number Q (qstat1,qstat0) (see sec 2.3.7.1.1)
12 TO 15	Not yet defined	Not yet defined

(N.A.Y.) (Not Available Yet)

2.3.6.1.1 G.I.R. Qstatus Table:

Qstat1:Qstat0	Meaning When Set
00	Trigger Broad cast nibble is equal to G.I.R. event counter Least Significant Nibble
01	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **more than one**
10	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **one**

2.3.6.2 G.I.R. Readout Status Register (*not fixed*): VME base Address : 0xAC

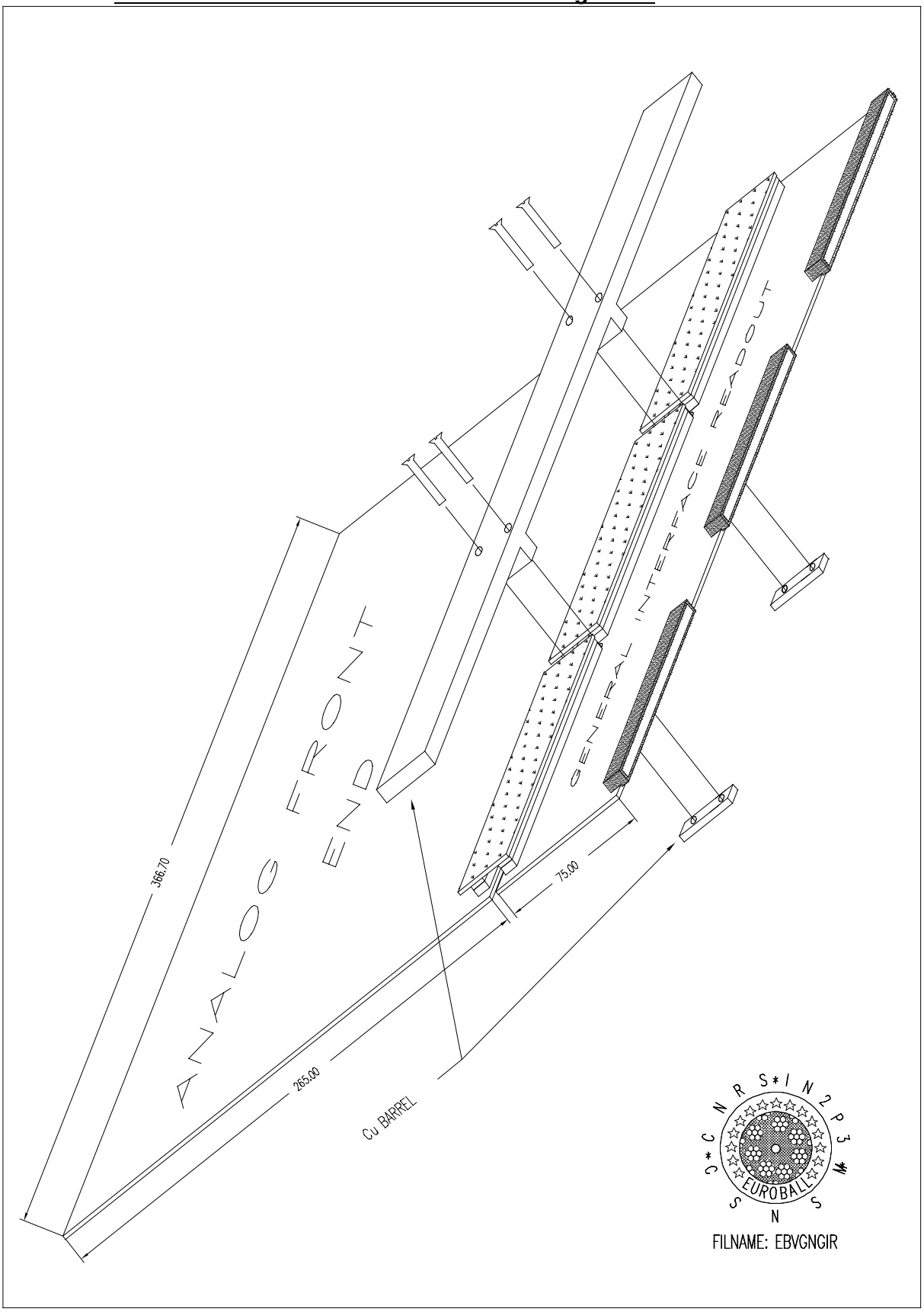
Bit Number	Meaning when = 0	Meaning when = 1
0	G.I.R. Temperature indicator is above the upper threshold	G.I.R. Temperature indicator is below the upper threshold
1	G.I.R. Temperature indicator is below the lower threshold	G.I.R. Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Valack Timeout deasserted	Valack Timeout asserted
7	Empty Flag of Fifo1 asserted	Empty Flag for Fifo1 deasserted
8	Full Flag of Fifo1 asserted	Full Flag for Fifo1 deasserted
9	NOT USED	NOT USED
10	NOT USED	NOT USED
11	NOT USED	NOT USED
12	NOT USED	NOT USED
13	Status: No fault	Status: Event fault 0
14	Status: No fault	Status: Event fault 1
15	Status: No fault	Status: Event fault 2

2.3.6.2.1 Event Fault Status:

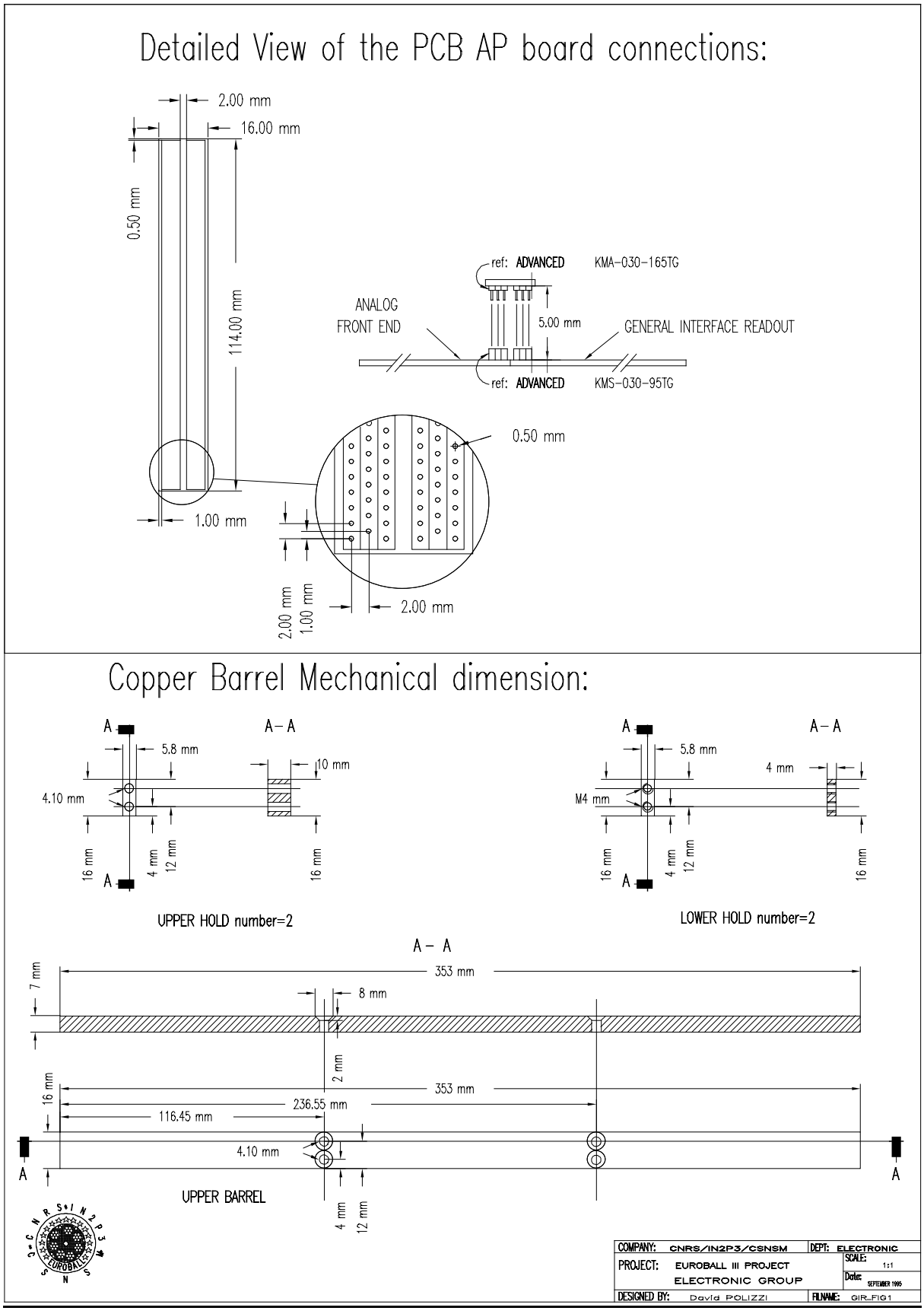
Event Fault Satus	Meaning When Set
Event Fault 0	local event number fails to match broadcast event number
Event Fault 1	Resynchronised by exactly 1 count (latched).
Event Fault 2	Resynchronised by more than 1 count (latched).

3. General Figures:

3.1. Isometric View of the G.I.R. & the Analog card:

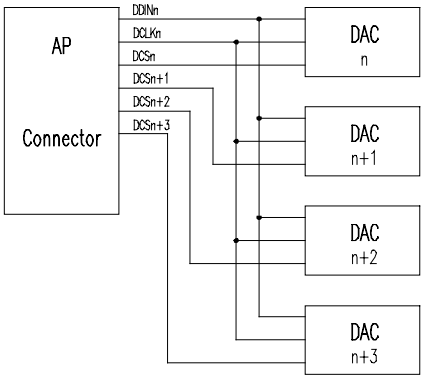


3.2. Copper Barrel Mechanical Dimensions,& PCB_AP board connections:

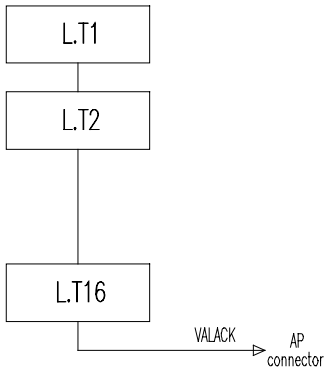


3.3. Master Trigger Dacs, Serial E²Prom, & Temperature Sensor connections figure :

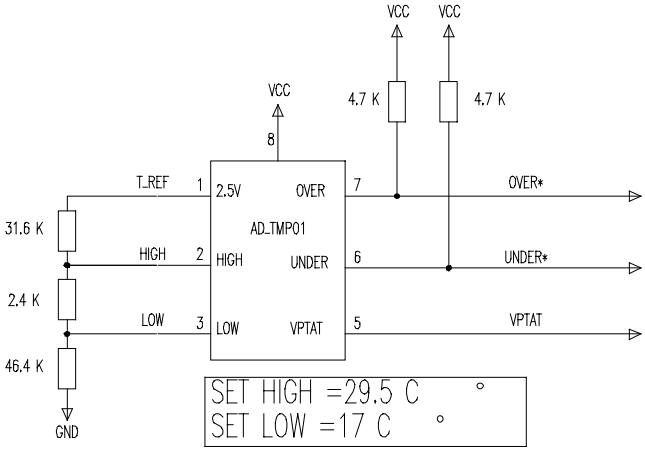
Dac connection figure:



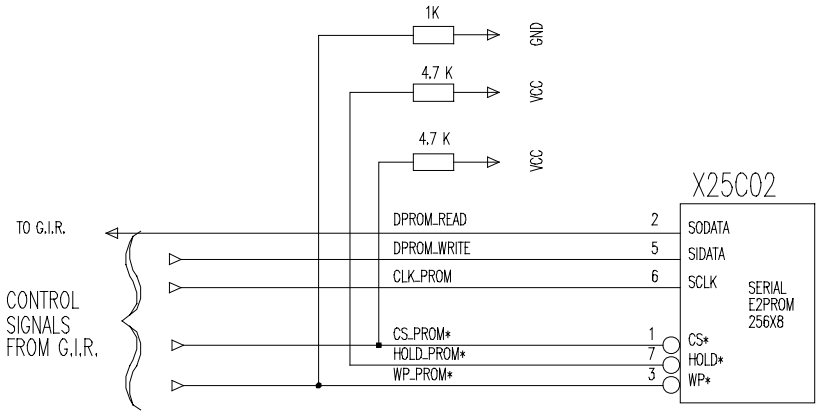
Valack L.T connection:



Temperature Sensor Connection Figure:



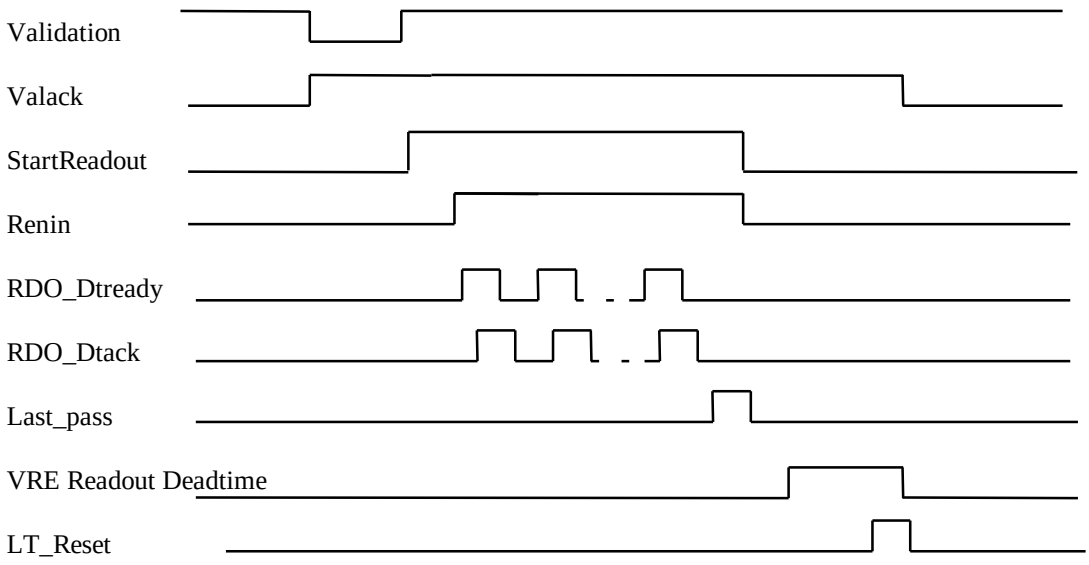
Serial E2Prom Connection Figure:



3.4. GIR power supply ratings on the AP connectors for the Analog card:

Voltage	Current +/-10%
- 2 V	8 A
+ 5 V	7 A
- 5.2 V	10 A
+ 12 V	2 A
- 12 V	2 A
+ 24 V	2 A
- 24 V	2 A

3.5. Readout Interface Timing Diagram between the Master Trigger, and the G.I.R.:



Note that in Pipeline Readout LT_Reset comes when Last_Pass comes, which is the same timing as the parallel mode unless the Master Trigger has a FIFO inside which handles several events before the readout into the G.I.R. of the current event. I think we must discuss in detail those problems to optimise the functioning of the Trigger, and to be the most reliable possible.