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SAPHIR Project

A.P. Description
& Memory Map
For
General Interface Readout

Version 1.0

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1. <u>AP Description.</u> This paragragh details the signals of **Table1**.

• 1.1) AP1 :

- DCLKn **:** Clock signal to load the *DAC*s, this signal is common for the 4 channels *n, n+1, n+2* and *n+3* (see fig. *Dacs connections*).

- DDINn **:** serial data signal to load the *DACs*, this signal is common for the 4 channels *n, n+1, n+2* and *n+3*(see fig. *Dacs connections*).

- DCSn **:** Chip Select signal to load the *DAC*s, there is one signal per *Dac*, n = 1 to 16 (see fig. *Dacs connections*).

- CLKProm: serial PROM Clock signal of the *SAPHIR Analog* card.

- CSProm : serial PROM Chip Select signal of the *SAPHIR Analog* card.

- DProm_Write: serial PROM Data write to the *SAPHIR Analog* card.

- DProm_Read: serial PROM Data to be read out of the *SAPHIR Analog* card.

(see E²Prom connection figure).

- CCRm **:** Channel Control Register, each signal enable or disable a function on each channel of the Analog part associeted with a **Latch** signal; *m* is the bit Register number. There are three registers of this type per channel :

0 ==> en/dis* external Linear Amp.
1 ==> en/dis* Test Generator.
2 ==> see below.
3 ==> pos/neg* PDS.

- LCCRn **:** Latch Signal for Channel Control Register; *n* is the channel number (1 to 16).

- CCR2n **:** Channel Control Register 2, each signal enable or disable each channel on the SAPHIR card; *n* is the channel number.

- ADD[7..1] : this is the lowest byte of the *VME* Address bus, it is enabled by the *LCA DECOD1*.

- Spare : these signals are not used in the *Euroball* SAPHIR card, they are controlled by the *LCA DECOD1*. They can be used by the *Analog* card for future applications.

- VPTAT1 : Voltage Proportional To Absolute Temperature signal of the sensor 1 from the *Analog* card and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER1 : high level temperature signal of the sensor 1 from the *Analog* card.

- UNDER1 : low level temperature signal of the sensor 1 from the *Analog* card.

- LED Temp: display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel for the temperature Alarm. Color : **RED**.

• 1.2) AP2 :

- SIROPCSn **:** SIROP Chip Select signal for the configuration of the *SIROPs* in the *SAPHIR* card, n is the *SIROP* number (n = 1 to 2).

- 16 MHz: buffered *VME* System Clock signal (not used).

- SIROP-DACWstrb: Write Strobe signal for the configuration of the *SIROPs* and the *General DAC*.

- Reject/Mark*: either mark or reject the prepileup event, common register on the *Analog* card.

- TEST-GEN: en/dis* Test Generator activity, common register on the *Analog* card.

- WP_Prom: en/dis*Enable or disable the write protection on the Identification serial prom.

- CS_DAC_Gene: Chip select of the DAC Test generator, which is latched with the SIROP-DACWstrb.

- ADD[23..8] : these are the other 2 bytes of the *VME* Address bus, they are enabled by the *LCA DECOD1*.

- AIn **:** Analogue Inspection Lines, n is the inspection line indicator.

- DIn **:** Digital Inspection Lines, n is the inspection line indicator. If the lignes are inactive, the level **MUST BE 0 logic** *ECL*. These signals **MUST NOT BE LOADED** by a charge resistor.

- VI : Voltage Inspection Line.

- DATA[15..0] : these are the lower sixteen bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SIROP* and *FIFO* data bus during Readout mechanism.

- EVT_IN[3..0] : these lines are the current event number, they are given by the *MASTER Trigger* via the *VXI Local* bus to the Analog cards with *Validation* (LBus [11..8]). They **must be latched** by *SAPHIR* card.

- SIROPDtreadyn **:** data ready given by the *SIROPs* when a data is ready to be latched in the *FIFO*, n is the *SIROP* number.

- OVER 3 : high level temperature signal of the sensor 3 from the *Analog* card.

- UNDER 3 : low level temperature signal of the sensor 3 from the *Analog* card.

- SIROP 1 L1, 2 : Digital Inspection Line Signals of the SIROP1, which are connected to the G.I.R. digital multiplexer. These signals show the internal logic function of the SIROP1.

- SIROPDTack_buf : buffered data acknowledge signal for each data word of the *SIROP* in a Readout cycle, common for all the *SIROPs*.

- Renin : start Readout cycle of the *SIROP*, this signal is sent to the first *SIROP*.

- RESET_A_buf : buffered Reset signal of the *Analog* card (acquisition) of the *SIROP*.

- LPASS : Last PASS, this is the renout signal of the last *SIROP* for the internal Readout mode.

- GLOBAL RESET : buffered global Reset signal of all the *Analog* card, connected to the *SIROP*.

- R/W_buf : buffered *VME* read-write signal, connected to the *SIROP*.

- ORVALACK : this signal is the *VALACKOUT* of the *Daisy chained Local Trigger* (see *Valack* fig).

- StartReadoutSirop : This signal latches the *ADC* data in the *SIROP* internal registers after coding, the back edge of this signal starts the internal Readout cycle.

- LT_Reset : buffered Reset signal for the *Local Trigger*.

- Coding : This is the coding dead time signal, which indicates that the *ADCs* are coding, and no *VME* Action must take place. This signal goes to the *MASTER Trigger* as an open collector at the Back plane.

- 25 MHz: *SIROP* Clock signal.

- Read Spare : these signals are dedicated for Readout interface and are not used in the *Euroball SAPHIR* card, they are controlled by the *LCA READOUT*. They can be defined for future applications.

- Spare : these signals are not used in the *Euroball* SAPHIR card, they are controlled by the *LCA DECODE2*. They can be defined for future applications.

- VPTAT2 : Voltage Proportional To Absolute Temperature signal of the sensor 2 from the Analog part and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER2 : high level temperature signal of the sensor 2 from the *Analog* card.

- UNDER2 : low level temperature signal of the sensor 2 from the *Analog* card.

- FIFO-ERROR : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel It indicates the FIFO Event Error. Color : **RED**. **(see the connection of the Led in Led connection figure!)**.

• 1.3) AP3 :

- DATA[31..16] : these are the sixteen higher bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SAROC* and *FIFO* data bus during Readout.

- EVT_out[3..0] : these lines are the event number that are sent with the *ADCs* data during acquisition, and are written into the *FIFO*.

- FT_ttl_buf : buffered *Fast Trigger* signal (positive TTL) from the *MASTER Trigger* (*starx* on the *VXI* back plane).

- Inhibit_buf : buffered *Inhibit* signal from the *MASTER Trigger* (on the *VXI* back plane).

- VAL_buf : buffered *Validation* signal from the *MASTER Trigger* (on the *VXI* back plane).

- SIROP 2 L1, 2 : Digital Inspection Line Signals of the SIROP2, which are connected to the G.I.R. digital multiplexer. These signals show the internal logic function of the SIROP2.

- LC1, 2 : Common Signals to be displayed on the Digital Inspection Lines (Or in & Or out of the *Trigger* logic on the card).

- FT_ECL -, FT_ECL+ : *Fast Trigger signals* (differential ECL) given by the *MASTER Trigger* (*starx* +/- on the *VXI* back plane). **These signals are not charged, the resistors MUST be placed on the Analog part.** (not used by *SAPHIR* card).

- DSPFLAG1, 2, 3 : these signals are not used for the moment in *Euroball*. They can be used later as a connection between the *DSP*, and the *Analog* card. They are controlled by the *DSP*.

- DONE-LED : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel This signal indicates that the G.I.R. LCAs are fully programmed, or Done LCAs is all High. Color: **GREEN (see the connection of the Led in Led connection figure!)**.

All the signals below are controlled by the *LCA DECODE2*.

- Vstrobe: load signal of all the voltage multiplexers.

- Anastrobe: load signal of all the Analog multiplexers.

- AnaSelAn **:** select signal of the Analog multiplexers for the Analog Inspection Line 1, *n* is the multiplexer select bit (n = 0 to 3)(the multiplexers are the same which are used in *Eurogam* and are *TTL* input compatible).

- AnaSelBn **:** select signal of the Analog multiplexers for the Analog Inspection Line 2, *n* is the multiplexer select bit (n = 0 to 3).

- AnEnAn **:** enable signal of the Analog multiplexers for the Analog Inspection Line 1. There is one per multiplexer (5 are used for the SAPHIR card).

- AnEnBn **:** enable signal of the Analog multiplexers for the Analog Inspection Line 2. there is one per multiplexer (5 are used for the SAPHIR card).

- DigSelAn **:** select signal of the digital multiplexers for the digital inspection line 1, *n* is the multiplexer select bit (n = 0 to 3).

- DigSelBn **:** select signal of the digital multiplexers for the digital inspection line 2, *n* is the multiplexer select bit (n = 0 to 3).

- DigOeAn **:** output enable signal of the Digital multiplexers for the Digital Inspection Line 1. there is one per multiplexer (8 are used for the SAPHIR card).

- DigOeBn **:** output enable signal of the Digital multiplexers for the Digital Inspection Line 2. there is one per multiplexer (8 are used for the SAPHIR card).

- VSel[3..0] : select bus of the voltage multiplexers. These signals must be common to all voltage multiplexers.

- Venablen **:** enable signal of the voltage multiplexers, 9 for SAPHIR card.

Pinouts of the AP Connector for the SAPHIR Card: (Table 1):

	AP1 Connector			AP2 Connector			AP3 Connector			
PIN NO.	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	PIN NO.
1	+5 V	Ana-Spare	+5 V	+5 V	Ana-Spare	+5 V	+5v	DSPFLAG1	+5v	1
2	+5 V	+5 V	+5 V	+5 V	+5v	+5 V	+5v	+5v	+5v	2
3	DCLK 1	OVER1	DDIN 1	SIROPCS1	OVER2	SIROPCS2	DATA 16	DSPFLAG2	DATA 17	3
4	DCS 1	UNDER1	DCS 2	Reject/Mark*	UNDER2	TEST-GEN	DATA 18	DSPFLAG3	DATA 19	4
5	DCS 3	LED Temp	DCS 4	WP-PROM	FIFO-ERR	CS_DAC_Gene	DATA 20	DONE-LED	DATA 21	5
6	DCLK 5	GND	DDIN 5	16 Mhz	GND	SIROP-DAC-Wstrb	DATA 22	GND	DATA 23	6
7	DCS 5	GND	DCS 6	GND	GND	AnAstrobe	GND	GND	GND	7
8	DCS 7	GND	DCS 8	ADD 8	GND	ADD 9	DATA 24	GND	DATA 25	8
9	DCLK 9	GND	DDIN 9	ADD 10	GND	ADD 11	DATA 26	GND	DATA 27	9
10	DCS 9	GND	DCS 10	ADD 12	GND	ADD 13	DATA 28	GND	DATA 29	10
11	DCS 11	GND	DCS 12	ADD 14	GND	ADD 15	DATA 30	GND	DATA 31	11
12	DCLK 13	GND	DDIN 13	ADD 16	GND	ADD 17	GND	GND	GND	12
13	DCS 13	GND	DCS 14	ADD 18	GND	ADD 19	EVT_out0	GND	EVT_out1	13
14	DCS 15	GND	DCS 16	ADD 20	GND	ADD 21	EVT_out2	GND	EVT_out3	14
15	CCR 0	GND	CCR 1	ADD 22	GND	ADD 23	SIROP2 L1	GND	SIROP2 L2	15
16	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	16
17	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	17
18	CCR 2	GND	CCR 3	Vstrobe	GND	AnASelA 0	LC 1(Or In)	GND	LC 2(Or Out)	18
19	LCCR 1	GND	LCCR 2	AnASelA 1	GND	AnASelA 2	FT_ECL +	GND	Read Spare	19
20	LCCR 3	GND	LCCR 4	AI 1	GND	GND	GND	GND	FT_ECL -	20
21	Clk Prom	GND	DProm_Write	GND	GND	GND	FT_ttl_buf	GND	Inhibit_buf	21
22	CS Prom	GND	DProm_Read	AI 2	GND	GND	VAL_buf	GND	AnASelB 2	22
23	LCCR 5	GND	LCCR 6	GND	GND	DI 1	AnASelB 3	GND	AnEnA 1	23
24	LCCR 7	GND	LCCR 8	DI 2	GND	GND	AnEnA 2	GND	AnEnA 3	24
25	LCCR 9	GND	LCCR 10	AnASelA 3	GND	VI	AnEnA 4	GND	AnEnA 5	25
26	LCCR 11	GND	LCCR 12	AnASelB 0	GND	AnASelB 1	AnEnB 1	GND	AnEnB 2	26
27	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	27
28	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	28
29	LCCR 13	GND	LCCR 14	DATA 0	GND	DATA 1	AnEnB 3	GND	AnEnB 4	29
30	LCCR 15	GND	LCCR 16	DATA 2	GND	DATA 3	AnEnB 5	GND	DigSelA 0	30
31	CCR2 1	GND	CCR2 2	DATA 4	GND	DATA 5	DigSelA 1	GND	DigSelA 2	31
32	CCR2 3	GND	CCR2 4	DATA 6	GND	DATA 7	DigSelA 3	GND	DigSelB 0	32
33	CCR2 5	GND	CCR2 6	GND	GND	GND	DigSelB 1	GND	DigSelB 2	33
34	CCR2 7	GND	CCR2 8	DATA 8	GND	DATA 9	DigSelB 3	GND	DigOeA 1	34
35	CCR2 9	GND	CCR2 10	DATA 10	GND	DATA 11	DigOeA 2	GND	DigOeA 3	35
36	CCR2 11	GND	CCR2 12	DATA 12	GND	DATA 13	DigOeA 4	GND	DigOeA 5	36
37	CCR2 13	GND	CCR2 14	DATA 14	GND	DATA 15	DigOeA 6	GND	DigOeA 7	37
38	CCR2 15	GND	CCR2 16	EVT_IN0	GND	EVT_IN1	DigOeA 8	GND	DigOeB 1	38
39	CCR2 17	GND	Spare	EVT_IN2	GND	EVT_IN3	DigOeB 2	GND	DigOeB 3	39
40	Spare	GND	Spare	SiropDtready 1	GND	SiropDtready 2	DigOeB 4	GND	DigOeB 5	40
41	Spare	GND	Spare	OVER3	GND	UNDER 3	DigOeB 6	GND	DigOeB 7	41
42	Spare	GND	Spare	SIROP1 L1	GND	SIROP1 L2	DigOeB 8	GND	VSel 0	42
43	Spare	GND	Spare	SIROPDtack	GND	Renin	VSel 1	GND	Vsel 2	43
44	Spare	GND	Spare	RESET A_buf	GND	LPASS	Vsel 3	GND	Venable 1	44
45	Spare	GND	Spare	GlobalReset	GND	R/W_buf	Venable 2	GND	Venable 3	45
46	ADD 2	GND	ADD 3	ORVALACK	GND	StartReadoutSirop	Venable 4	GND	Venable 5	46
47	ADD 4	GND	ADD 5	LT_Reset	GND	Read Spare	Venable 6	GND	Venable 7	47
48	ADD 6	GND	ADD 7	Clk 25MHz	GND	Coding	Venable 8	GND	Venable 9	48
49	+5 V	GND	+5 V	+5 V	GND	+5 V	+5 V	GND	+5 V	49
50	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	50
51	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	51
52	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	52
53	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	53
54	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	54
55	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	55
56	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	56

2 Memory Map of the G.I.R. for the Saphir Card

2.1 VXI Configuration Registers: (Inside the G.I.R.)

⌦ *will be modified by GaD : waiting for institute identifier to replace IN2P3*

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11).

VXI Base Address (slot 1)	*Description*	*DATA Format*
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8a	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

2.2 Channel Area Addresses

Channel 1 (0x1000 --0x10FE)	**Bus Width**	**Read/ Write**	**Function**
0x1000	16	w	Dac Adjustment no.1 (see Dac Memory Map below)
0x1010	16	r/w	Channel Control Register 4 bits bit0 = external /internal* amplifier, bit1 = enable/disable* test generator, bit2 = disable/ enable* channel . bit3 = Inverseur de l'ampli vers le PDS.
Channel 2 (0x1100 --0x11FE)	**16**	**r/w**	**Function**
0x1100	16	w	Dac Adjustment no.2 (see Dac Memory Map below)
0x1110	16	r/w	Channel Control Register 3 bits
Channel 16 (0x1f00 --0x1fFE)	**16**	**(r/w)**	**Function**
0x1F00	16	w	Dac Adjustment no.16 (see Dac Memory Map below)
0x1F10	16	r/w	Channel Control Register 3 bits

2.2.1 DAC Memory Map:

This applies to all channel DAC set-up for Address 0x1000 to 0x100a (channel 1) up to (channel 16).

Channel 1 Dacs (0x1000..0x100a)	**DAC A/B**	**G.I.R. DAC parameter Value**	**DAC Parameter Name**
0x1000	?	?	S1 : CFD Output Delay (Seuil R) Channel 1
0x1002	?	?	S2 : CFD Threshold (Seuil bas) Channel 1
0x1004	?	?	S3 : CFD Output DELAY+WIDTH (seuil R+D) Channel 1
0x1006	?	?	S4 :Validation Sample Delay (Ret Val Sample) Channel 1
0x1008	?	?	S5 : FT Sample Delay (Ret F.T Sample) Channel 1
0x100a	?	?	S6 : PDS Gate Width (PDS GATE TH) Channel 1
Channel 2 Dacs (0x1100 --0x110a)			
Channel 3 Dacs (0x1200 --0x120a)			
Channel 4 Dacs (0x1300 --0x130a)			
...			
Channel 16 Dacs (0x1f00 --0x1f0a)			

2.2.2 DAC Memory Map: (A VOIR)

⌦ *will be modified by Nab or other hardware specialist . SEE Alain* ***FOR DESTROY ??????***

This Table shows the hardware parameter's list of the DACs parameters w.r.t. their effective position.

Channel 1 (0x1000 --0x10FE)	DAC A/B	G.I.R. DAC parameter Value	DAC Parameter Name

2.3 Common Area Addresses

2.3.1 Common DACs:

VME Address	Bus Width	R/W	Function
0x0	16	w	Test Generator amplitude adjustment

2.3.2 Common Registers:

Global Addresses	Bus Width	Read/ Write	Function
0x10	16	r/w	Module Control Register (MCR)
0x20	16	r/w	Digital Inspection 1 channel select
0x22	16	r/w	Digital Inspection 1 parameter Select
0x24	16	r/w	Digital Inspection 2 channel select
0x26	16	r/w	Digital Inspection 2 parameter Select
0x28	16	r/w	Analog Inspection 1 channel select
0x2A	16	r/w	Analog Inspection 1 parameter Select
0x2C	16	r/w	Analog Inspection 2 channel select
0x2E	16	r/w	Analog Inspection 2 parameter Select
0x30	16	r/w	Voltage Inspection channel select
0x32	16	r/w	Voltage Inspection parameter Select
0x40--0x5E	16	r only	Read Default DAC Buffer values from XCProm
0x60--0x7E	16	w only	Set Default DAC Buffer Values in XCPROM for non volatile mode
0x80--0x90	16	w only	Change Default DAC Buffer Set-up in Volatile mode
0xA0--0xBE	16/32	r/w	Readout Set-up
0x100--0x17C	32	r/w	Sirop 1 Set-up
0x180-0x1FC	32	r/w	Sirop 2 Set-up

2.3.2.1 Module Control Register: VME base Address : 0x10 **a verifier avec Nab**

→→→ modified by GaD : WARNING bit 0 is used to mark or reject .   New   New   New

Bit Number	Meaning when = 0	Meaning when = 1
0	***Mark Pre-Pileup***	***Reject Pre-Pileup***
1	Test generator Disable	Test generator Enable
2	Not Allocated	Not Allocated
3	Not Allocated	Not Allocated
4	Prom Write Protect Disable	Prom write Protect Enable
5	Not Allocated	Not Allocated
6	Not Allocated	Not Allocated
7	Not Allocated	Not Allocated
8	Reset FIFO Disable	Reset FIFO
9	Reset G.I.R. Disable	G.I.R. Reset
10	Not Last Card	Last Card (use terminators)
11 TO 15	Not Allocated	Not Allocated

2.3.2.2 Digital inspection lines:

Digital Inspection line 1 : VME base Address : 0x20 (channel Select), and 0x22 (parameter Select)
To Disable the Digital inspection Line 1 write 0x00 at address 0x20.
Digital Inspection line 2 : VME base Address : 0x24 (channel Select), and 0x26(parameter Select).
To Disable the Digital inspection Line 2 write 0x00 at address 0x24.

parameters Line1 =DIGSELA [3..0] & DIGOEA [8..1] Line2 =DIGSELB[3..0] & DIGOEB [8..1]	GIR Control Lines to Analogue Card DIGSELx [3..0]	GIR Control Lines to Analogue Card DIGOEx [8..1]	Data Value for channel Address	Data Value for Parameter Address
Disable	xx	**0x0**	0x00	xx
CFD Direct 1	0x0	0x1	0x01	0x00
CFD Delayed 1	0x1	0x1	0x01	0x01
TAC Start 1	0x2	0x1	0x01	0x02
TAC+PDS Reset 1	0x3	0x1	0x01	0x03
Encode Command 1	0x4	0x1	0x01	0x04
PDS Gate 1	0x5	0x1	0x01	0x05
FT sample 1	0x6	0x1	0x01	0x06
Val sample 1	0x7	0x1	0x01	0x07
CFD Direct 2	0x8	0x1	0x02	0x00
CFD Delayed 2	0x9	0x1	0x02	0x01
TAC Start 2	0xA	0x1	0x02	0x02
TAC+PDS Reset 2	0xB	0x1	0x02	0x03
Encode Command 2	0xC	0x1	0x02	0x04
PDS Gate 2	0xD	0x1	0x02	0x05
FT sample 2	0xE	0x1	0x02	0x06
Val sample 2	0xF	0x1	0x02	0x07
Channel 3 & 4 same values	see above	0x2	0x03 to 0x04	see above
Channel 5 & 6 same values	see above	0x4	0x05 to 0x06	see above
Channel 15 & 16 same values	see above	0x80	0x0F to 0x10	see above
Not Used all Chan(Disable)		0x0	0x11 to 0x1F	

G.I.R. Global Parameters	GIR Control Lines	channel Data Value	Parameter Data Value
Disable		*0x20*	*0x000*
Fast_Trigger	0x001	0x20	0x001
Inhibit_buf (M.T.)	0x002	0x20	0x002
Validation	0x003	0x20	0x003
Veto	0x004	0x20	0x004
OrValack	0x005	0x20	0x005
Conversion DTime (coding)	0x006	0x20	0x006
StartReadoutSIROP	0x007	0x20	0x007
Renin (SIROP)	0x008	0x20	0x008
SIROPDTready0	0x009	0x20	0x009
SIROPDTready1	0x00A	0x20	0x00A
OR8CFD-Delay	0x00B	0x20	0x00B
Inhibit Card	0x00C	0x20	0x00C
SIROPDTack_buf	0x00D	0x20	0x00D
SIROPEmpty0	0x00E	0x20	0x00E
SIROPEmpty1	0x00F	0x20	0x00F
Readout Event Fault	0x010	0x20	0x010
Readout Event Match	0x011	0x20	0x011
SIROPLPASS	0x012	0x20	0x012
CSA *(FifoChipSelect_A)	0x013	0x20	0x013

CLKA(FifoClock_A)	0x014	0x20	0x014
ENA(Fifo Enable Port_A)	0x015	0x20	0x015
AS* (VME)	0x016	0x20	0x016
DS (DS0* and DS1*) (VME)	0x017	0x20	0x017
R/W* (VME)	0x018	0x20	0x018
ModRoco	0x019	0x20	0x019
CardRenin *(From ROCO)	0x01A	0x20	0x01A
BLTACK (Card)	0x01B	0x20	0x01B
BLTACK (Bus)	0x01C	0x20	0x01C
OE_Ident*	0x01D	0x20	0x01D
CSB* (FifoChipSelect_B)	0x01E	0x20	0x01E
CLKB (FifoClock_B)	0x01F	0x20	0x01F
ENB (Fifo Enable Port_B)	0x020	0x20	0x020
OR_fifo (EmptyFlag)	0x021	0x20	0x021
FDTACK	0x022	0x20	0x022
DTACK* (VME)	0x023	0x20	0x023
CardRenout(Bus Renout)	0x024	0x20	0x024
SysClk	0x025	0x20	0x025
LT_Reset*	0x026	0x20	0x026
Oe_Global	0x027	0x20	0x027
Reset_Fifo*	0x028	0x20	0x028
DecodeSel(CardChipSelect)	0x029	0x20	0x029
Strobe_Dec2	0x02A	0x20	0x02A
Dclk	0x02B	0x20	0x02B
DCS*	0x02C	0x20	0x02C
DDin	0x02D	0x20	0x02D
Coding_Bus	0x02E	0x20	0x02E
ExternalReset_ LT	0x02F	0x20	0x02F
Readout Event Fault more than 1	0x030	0x20	0x030
Spare2	0x031	0x20	0x031
Vme Address 1	0x032	0x20	0x032
Vme Address 2	0x033	0x20	0x033
Vme Address 3	0x034	0x20	0x034
Vme Address 4	0x035	0x20	0x035
Vme Address 5	0x036	0x20	0x036
Not Used (DI Disable)	Disable	valus not = 0x20	xxxx

2.3.2.3 Analog inspection lines:

Analog Inspection line 1 : VME base Address: 0x28 (channel Select), & 0x2A (parameter Select).
To Disable the Analog inspection Line 1 write 0x00 at address 0x28.
Analog Inspection line 2 : VME base Address : 0x2C (channel Select), and 0x2E (parameter Select).
To Disable the Analog inspection Line 2 write 0x00 at address 0x2C.

→→→ modified by GaD . ?
⌦ will be modified by Nab or other hardware specialist .

Parameters for channel 1, 2,3 &4. Channel 5to 16 are coupled by 4.	GIR Control Lines to Analogue Card AI 1 :AnaSelA [3..0] AI 2 :AnaSelB [3..0]	GIR Control Lines to Analogue Card AI 1: AnaEnA[5..1] AI 2: AnaEnB[5..1]	Data Value for channel Address	Data Value for Parameter Address
Disable	**xx**	**0**	***0x00***	**xx**
Input 1	0x0	0 0001	0x01	00
TFA Ouput 1	0x1	0 0001	0x01	01
LA Ouput 1	0x2	0 0001	0x01	02
PDS output 1	0x3	0 0001	0x01	03
TAC output 1	0x0	1 0000	0x01	04
Input 2	0x4	0 0001	0x02	00
TFA Ouput 2	0x5	0 0001	0x02	01
LA Ouput 2	0x6	0 0001	0x02	02
PDS output 2	0x7	0 0001	0x02	03
TAC output 2	0x1	1 0000	0x02	04
Input 3	0x8	0 0001	0x03	00
TFA Ouput 3	0x9	0 0001	0x03	01
LA Ouput 3	0xA	0 0001	0x03	02
PDS output 3	0xB	0 0001	0x03	03
TAC output 3	0x2	1 0000	0x03	04
Input 4	0xC	0 0001	0x04	00
TFA Ouput 4	0xD	0 0001	0x04	01
LA Ouput 4	0xE	0 0001	0x04	02
PDS output 4	0xF	0 0001	0x04	03
TAC output 4	0x3	1 0000	0x04	04
Not used(Disable) 1 & 2	XXX	0 0000	xxxx	08 to FF
Channel 5 to 8 same values	see above	0 0010 Except TAC (see above)	0x05 to 0x08	see above
Channel 9 to 12 same values	see above	0 0100 Except TAC (see above)	0x09 to 0x0C	see above
Channel 13 to 16 same values	see above	0 1000 Except TAC (see above)	0x0D to 0x10	see above
Not used(Disable) 1 & 2	XXX	0 0000	xxxx	08 to FF

2.3.2.4 Voltage inspection line:

VME base Address : 0x30 (channel select), and 0x32 (parameter select).
To Disable the Voltage Inspection line : write 0x00 at address 0x30.

→→→ remodified by DLi . ?
⌦ will be checked by Nab and other hardware specialist .

parameters	GIR Control Lines to Analogue Card VSel [3..0]	GIR Control Lines to Analogue Card Venable[9..1]	Data Value for Channel Address	Data Value for Parameter Address
Disable	**xx**	**0**	***0x00***	**xx**
CFD Output Delay 1 S1 : (Seuil R)	0000	000000001	0x01	00
CFD Threshold 1 S2 : (Seuil bas)	0001	000000001	0x01	01
CFD Output Delay+Width 1 S3 : (seuil R+D)	0010	000000001	0x01	02
Validation Sample delay 1 S4 : (Ret Val Sample)	0011	000000001	0X01	03
FT Sample delay 1 S5 : (Ret F.T. Sample)	0100	000000001	0X01	04
PDS Gate width 1 S6 : (PDS GATE TH)	0101	000000001	0X01	05
CFD Output Delay 2 S1 : (Seuil R)	1000	000000001	0x2	00

CFD Threshold 2 S2 : (Seuil bas)	1001	000000001	0x2	01
CFD Output Delay+Width 2 S3 : (seuil R+D)	1010	000000001	0x2	02
Validation Sample delay 2 S4 : (Ret Val Sample)	1011	000000001	0x2	03
FT Sample delay 2 S5 : (Ret F.T. Sample)	1100	000000001	0x2	04
PDS Gate width 2 S6 : (PDS GATE TH)	1101	000000001	0x2	05
Not used (Disable) 1 & 2	xxxx	000000001	xxxx	xxxx
Channel 3 & 4 Same Values **Channel 5 & 6 Same Values** **Channel 7 & 8 Same Values**	See upper See upper See upper	000000010 000000100 000001000	0x03 to 0x04 0x05 to 0x06 0x07 to 0x08	See upper See upper See upper
Channel 9 & 10 Same Values **Channel 11 & 12 Same Values** **Channel 13 & 14 Same Values**	See upper See upper See upper	000010000 000100000 001000000	0x09 to 0x0a 0x0b to 0x0c 0x0d to 0x0e	See upper See upper See upper
Channel 15 & 16 Same Values	See upper	010000000	0x0f to 0x10	See upper
tension +5v	0000	100000000	0x20	0x00
tension -5.2v	0001	100000000	0x20	0x01
tension +12v	0010	100000000	0x20	0x02
tension -12v	0011	100000000	0x20	0x03
tension +24v	0100	100000000	0x20	0x04
tension -24v	0101	100000000	0x20	0x05
tension -2v	0110	100000000	0x20	0x06
tension +20v	0111	100000000	0x20	0x07
REFH 1 (references internes DAC)	1000	100000000	0x20	0x08

2.3.2.5 Saphir Configuration Registers (Analogue part):

⌦ *will be modified later..................*

VXI Base Address	*Description*	*DATA Format*
0x40	In Read Mode this is the Man. ID	D7..D0 from XCPROM ⌦ ***code CEA***
0x42		
0x44		
0x46		
0x48	Read Only: Serial no.	Read 8 bits only from XCPROM d7 to d0
0x4a	Read Only: Modification Level	Read 8 bits only from XCPROM d7 to d0

2.3.2.6 Saphir DAC Buffer Control Memory Map (non volatile):

⌦ *will be modified later..................*

Base Addresses	Bus Width	Read/ Write	Function
0x60	16	r/w	Default DAC Buffer **1** values from XCProm
0x62	16	r/w	Default DAC Buffer **2** values from XCProm
0x64	16	r/w	Default DAC Buffer **3** values from XCProm
0x66	16	r/w	Default DAC Buffer **4** values from XCProm
0x68	16	r/w	Default DAC Buffer **5** values from XCProm
0x6A	16	r/w	Default DAC Buffer **6** values from XCProm
0x7E	16	r/w	Default DAC Buffer **16** values from XCProm

2.3.2.7 Saphir DAC Buffer Setup Memory Map (volatile):

⌦ *will be modified later.................. ?*

Base Addresses	Bus Width	Read/ Write	Function
0x80	16	write only	Change Default DAC Buffer **1** mode in XCProm
0x82	16	write only	Change Default DAC Buffer **2** mode in XCProm
0x84	16	write only	Change Default DAC Buffer **3** mode in XCProm
0x86	16	write only	Change Default DAC Buffer **4** mode in XCProm
0x88	16	write only	Change Default DAC Buffer **5** mode in XCProm
0x8A	16	write only	Change Default DAC Buffer **6** mode in XCProm
0x9E	16	write only	Change Default DAC Buffer **16** mode in XCProm

2.3.2.8 G.I.R. Readout Memory Map : VME base Address : 0xA0 to 0xBE.

Base Addresses	Bus Width	Read/ Write	Function
0xA0	16	r/w	Event Counter Register

0xA2	16	r/w	Item + Group no. Register
0xA0	32	read only	Item + Group no. + Event Counter
0xA4	32	r/w	Fifo Test Access
0xA8	16	r/w	G.I.R. Readout Control Register
0xAA	N.A.	r only w only	Start Readout SIROP in test mode End Readout SIROP in test mode
0xAC	16	r only	Readout, Temperature Status Register
0xAE	16	r/w	Valack Timeout Register (multiple of 62.5 ns) (100 <t< 4 sec.) (active when bit2 of RCR is 1) e.g. to have 100 us timeout write the value 0x640 (1600).
0xB0	32	r only	Qstat1,Qstat0 counter (16 bit each). The Qstat1 counter is to count the number of event faults difference more than one. Qstat0 counter for the number of event faults. Qstat1 value in 16 MSB, Qstat0 value is in 16 LSB
0xB4to 0xBE	N.A.	r/w	Not yet Implemented

2.3.2.8.1 G.I.R. Readout Control Register (RCR) (*not fixed*):

VME base Address : 0xA8 to be upgraded

Bit Number	Meaning when = 0	Meaning when = 1
0	Run mode for SIROP readout	Test mode for SIROP readout
1	Run mode for External readout	Test mode for External readout
2	Disable Valack Timeout Reset	Enable Valack Timeout Reset
3	Enable Readout from G.I.R.	Disable Readout from G.I.R. (card is bypass)
4	Not yet defined	Not yet defined
5	no pipelining at all (dead until VXI Readout ends)	Pipeline Readout stage (dead until data are in FIFO) (N.A.Y.)
6	Event Number Readout off	Event Number Readout on
7	Common Deadtime Readout mode (Eurogam I & II)	Euroball Readout mode
8	DSP set to Slave Mode (N.A.Y.)	DSP set to Master Mode(N.A.Y.)
9	DSP Slave is not last Slave Card(N.A.Y.)	DSP Slave is the last Slave Card(N.A.Y.)
10	Contrôle des fenêtres off(N.A.Y.)	Contrôle des fenêtres on(N.A.Y.)
11	Use Event Number Q = 00 given by 0xa2 register	Use Event Number Q (qstat1,qstat0) (see table below)
12 TO 15	Not yet defined	Not yet defined

(N.A.Y.) (Not Available Yet)

2.3.2.8.1.1 G.I.R. Qstatus Table:

Qstat1:Qstat0	Meaning When Set
00	Trigger Broad cast nibble is equal to G.I.R. event counter Least Significant Nibble
01	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **more than one**
10	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **one**

2.3.2.8.2 G.I.R. Readout Status Register (*not fixed*): VME base Address : 0xAC

→→→ *modified by GaD : WARNING ,some bits have been moved in order to have a temperature BYTE*

Bit Number	Meaning when = 0	Meaning when = 1
0	G.I.R. Temperature indicator is above the upper threshold	G.I.R. Temperature indicator is below the upper threshold
1	G.I.R. Temperature indicator is below the lower threshold	G.I.R. Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Temperature indicator 3 is above the upper threshold	
7	Temperature indicator 3 is below the lower threshold	
8	Valack Timeout deasserted	Valack Timeout asserted
9	Empty Flag of Fifo1 asserted	Empty Flag for Fifo1 deasserted
10	Full Flag of Fifo1 asserted	Full Flag for Fifo1 deasserted
11	Global SIROP_Empty asserted	Global SIROP_Empty deasserted
12(Unused)		
13	Status: No fault	Status: Event fault 0
14	Status: No fault	Status: Event fault 1
15	Status: No fault	Status: Event fault 2

Event Fault 0 = local event number fails to match broadcast event number.
Event Fault 1 = Resynchronised by exactly 1 count (latched).
Event Fault 2 = Resynchronised by more than 1 count (latched).

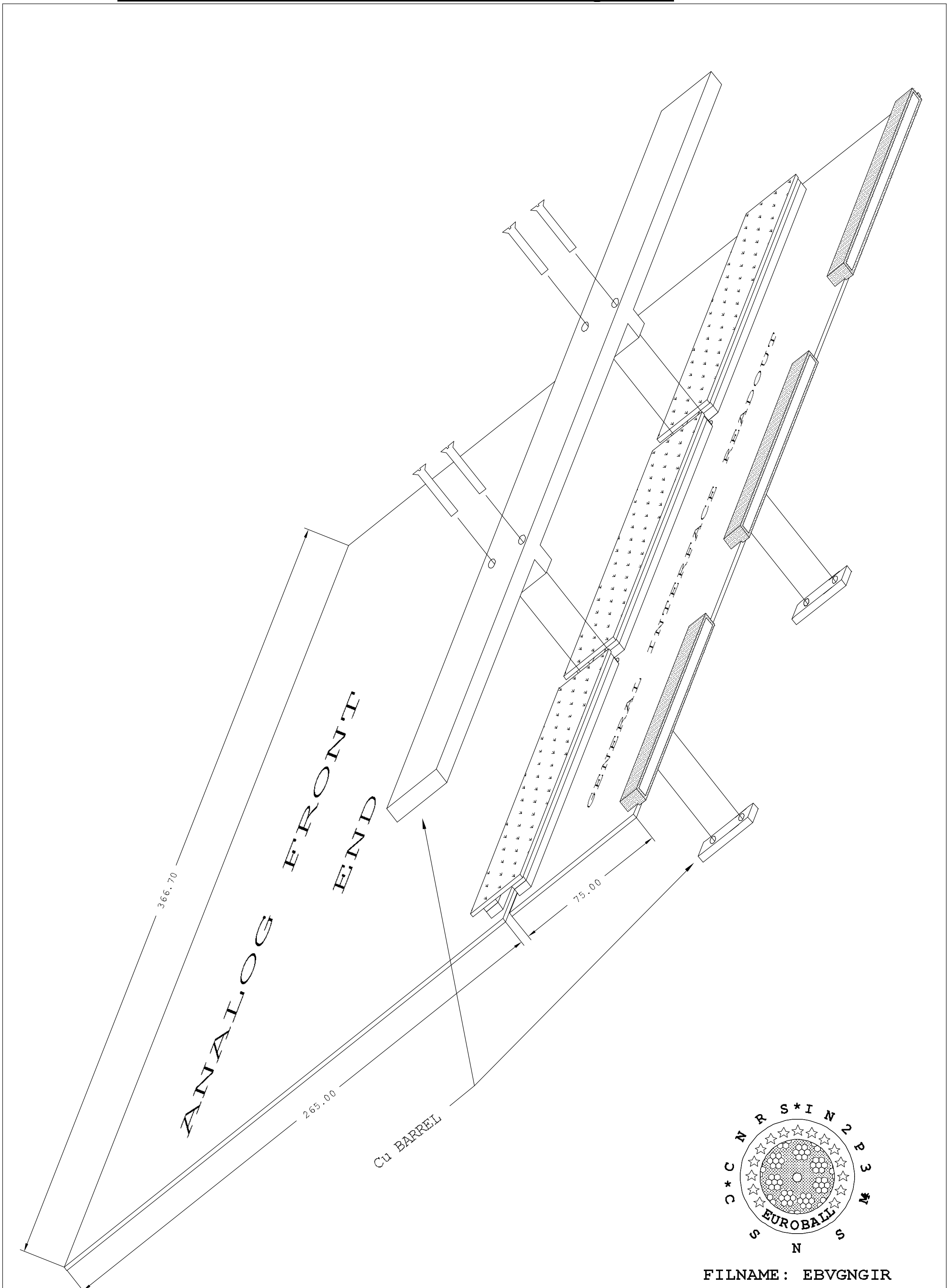
2.3.2.9 **Memory Map of the SIROP8 for 16 channel:** base Address : 0x100 & 0x180.

→→→ *modified by D. LINGET . ? ? ? ? **New New New New New?** ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?*
⌦ *will be modified by Alain Le Coguie by Check **Channel 1 Energy, Channel 2 Time or not ? ? ? ?***

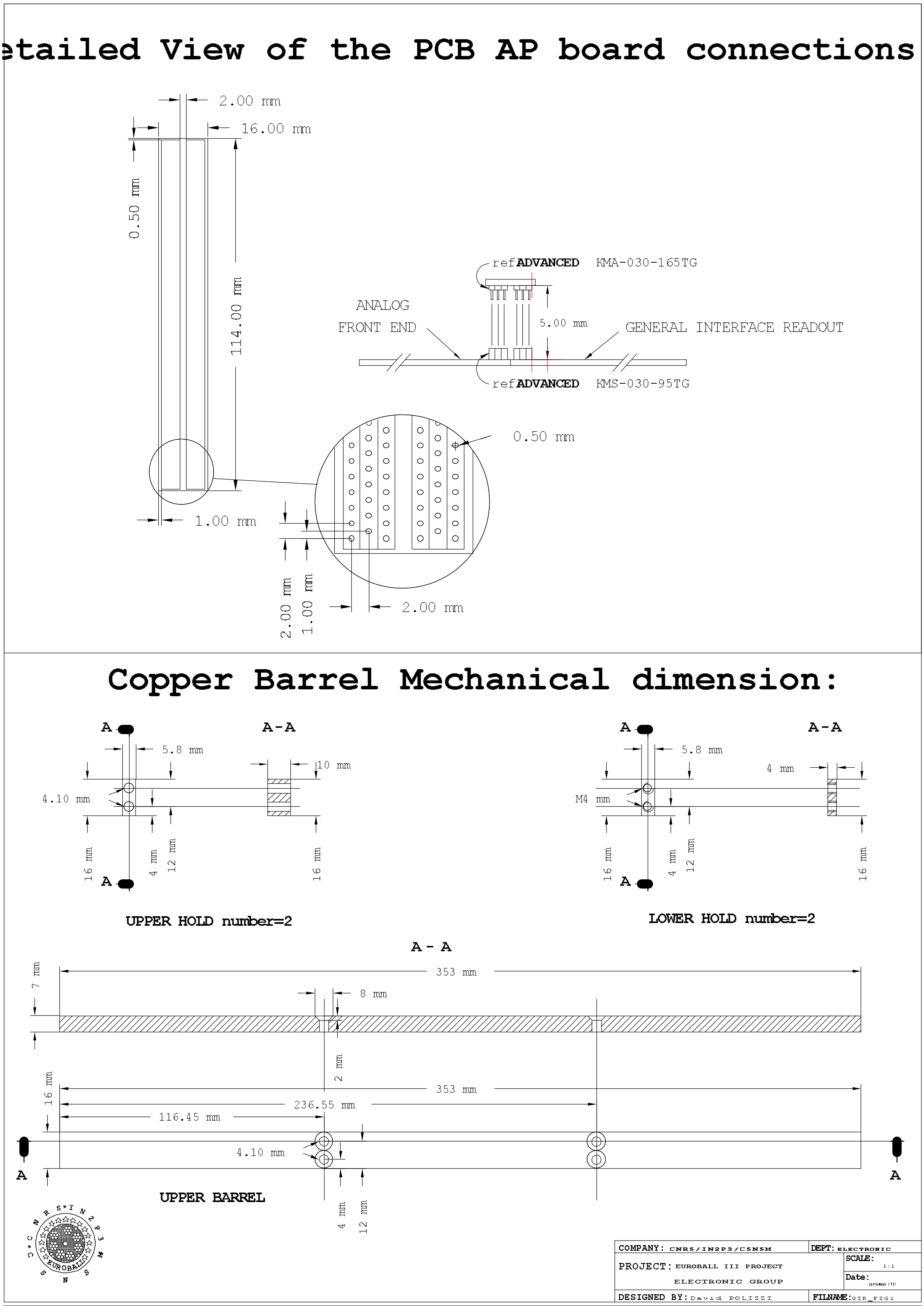
Offset Address	Bus Width	Read/ Write	Function
0x0	32	r/w	data [29:16] Item and Group, data[15:0] simulate ADC data for channel 1
0x4	32	r/w	data [29:16] Item and Group, data[15:0] simulate ADC data for channel 2
...			
0x3C	32	r/w	data [29:16] Item and Group, data[15:0] simulate ADC data for channel 16
0x40	32	r/w	enable Dtready in test mode data[15:0] corresponds to channel 16 to 1
0x44	32	r/w	enable channel for readout data[15:0] corresponds to channel 16 to 1 data [17:16] ADC shift value (00 noshift, 01 shift by 1, 10 shift by 2, 11 shift by 3 bit) data 18 is sliding scale enable, data [29:19] is spare
0x48	32	r/w	Sliding Scale load value

3. General Figures:

3.1.Isometric View of the G.I.R. & the Analog card:

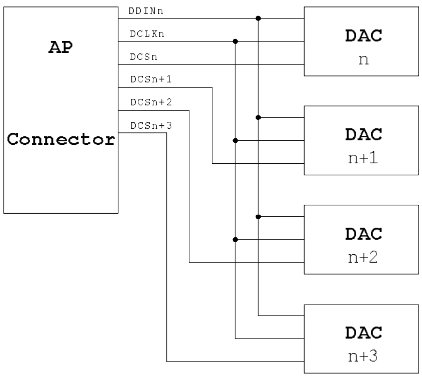


3.2. Copper Barrel Mechanical Dimensions,& PCB AP board connections:

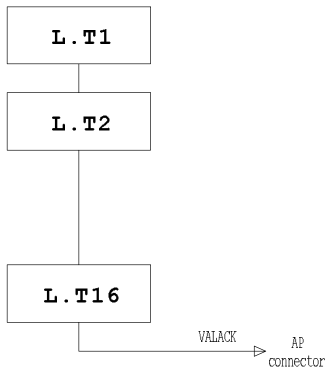


3.3. SAPHIR Dacs, Local Trigger Valack, Serial E²Prom, & Temperature Sensor connections figure :

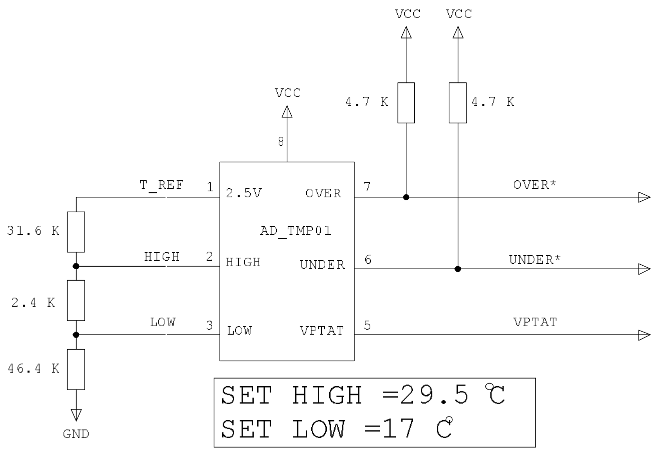
Dac connection figure:



Valack L.T connection:

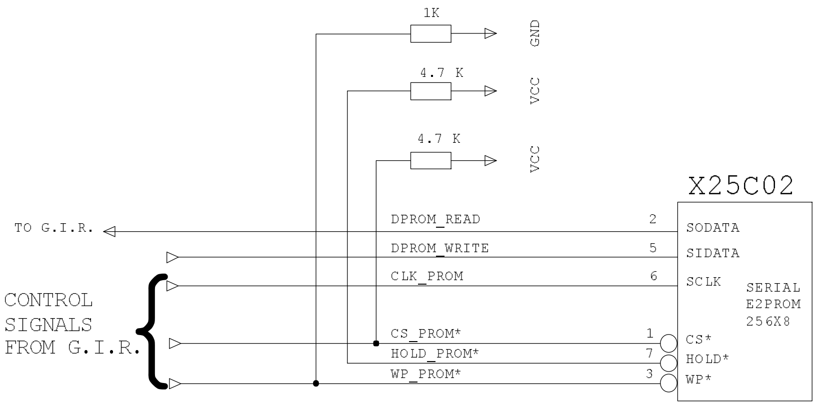


Temperature Sensor Connection Figure:



Filenam:SAP_GIR

Serial E2Prom Connection Figure:



3.4. GIR power supply ratings on the AP connectors for the Analog card:

Voltage	Current +/-10%
- 2 V	8 A
+ 5 V	7 A
- 5.2 V	10 A
+ 12 V	2 A
- 12 V	2 A
+ 24 V	2 A
- 24 V	2 A

3.5. SIROP - PROM connection figure :