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Euroball Project

G. I.R.

General Interface Readout

Ver 2.0 (Defined version for phase I)

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Contents:

1. Introduction:

One of the solutions for electronics of the data acquisition systems in Nuclear physics experiments is to use *VXI* (VME eXtension bus for Instrumentation) standard electronics.

In *Euroball III* we have new detectors called the *Cluster* detector. Each detector contains seven *Ge* crystals, and 18 BGO. This means that electronics cannot be in one *VXI* card as the *Clover* detector electronics used in Eurogam II for example, and to make things easy all the crystals of the same type should be in the same *VXI* card. That is we need two *VXI* cards to make the data acquisition of one *Cluster* detector. These boards are: The *Ge*, and *BGO*. *PPADC Cluster* (used for low Energy *Ge*) is a new way of data acquisition analysis. Each *VXI* card must include the same no. of crystals plus one spare; so the *Ge*, *PPADC Cluster* has 8 channels, and the *BGO* has 20 (18 crystals, one sum Energy, plus one spare). In *Eurogam I & II* we had only six channels per *VXI* card. Therefore the need of space on each card is a major problem. **Only** 75 mm x 366 mm is left for card configuration logic, Readout interface logic (internal, and external), *FIFO's* to write the current event data in, *VXI* power supply filtering, Inspection lines control logic, *DSP* control for multiprocessing plus new features were requested etc...

G.I.R. was accepted because it responds to the above requests. The *G.I.R.* is a **G**eneral **I**nterface **R**eadout card, which is connected between the *VXI* back plane and an *Analog* card, so that the 2 cards (*G.I.R.-Analog*) form a complete *VXI* D-size Board. This Board have general re programmable Input/ Output signals that can be connected to other *Analog* cards for different data acquisition. For example in *Euroball III*, there are three types of *Analog* cards for each *Cluster* detector, and the same *G.I.R.* should be used. The only changes are the programmable devices in each *PCB*, but the printed circuit Board is the same. This is an advantage because the budget for the *G.I.R.* is much cheaper for all the *VXI* electronics than different *PCB's* specific for each card. Also the testing of the cards is easier if we have the same *PCB* even if the *LCA* 's designs are different.

The *G.I.R.* 's job is to read out the *ADC* data (through the *SAROC* for the *Ge*, and *BGO*), and writes them into the *FIFO's*, then these data are transferred to the *ReadOut Controller* Board on the *VXI* back plane. The Readout mechanism is completely programmable, and suitable for any acquisition system. In the case of *Euroball III*, *Eurogam* Readout interface is used. The *G.I.R.* can configure the *Analog* card, e.g. *DAC* adjustment Register set-up *Inspection Lines*, fully programmable internal Readout mechanism etc..

2. New Features:

There are some features other than the Readout interface and card decoding on this Board which are the following:

1. **T**emperature **S**ensor **A**larm. This feature uses a temperature sensor in which we have 3 outputs; 2 digital signals which indicates if the temperature is below a threshold, or above a threshold, and an Analog output which indicates the proportional voltage with respect to absolute temperature reference. The 2 digital signals are connected to a status Register in the G.I.R., and the Analog flag is connected to the Analog multiplexer inside the G.I.R.. This signal is then coded, and the data are send to the DSP.

2. *DSP* multiprocessing Control:
   This new feature is added to interconnect any assembly of *VXI* cards *DSP's* together through the *VXI* Local bus. This feature is completely programmable. That is by software control we can specify graphically which *VXI* cards can be grouped together through the Local bus, so that the *DSP* can have data exchange for Readout decision, and in this way we can decide in a more accurate way if the data in the *FIFOs* are good data or not. In another context, this decision acts as a trigger level which could be called *Readout trigger*, that is after the data are sent to the *FIFO's* the *DSP* can make some analysis on these data, and can interrupt the external Readout cycle if those analysis don't correspond to what the user needs. Other feature for the *DSP* is Local control on the *VXI* card for Analog signal through a 16 input Analog multiplexer; there are 2 free Analog flags on the AP connector, the Analog Inspection Lines as well as the Voltage inspection line are connected to this multiplexer, and the VXI power supplies are connected too. We can, for example, control the Automatic Pole Zero Adjustment specific for *Ge* detectors or other detectors which need Pole Zero Adjustment or other Automatic Dac Adjustment (by

DSP Programming). This multiplexer is connected to a local high Speed *ADC*, then the values are written in the *DSP RAM*, after which the *DSP* Processes the data, and send the correction to the *Software on-line* control through flag registers.

To define clearly the *G.I.R.* we will refer to the *Euroball III* Project as a concrete example. That is some technical words which belong only to *Euroball III*, but can be adapted to other applications.

3. General Description & Pinouts of the AP connectors.

The *G.I.R.* is connected to the *Analog* card through three connectors (3 x 56= 168 pins). These connectors are called *Analog_P* (*AP*) connectors. The connections between the *G.I.R.*, and the *Analog* card is made through a PCB (called the *PCB_AP*). The middle column of this connector is mostly connected to the ground for *EMC* precautions (for more details refer to the *Electrical Precautions*). These connectors are called **AP1, AP2, & AP3** (from top to bottom). All three connectors are fully compatible so that the same PCB_AP is used. For example the same power supply pins are connected through a routing shape. Table 1 describes the three AP connector pins, and their locations.

• AP1:

This connector contains the following signals:

a. 76 Input/ Output pins (called Reg_Io) which are fully programmable pins of a *XILINX FPGA* (*LCA decode1*).
b. 7 bits of a latched address bus (*ADD* 1 to *ADD* 7).
c. Filtered -2 volts *VXI* power supply.
d. 1 *Analog Flag* free signal which is connected to an analog multiplexer inside the G.I.R., and which can be digitised by the DSP program, plus two digital free I/O signals(RDFLAG1,2).

• AP2:

The *AP2* contains the following signals:

a. The higher 16 bit of a latched address bus (*ADD* 8 to *ADD* 23).
b. There is also the *Analog*, *Digital*, and Voltage Inspection Lines which come from the *Analog* card.
c. the lower 16 bits of the bidirectional data bus.
d. 16 input/output reprogrammable pins (called Reg_Io) from *XILINX FPGA* (*LCA Decode2)*.
e. 18 input/output pins from the *ReadOut LCA* (*READ* 0 to *READ* 17 except *READ* 6,8,10,11,14 which are buffered output signals to the *Analog card*.
f. 4 *TTL* signals which come from the *VXI* back plane as *ECL* signals (they are the *Trigger Event* numbers in *Euroball III*),
g. the *VME* 16 MHz Clock, and filtered +/- 12 volts *VXI* power supply.
h. 1 *Analog Flag* free signal which is connected to an analog multiplexer inside the G.I.R., and which can be digitised by the DSP program, and two digital free I/O signals (RDFLAG3 ,4).

• AP3:

The *AP3* connector contains the following signals:

a. The higher 16 bits of the data bus (*DATA* 16 to *DATA* 31).
b. 5 input/output signals from the *ReadOut LCA* (*READ* 18 to *READ* 22).
c. The Differential *VXI* line Starx +/- , and 2 *TTL* Trigger lines (which is the *Fast Trigger*, *Validation*, and *Inhibit* signals respectively). They are the *Euroball MASTER Trigger* signals.
d. Moreover there are 49 INPUT/output pins from *LCA Decode2* (called Reg_IO).
e. 4 bits which are connected to the highest nibble in the FIFO, they are the event no. latched in the Analog Board.
f. 3 TTL signals which can be used as flags for the DSP

Pinouts of the General AP Connector figure. (Table 1):

	AP1 Connector			AP2 Connector			AP3 Connector			
PIN NO.	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	PIN NO.
1	+5 V	AFLAG1	+5 V	+5 V	AFLAG2	+5 V	+5v	DSPFLAG1	+5v	1
2	+5 V	+5v	+5 V	+5 V	+5 V	+5 V	+5v	+5v	+5v	2
3	Reg_Io	RDFLAG1	Reg_Io	Reg_Io	RDFLAG3	Reg_Io	DATA 16	DSPFLAG2	DATA 17	3
4	Reg_Io	RDFLAG2	Reg_Io	Reg_Io	RDFLAG4	Reg_Io	DATA 18	DSPFLAG3	DATA 19	4
5	Reg_Io	LED	Reg_Io	Reg_Io	LED	Reg_Io	DATA 20	LED	DATA 21	5
6	Reg_Io	GND	Reg_Io	16 Mhz	GND	Reg_Io	DATA 22	GND	DATA 23	6
7	Reg_Io	GND	Reg_Io	GND	GND	Reg_Io	GND	GND	GND	7
8	Reg_Io	GND	Reg_Io	ADD 8	GND	ADD 9	DATA 24	GND	DATA 25	8
9	Reg_Io	GND	Reg_Io	ADD 10	GND	ADD 11	DATA 26	GND	DATA 27	9
10	Reg_Io	GND	Reg_Io	ADD 12	GND	ADD 13	DATA 28	GND	DATA 29	10
11	Reg_Io	GND	Reg_Io	ADD 14	GND	ADD 15	DATA 30	GND	DATA 31	11
12	Reg_Io	GND	Reg_Io	ADD 16	GND	ADD 17	GND	GND	GND	12
13	Reg_Io	GND	Reg_Io	ADD 18	GND	ADD 19	EVT_out0	GND	EVT_out1	13
14	Reg_Io	GND	Reg_Io	ADD 20	GND	ADD 21	EVT_out2	GND	EVT_out3	14
15	Reg_Io	GND	Reg_Io	ADD 22	GND	ADD 23	READ 18	GND	READ 19	15
16	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	16
17	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	17
18	Reg_Io	GND	Reg_Io	Reg_Io	GND	Reg_Io	READ 20	GND	READ 21	18
19	Reg_Io	GND	Reg_Io	Reg_Io	GND	Reg_Io	FT_ECL +	GND	READ 22	19
20	Reg_Io	GND	Reg_Io	AI 1	GND	GND	GND	GND	FT_ECL -	20
21	Reg_Io	GND	Reg_Io	GND	GND	GND	FT_ttl_buf	GND	Inhibit_buf	21
22	Reg_Io	GND	Reg_Io	AI 2	GND	GND	VAL_buf	GND	Reg_Io	22
23	Reg_Io	GND	Reg_Io	GND	GND	DI 1	Reg_Io	GND	Reg_Io	23
24	Reg_Io	GND	Reg_Io	DI 2	GND	GND	Reg_Io	GND	Reg_Io	24
25	Reg_Io	GND	Reg_Io	Reg_Io	GND	VI	Reg_Io	GND	Reg_Io	25
26	Reg_Io	GND	Reg_Io	Reg_Io	GND	Reg_Io	Reg_Io	GND	Reg_Io	26
27	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	27
28	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	28
29	Reg_Io	GND	Reg_Io	DATA 0	GND	DATA 1	Reg_Io	GND	Reg_Io	29
30	Reg_Io	GND	Reg_Io	DATA 2	GND	DATA 3	Reg_Io	GND	Reg_Io	30
31	Reg_Io	GND	Reg_Io	DATA 4	GND	DATA 5	Reg_Io	GND	Reg_Io	31
32	Reg_Io	GND	Reg_Io	DATA 6	GND	DATA 7	Reg_Io	GND	Reg_Io	32
33	Reg_Io	GND	Reg_Io	GND	GND	GND	Reg_Io	GND	Reg_Io	33
34	Reg_Io	GND	Reg_Io	DATA 8	GND	DATA 9	Reg_Io	GND	Reg_Io	34
35	Reg_Io	GND	Reg_Io	DATA 10	GND	DATA 11	Reg_Io	GND	Reg_Io	35
36	Reg_Io	GND	Reg_Io	DATA 12	GND	DATA 13	Reg_Io	GND	Reg_Io	36
37	Reg_Io	GND	Reg_Io	DATA 14	GND	DATA 15	Reg_Io	GND	Reg_Io	37
38	Reg_Io	GND	Reg_Io	EVT_IN0	GND	EVT_IN1	Reg_Io	GND	Reg_Io	38
39	Reg_Io	GND	Reg_Io	EVT_IN2	GND	EVT_IN3	Reg_Io	GND	Reg_Io	39
40	Reg_Io	GND	Reg_Io	READ 0	GND	READ 1	Reg_Io	GND	Reg_Io	40
41	Reg_Io	GND	Reg_Io	READ 2	GND	READ 3	Reg_Io	GND	Reg_Io	41
42	Reg_Io	GND	Reg_Io	READ 4	GND	READ 5	Reg_Io	GND	Reg_Io	42
43	Reg_Io	GND	Reg_Io	Read 6_buf	GND	READ 7	Reg_Io	GND	Reg_Io	43
44	Reg_Io	GND	Reg_Io	READ 8	GND	Read 9_buf	Reg_Io	GND	Reg_Io	44
45	Reg_Io	GND	ADD1	READ 10	GND	R/W_buf	Reg_Io	GND	Reg_Io	45
46	ADD2	GND	ADD3	READ 12	GND	Read13_buf	Reg_Io	GND	Reg_Io	46
47	ADD4	GND	ADD5	Read 14_buf	GND	READ 15	Reg_Io	GND	Reg_Io	47
48	ADD6	GND	ADD7	READ 16	GND	READ 17	Reg_Io	GND	Reg_Io	48
49	+5 V	GND	+5 V	+5 V	GND	+5 V	+5 V	GND	+5 V	49
50	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	50
51	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	51
52	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	52
53	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	53
54	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	54
55	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	55
56	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	56

4. Readout Mechanism:

The Readout Mechanism will be divided into two cycles: Internal, and External Readout cycles. The Internal cycle is the cycle which takes place for data transfer between the *Analog* card, and the *G.I.R.*. While the External Readout cycle is the interface between the *G.I.R*, and the *Readout Controller* Board. In *Euroball III SAROC's* Chips will be used on the *Analogue* card to put the *ADC* data into registers (32 bit wide) to be transferred to the *G.I.R.* into the *FIFO's*. So the internal Readout cycle is similar to *Eurogam Readout* cycle. The only difference is that the *SAROC's* have twelve inputs, and they are faster than the *Eurogam ROCIs*.

In the External Readout cycle the *Eurogam* Readout interface will be used. We will upgrade later the Readout interface to several Readout mechanisms due to programmable devices (e.g. *SSBLT* or *MBLT 64* transfer etc.).

In *Euroball III* the *G.I.R.* uses as in *Eurogam* the same *VXI* lines dedicated for the *Digital*, and *Analog* multiplexing lines, *Fast* trigger, and *Validation* signals, etc...[1]

First, When the *CFD* of a *Ge* channel fires and when the *Sumbus* signal exceeds the sumbus threshold in the *MASTER trigger*, this latter sends a *Fast Trigger* signal followed by a *Validation* signal (with the event no. on the *VXI* local bus) as a confirmation that the present event (which is already running) is a good event to be coded, and the data in the ADCs are to be read out or transferred into the *FIFO*[2].

When it receives *Validation* the crate *ReadOut COntroller* asserts the *AS** (Address Strobe) signal onto the *VXI* back plane with the event no. on the *VME* address bus, and waits for the *VXI* boards that participate in this event by asserting or not *BLTACK** (*BLTACK** is an open collector signal). At that time the Readout interface inside each *G.I.R.* maintains *BLTACK** if *Validation Acknowledge* signal from the *Local Trigger*(s) is asserted, and it waits until the *ADC* data are sent out to the *FIFO*. The *ROCO* reads all the data from all the *VXI* cards by daisy chain[3]. For more details about how the *G.I.R.* builds its interface refer to the *Readout* document, concerning both the Internal, and the External Readout mechanism.

5. Electrical, and Mechanical precautions:

This card is specifically designed for low noise Analog data acquisition systems. It takes care of the *EMC* problems. It already contains several elements which worked before in other similar cards. Data transfer is 20 Mbytes/sec 5 Mwords/sec, and in *Nuclear* physics data acquisition systems the shaping time and the coding time take highest percentage of the total channel dead time.
The aim of this Board is to have Readout interface completely programmable for different Readout mechanisms, and which can be suitable for different data acquisitions. That is it can be adapted to either fast or slow data transfers. The Analog engineer need not be anxious about the Readout part of his Board. He needs only to design his Board up to digital data, and then he has to choose the Readout system to be adapted for his experiment, so that the Readout interface can be built.

1. Electrical precautions:

EMC problems are very dangerous to sensitive Analog signals, especially in *Nuclear* physics data acquisitions. *G.I.R.* has the middle column of the 168 pin *AP* connectors (as shown previously) mostly grounded. Extra flat connectors will be used to minimise the electromagnetic noise penetrations. 16 MHz *VME* Clock will be used on the Board for the *DSP*. Slow asynchronous data transfer from the *FIFO's*. (see the *PCB_AP* connections diagram.). For example the 2 *Analog* Inspection Lines are surrounded with ground pins. Power Supply chokes, and *OSCON* capacitors are used to filter the *VXI* power supplies.

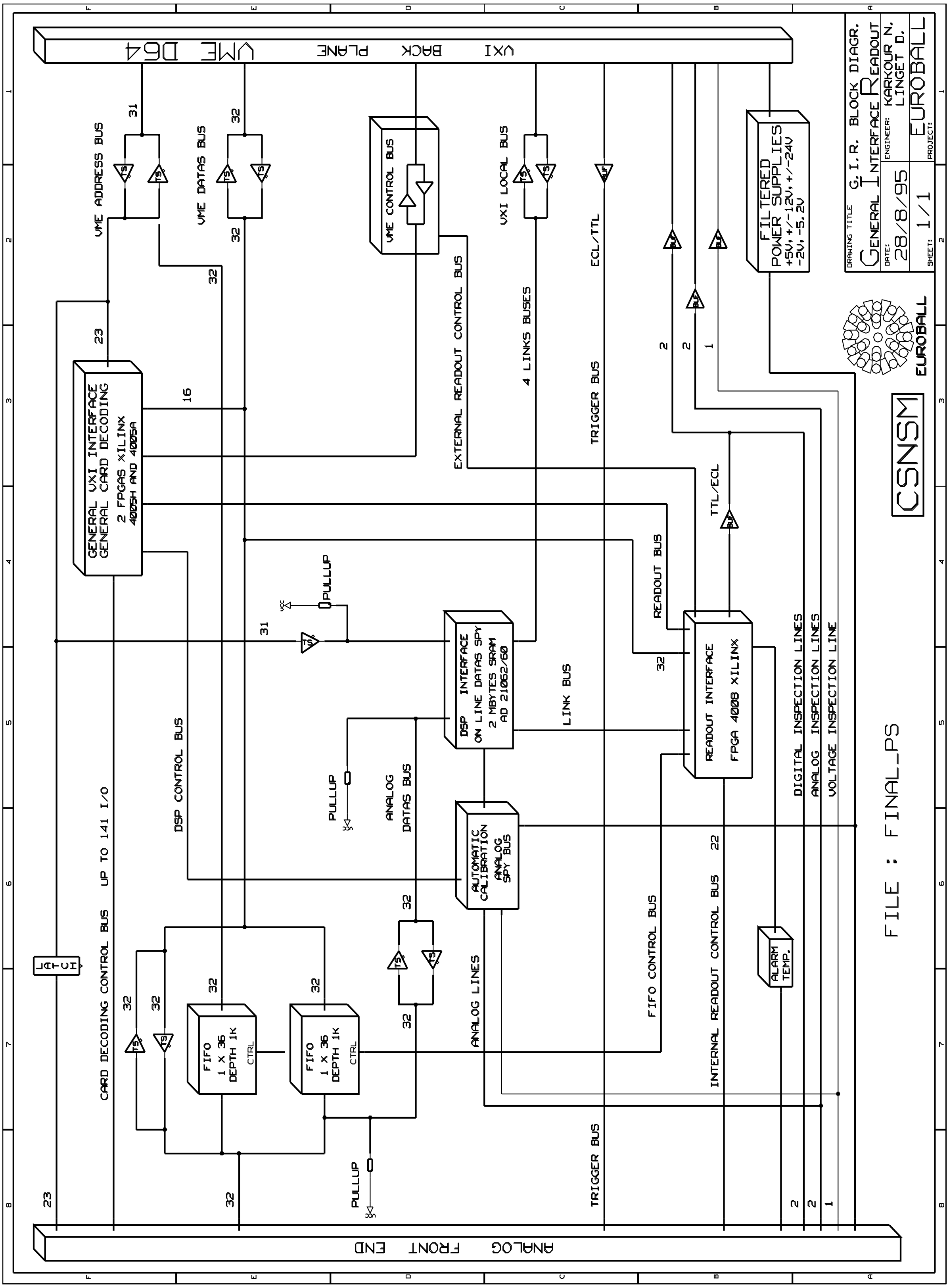
2. Mechanical precautions:

The interconnection between the *Analog* card and *G.I.R.* can be shown in the figures below showing the top, bottom, and face views. High ground precautions is taken on the top of the *Mother Board* by using a *Copper Barrel* shield over the three connectors, and on the bottom 2 small copper joints are fixed tightly as shown in the figure (*G.I.R.- Analog*). On the top side *EMC* joints are to be glued on those barrels so that they have good connections to the external *VXI* Board shield. The two diagrams, one with the mechanical details of the Copper Barrel, and one shows how the *G.I.R.* will be mounted data can show us clearly how the system is implemented. An extractor tool is built to extract the *PCB_AP* connector (336

[1]See the VXI Lines Definition Document by: A. Richard
[2]See the Euroball Trigger Specification by: I. Lazarus CLRC,, Daresbury U.K.
[3]See the Eurogam VXI Readout Specification by J. Alexander.

pins) out of both the *G.I.R.*, and the *Analog* card. A special tool exists to mount, and unmount the *G.I.R.*, and the *Analog* card together with the *PCB_AP* without having any pressure on the *SMD* components, just on the surrounding of both *PCB's* (see the mechanical dimensions, and the isometric view figures for more details).

6. Block Diagram of the G.I.R.:



7. Description of the A P connectors for the Cluster cards.

7.1. BGO Cluster AP Description.

• 1.1) AP1 :

- DCLKn **:** Clock signal to load the *DAC*s, this signal is common for the two channels *n* and *n+1* (see fig. *Dacs connections*).

- DDINn **:** serial data signal to load the *DACs*, this signal is common for the two channels *n* and *n+1* (see fig. *Dacs connections*).

- DCSn **:** Chip Select signal to load the *DAC*s, there is one signal per *Dac*, n = 1 to 3 (see fig. *Dacs connections*).

- CLKProm: serial PROM Clock signal of the *BGO Analog* card.

- CSProm : serial PROM Chip Select signal of the *BGO Analog* card.

- DProm_Write: serial PROM Data write to the *BGO Analog* card.

- DProm_Read: serial PROM Data to be read out of the *BGO Analog* card.

(see E²Prom connection figure).

- CCRnm **:** Channel Control Register, each signal enable or disable a function on each channel of the Analog part; *n* is the channel number (1 to 20) and *m* the bit Register number. There are two registers per channel :

0 ==> en/dis* channel.
1 ==> set/reset* channel.

- Latch_Card : This signal can be used to enable the data bus buffer on the *Analog* card. It is active, during a complete VME cycle, when the G.I.R. is selected

- ADD[7..1] : this is the lowest byte of the *VME* Address bus, it is enabled by the *LCA DECOD1*.

- Spare : these signals are not used in the *Euroball* BGO card, they are controlled by the *LCA DECOD1*. They can be used by the *Analog* card for future applications.

- VPTAT1 : Voltage Proportional To Absolute Temperature signal of the sensor 1 from the *Analog* card and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER1 : high level temperature signal of the sensor 1 from the *Analog* card.

- UNDER1 : low level temperature signal of the sensor 1 from the *Analog* card.

- LED 1: display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

• 1.2) AP2 :

- SAROCCSn **:** SAROC Chip Select signal for the configuration of the *SAROCs* in both the *BGO* card, n is the *SAROC* number (n = 1 to 4).

- 16 MHz: buffered *VME* System Clock signal.

- SAROCWstrb: Data Strobe signal for the configuration of the *SAROCs*, common for all the *SAROCs*.

- MRegn**:** 8 bits Module Register, each signal enable or disable a common function on the *Analog* card, *n* is the bit Register number.

0 ==> reject/mark* event on pileup.
1 ==> low/high* Timing Filter Amplifier gain.
2 ==> en/dis* Sliding Scale.
3 ==> high/zero* value fixed on Sliding Scale.
4 ==> high/zero* E²Prom Hold.
5, 6, 7 ==> spare, free use.

- ADD[23..8] : these are the other 2 bytes of the *VME* Address bus, they are enabled by the *LCA DECOD1*.

- AIn **:** Analogue Inspection Lines, n is the inspection line indicator.

- DIn **:** Digital Inspection Lines, n is the inspection line indicator.

- VI : Voltage Inspection Line.

- DATA[15..0] : these are the lower sixteen bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SAROC* and *FIFO* data bus during Readout mechanism.

- EVT_IN[3..0] : these lines are the current event number, they are given by the *MASTER Trigger* via the *VXI Local* bus to the Analog cards with *Validation* (LBus [11..8]).

- SAROCDtreadyn **:** data ready given by the *SAROCs* when a data is ready to be latched in the *FIFO*, n is the *SAROC* number.

- SAROCEmptyn **:** Empty flag given by the *SAROCs* when there are no data in it. These signals can check if there are data in the *SAROC* when the Readout takes place, n is the *SAROC* number.

- SAROCDTack_buf : buffered data acknowledge signal for each data word of the *SAROC* in a Readout cycle, common for all the *SAROCs*.

- Renin : start Readout cycle of the *SAROC*, this signal is sent to the first *SAROC*.

- RESET_A_buf : buffered Reset signal of the *Analog* card (acquisition) of the *SAROC*.

- LPASS : Last PASS, this is the renout signal of the last *SAROC* for the internal Readout mode.

- GLOBAL RESET : buffered global Reset signal of all the *Analog* card.

- R/W_buf : buffered *VME* read-write signal.

- OrValack : this signal is the result of the *OR* of all the *Validation Acknowledge* signals given by the *Local Trigger*.

- StartReadoutSaroc : This signal latches the *ADC* data in the *SAROC* internal registers, the back edge of this signal starts the internal Readout cycle.

- LT_Reset : buffered Reset signal for the *Local Trigger*.

- Coding : This is the coding dead time signal, which indicates that the *ADC* are coding, and no *VME* Action must take place. This signal goes to the *MASTER Trigger* as an open collector at the Back plane.

- Spare : these signals are not used in the *Euroball* BGO card, they are controlled by the *LCA DECODE2*. They can be defined for future applications.

- VPTAT2 : Voltage Proportional To Absolute Temperature signal of the sensor 2 from the Analog part and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER2 : high level temperature signal of the sensor 2 from the *Analog* card.

- UNDER2 : low level temperature signal of the sensor 2 from the *Analog* card.

- LED2 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

• 1.3) AP3 :

- DATA[31..16] : these are the sixteen higher bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SAROC* and *FIFO* data bus during Readout.

- EVT_out[3..0] : these lines are the event number that are sent with the data during acquisition mode, and are written in the *FIFO*.

- READ [21..18] : these signals are dedicated for Readout interface and are not used in the *Euroball BGO* card, they are controlled by the *LCA READOUT*. They can be defined for future applications.

- VETO : Veto signal given by the *BGO* card (shield) (this signal comes from the front panel for both the *Ge, & PPADC* boards, while for the *BGO* card this signal is generated from the internal mother Board).

- FT_ttl_buf : buffered *Fast Trigger* signal (positive TTL) from the *MASTER Trigger* (*starx* on the *VXI* back plane).

- Inhibit_buf : buffered *Inhibit* signal from the *MASTER Trigger* (on the *VXI* back plane).

- VAL_buf : buffered *Validation* signal from the *MASTER Trigger* (on the *VXI* back plane).

- FT_ECL -, FT_ECL+ : *Fast Trigger signals* (differential ECL) given by the *MASTER Trigger* (*starx* +/- on the *VXI* back plane). **These signals are not charged, the resistors MUST be placed on the Analog part.**

- DSPFLAG1, 2, 3 : these signals are not used for the moment in *Euroball*. They can be used later as a connection between the *DSP*, and the *Analog* card. They are controlled by the *DSP*.

- LED3 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

All the signals below are controlled by the *LCA DECODE2*.

- AnaSelAn **:** select signal of the Analog multiplexers for the Analog Inspection Line 1, *n* is the multiplexer select bit (n = 0 to 3)(the multiplexers are the same which are used in *Eurogam* and are *TTL* input compatible).

- AnaSelBn **:** select signal of the Analog multiplexers for the Analog Inspection Line 2, *n* is the multiplexer select bit (n = 0 to 3).

- AnEnAn **:** output enable signal of the Analog multiplexers for the Analog Inspection Line 1. There is one per multiplexer (3 are used for the BGO card).

- AnEnBn **:** output enable signal of the Analog multiplexers for the Analog Inspection Line 2. there is one per multiplexer (3 are used for the BGO card).

- DigSelAn **:** select signal of the digital multiplexers for the digital inspection line 1, *n* is the multiplexer select bit (n = 0 to 5).

- DigSelBn **:** select signal of the digital multiplexers for the digital inspection line 2, *n* is the multiplexer select bit (n = 0 to 5).

- VSel[3..0] : select bus of the voltage multiplexers. These signals must be common to all voltage multiplexers.

- Venablen **:** enable signal of the voltage multiplexers, 2 for BGO card.

- Spare : these signals are not used in the *Euroball* BGO cards, they can be defined for future applications.

- Vstrobe: load signal of all the voltage multiplexers.

- Anastrobe: load signal of all the Analog multiplexers.

Pinouts of the AP Connector for the BGO Cluster: (Table 2):

	AP1 Connector			AP2 Connector			AP3 Connector			
PIN NO.	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	PIN NO.
1	+5 V	VPTAT1	+5 V	+5 V	VPTAT2	+5 V	+5v	DSPFLAG1	+5v	1
2	+5 V	+5 V	+5 V	+5 V	+5v	+5 V	+5v	+5v	+5v	2
3	DCLK 1	OVER1	DDIN 1	SAROCCS1	OVER2	SAROCCS2	DATA 16	DSPFLAG2	DATA 17	3
4	DCS 1	UNDER1	Spare	SAROCCS2	UNDER2	SAROCCS4	DATA 18	DSPFLAG3	DATA 19	4
5	Spare	LED	DCS 2	Spare	LED	Spare	DATA 20	LED	DATA 21	5
6	DCLK 3	GND	DDIN 3	16 Mhz	GND	SAROCWstrb	DATA 22	GND	DATA 23	6
7	DCS 3	GND	Spare	GND	GND	MReg0	GND	GND	GND	7
8	Spare	GND	Spare	ADD 8	GND	ADD 9	DATA 24	GND	DATA 25	8
9	Spare	GND	Spare	ADD 10	GND	ADD 11	DATA 26	GND	DATA 27	9
10	Spare	GND	Spare	ADD 12	GND	ADD 13	DATA 28	GND	DATA 29	10
11	Spare	GND	Spare	ADD 14	GND	ADD 15	DATA 30	GND	DATA 31	11
12	Spare	GND	Spare	ADD 16	GND	ADD 17	GND	GND	GND	12
13	Spare	GND	Spare	ADD 18	GND	ADD 19	EVT_out0	GND	EVT_out1	13
14	Spare	GND	Spare	ADD 20	GND	ADD 21	EVT_out2	GND	EVT_out3	14
15	Spare	GND	Spare	ADD 22	GND	ADD 23	SAROC 18	GND	SAROC 19	15
16	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	16
17	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	17
18	Spare	GND	Spare	MReg 1	GND	MReg2	SAROC 20	GND	SAROC 21	18
19	Spare	GND	Spare	MReg 3	GND	MReg4	FT_ECL +	GND	VETO	19
20	Spare	GND	Spare	AI 1	GND	GND	GND	GND	FT_ECL -	20
21	Clk Prom	GND	DProm_Write	GND	GND	GND	FT_ttl_buf	GND	Inhibit_buf	21
22	CS Prom	GND	DProm_Read	AI 2	GND	GND	VAL_buf	GND	AnaSelA 0	22
23	CCR 10	GND	CCR 11	GND	GND	DI 1	AnaSelA 1	GND	AnaSelA 2	23
24	CCR 20	GND	CCR 21	DI 2	GND	GND	AnaSelA 3	GND	AnaSelB 0	24
25	CCR 30	GND	CCR 31	MReg 5	GND	VI	AnaSelB 1	GND	AnaSelB 2	25
26	CCR 40	GND	CCR 41	MReg 6	GND	MReg7	AnaSelB 3	GND	AnEnA 1	26
27	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	27
28	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	28
29	CCR 50	GND	CCR 51	DATA 0	GND	DATA 1	AnEnA 2	GND	AnEnA 3	29
30	CCR 60	GND	CCR 61	DATA 2	GND	DATA 3	AnEnB 1	GND	AnEnB 2	30
31	CCR 70	GND	CCR 71	DATA 4	GND	DATA 5	AnEnB 3	GND	DigSelA 0	31
32	CCR 80	GND	CCR 81	DATA 6	GND	DATA 7	DigSelA 1	GND	DigSelA 2	32
33	CCR 90	GND	CCR 91	GND	GND	GND	DigSelA 3	GND	DigSelA 4	33
34	CCR A0	GND	CCR A1	DATA 8	GND	DATA 9	DigSelA 5	GND	DigSelB 0	34
35	CCR B0	GND	CCR B1	DATA 10	GND	DATA 11	DigSelB 1	GND	DigSelB 2	35
36	CCR C0	GND	CCR C1	DATA 12	GND	DATA 13	DigSelB 3	GND	DigSelB 4	36
37	CCR D0	GND	CCR D1	DATA 14	GND	DATA 15	DigSelB 5	GND	VSel 0	37
38	CCR E0	GND	CCR E1	EVT_IN0	GND	EVT_IN1	VSel 1	GND	Vsel 2	38
39	CCR F0	GND	CCR F1	EVT_IN2	GND	EVT_IN3	Vsel 3	GND	Venable 1	39
40	CCR G0	GND	CCR G1	SarocDtready 0	GND	SarocDtready 1	Venable 2	GND	Spare	40
41	CCR H0	GND	CCR H1	SarocDtready 2	GND	SarocDtready 3	Spare	GND	Spare	41
42	CCR J0	GND	CCR J1	SarocEmpty 0	GND	SarocEmpty 1	Spare	GND	Spare	42
43	CCR K0	GND	CCR K1	SAROCDtack	GND	Renin	Spare	GND	Spare	43
44	CCR M0	GND	CCR M1	RESET A_buf	GND	LPASS	Spare	GND	Spare	44
45	Latch_Card	GND	ADD 1	GlobalReset	GND	R/W_buf	Anastrobe	GND	Vstrobe	45
46	ADD 2	GND	ADD 3	OrValack	GND	StartReadoutSaroc	Spare	GND	Spare	46
47	ADD 4	GND	ADD 5	LT_Reset	GND	SarocEmpty 2	Spare	GND	Spare	47
48	ADD 6	GND	ADD 7	SarocEmpty 3	GND	Coding	Spare	GND	Spare	48
49	+5 V	GND	+5 V	+5 V	GND	+5 V	+5 V	GND	+5 V	49
50	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	50
51	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	51
52	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	52
53	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	53
54	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	54
55	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	55
56	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	56

7.2. Germanium Cluster AP description.

• 1.1) AP1 :

- DCLKn **:** Clock signal to load the *DAC*s, this signal is common for the two channels *n* and *n+1* (see fig. *Dacs connections*).

- DDINn **:** serial data signal to load the *DACs*, this signal is common for the two channels *n* and *n+1* (see fig. *Dacs connections*).

- DCSn **:** Chip Select signal to load the *DAC*s, there is one signal per Dac, n = 1 to 9 (see fig. *Dacs connections*).

- CLKProm : serial PROM Clock signal of the *Ge Analog* card.

- CSProm : serial PROM Chip Select signal of the *Ge Analog* card.

- DProm_Write: serial PROM Data write to the *Ge Analog* card.

- DProm_Read: serial PROM Data to be read out of the *Ge Analog* card.

(see E²Prom connection figure).

- CCRnm **:** Channel Control Register, each signal enable or disable a function on each channel of the Analog part; *n* is the channel number (1 to 8) and *m* the bit Register number. There are four registers per channel :

0 ==> en/dis* channel.
1 ==> en/dis* test generator channel.
2 ==> spare, free use.
3 ==> spare, free use.

- Latch_Card : This signal can be used to enable the data bus buffer on the *Analog* card. It is active, during a complete VME cycle, when the G.I.R. is selected

- ADD[7..1] : this is the lowest byte of the *VME* Address bus, it is enabled by the *LCA DECOD1*.

- Spare : these signals are not used in the *Euroball Ge Cluster* card, they are controlled by the *LCA DECOD1*. They can be used by the *Analog* card for future applications.

- VPTAT1 : Voltage Proportional To Absolute Temperature signal of the sensor 1 from the *Analog* part and controlled by the *DSP* (via an *ADC*). (see fig. *Sensors connections*).

- OVER1 : high level temperature signal of the sensor 1 from the *Analog* card.

- UNDER1 : low level temperature signal of the sensor 1 from the *Analog* card.

- LED 1: display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

• 1.2) AP2 :

- SAROCCSn **:** *SAROC* Chip Select signal for the configuration of the *SAROCs* in both the Ge *Cluster* card, n is the *SAROC* number (n = 1 to 2).

- 16 MHz : buffered VME System Clock signal.

- SAROCWstrb : buffered data Strobe signal for the configuration of the *SAROCs*, common for all the *SAROCs*.

- MRegn **:** 8 bits buffered Module Register, each signal enable or disable a common function on the *Analog* card, *n* is the bit Register number.

0 ==> reject/mark* event on pileup.
1 ==> low/high* Timing Filter Amplifier gain.
2 ==> en/dis* Sliding Scale.
3 ==> high/zero* value fixed on Sliding Scale.
4 ==> high/zero* PROM Hold.
5, 6, 7 ==> spare, free use.

- ADD[23..8] : these are the other 2 bytes of the *VME* Address bus, they are latched by the *LCA DECOD1*.

- AIn **:** Analogue Inspection Lines, n is the inspection line indicator.

- DIn **:** Digital Inspection Lines, n is the inspection line indicator.

- VI : Voltage Inspection Line.

- DATA[15..0] : these are the lower sixteen bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SAROC* and *FIFO* data bus during Readout mechanism.

- EVT_IN[3..0] : these lines are the current event number, they are given by the *MASTER Trigger* via the *VXI Local* bus **TO** the *Analog* cards with *Validation* (LBus [11..8]).

- SAROCDtreadyn **:** data ready given by the *SAROCs* when a data is ready to be latched in the *FIFO*, n is the *SAROC* number.

- SAROCEmptyn **:** Empty flag given by the *SAROCs* when there are no data in it. These signals can check if there are data in the *SAROC* when the Readout takes place, n is the *SAROC* number.

- SAROCDtack : buffered data acknowledge signal for each data word of the *SAROC* in a Readout cycle, common for all the *SAROCs*.

- Renin : Renin signal of the first *SAROC*.

- RESETA_buf : buffered Reset signal of the Analog part (acquisition) of the *SAROC*.

- LPASS : Last PASS, this is the renout signal of the last *SAROC* for the internal Readout mode.

- GLOBALReset : buffered global Reset signal of the Analog card.

- R/W_buf : buffered *VME* read-write signal.

- Valackn **:** this signal is the *Validation Acknowledge* given by the *Local Trigger*. For the Ge card we have n=1 to 8.

- StartReadoutSaroc : This signal latches the *ADC* data in the *SAROC* internal registers, the back edge of this signal starts the internal Readout cycle.

- LT_Reset : buffered Reset signal for the *Local Trigger*.(active Low).

- Conv_DTb : This is the coding dead time signal, which indicates that the *ADC* are coding, and no *VME* Action must take place. This signal goes to the *MASTER Trigger* as an open collector at *the VXI Back plane*.

- Spare : these signals are not used in the *Euroball Ge Cluster* Card, they are controlled by the *LCA DECODE2*. They can be defined for future applications.

- AFLAG2 : Free Analog signal from the *Analog* card, controlled by the *DSP* (via an *ADC*).

- Inhibit_Card : Local Inhibit signal for the *Analog* card. Used for inspection Lines.

- ExtResetLT: Local Trigger Reset from Reset Logic of the *Analog* card. Used for inspection Lines.

- LED2 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

• 1.3) AP3 :

- DATA[31..16] : these are the sixteen higher bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SAROC* and *FIFO* data bus during Readout.

- EVT_out[3..0] : these lines are the event number that are sent with the data during acquisition mode, and are written in the *FIFO*.

- OR8CFDdly : This is the out put of an Or 8 CFD delayed signals. Used for inspection Lines.

- BGOVETO : Veto signal given by the *BGO* card (shield) (this signal comes from the front panel for the *Ge, & PPADC* boards, while for the *BGO* card this signal is generated from the internal mother Board).

- FT_ttl_buf : buffered *Fast Trigger* signal (positive *TTL*) from the *MASTER Trigger* (*starx* +/- on the *VXI* back plane).

- Inhibit_buf : buffered *Inhibit* signal from the *MASTER Trigger* (on the *VXI* back plane).

- VAL_buf : buffered *Validation* signal from the *MASTER Trigger* (on the *VXI* back plane).

- FT_ECL-, FT_ECL+ : *Fast Trigger* signals (differential *ECL*) given by the *MASTER Trigger* (*starx* +/- on the *VXI* back plane). **These signals are not charged, the resistors MUST be placed on the Analog part.**

- DSPFLAG1, 2, 3 : these signals are not used for the moment in Euroball. They can be used later as a connection between the DSP, and the Analog card. They are controlled by the *DSP*.

- LED3 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

All the signals below are controlled by the *LCA DECODE2*.

- AID[7..4,3..0] : select signal of the multiplexers for the Analog Inspection lines, *n* is the multiplexer select bit (0 to 3 for Line 1, 4 to 7 for Line 2). The multiplexers are the same which are used in *Eurogam* and are *TTL* input compatible. These select bus are inverted i. e. input *0x0* on the *Mux*. gives channel *0xF*.

- AIm**-OE**n-n+1 **:** output enable signal of the multiplexers for the Analog Inspection lines. There is one per multiplexer, *n* is the channel select bit (n = 1, 3, 5, 7), m is the select line number.

- SRCELI[3..0] : select bus of the multiplexers for the Digital Inspection lines.

- LIm**-OE**n-n+1**:** output enable signal of the multiplexers for the Digital Inspection lines 1. There is one per multiplexer, *n* is the channel select bit (n = 1, 3, 5, 7), m is the select line number.

- MUX_CH_SEL: channel select signal of the multiplexers for the Digital Inspection lines (with 0 for the odd channels, 1 for the even).

- AMD[3..0] : select bus of the voltage multiplexers. These signals must be common to all voltage multiplexers.

- MTOEn-n+1 **:** output enable signal of the voltage multiplexers, there is one per multiplexer, *n* is the channel select bit (n = 1, 3, 5, 7).

- MTOE1 : output enable signal of the voltage multiplexer for global parameters.

- Vstrobe : Strobe signal of all the voltage multiplexers.

- Anastrobe : Strobe signal of all the Analog multiplexers.

- Dloadn **:** load signal of digital multiplexers, n is digital inspection line number.

- Spare : these signals are not used in the *Euroball Ge Cluster* cards, they can be defined for future applications.

Pinouts of the AP Connector for the Ge Cluster: (Table 3):

	AP1 Connector			AP2 Connector			AP3 Connector			
PIN NO.	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	PIN NO.
1	+5 V	VPTAT 1	+5 V	+5 V	AFLAG2	+5 V	+5v	DSPFLAG1	+5v	1
2	+5 V	+5 V	+5 V	+5 V	+5v	+5 V	+5v	+5v	+5v	2
3	DCLK1	OVER 1	DDIN 1	SAROCCS1	Inhibit_card	SAROCCS2	DATA 16	DSPFLAG2	DATA 17	3
4	DCS 1	UNDER 1	Spare	Spare	ExtResetLT	Spare	DATA 18	DSPFLAG3	DATA 19	4
5	Spare	LED 1	DCS 2	Spare	LED 2	Spare	DATA 20	LED 3	DATA 21	5
6	DCLK 3	GND	DDIN 3	16 Mhz	GND	SAROCWstrb	DATA 22	GND	DATA 23	6
7	DCS 3	GND	Spare	GND	GND	MReg0	GND	GND	GND	7
8	Spare	GND	DCS 4	ADD 8	GND	ADD 9	DATA 24	GND	DATA 25	8
9	DCLK 5	GND	DDIN 5	ADD 10	GND	ADD 11	DATA 26	GND	DATA 27	9
10	DCS 5	GND	Spare	ADD 12	GND	ADD 13	DATA 28	GND	DATA 29	10
11	Spare	GND	DCS 6	ADD 14	GND	ADD 15	DATA 30	GND	DATA 31	11
12	DCLK7	GND	DDIN 7	ADD 16	GND	ADD 17	GND	GND	GND	12
13	DCS 7	GND	Spare	ADD 18	GND	ADD 19	EVT_out0	GND	EVT_out1	13
14	Spare	GND	DCS 8	ADD 20	GND	ADD 21	EVT_out2	GND	EVT_out3	14
15	DCLK9	GND	DDIN 9	ADD 22	GND	ADD 23	Valack6	GND	Valack7	15
16	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	16
17	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	17
18	DCS 9	GND	Spare	MReg 1	GND	MReg2	Valack8	GND	OR8CFDdly	18
19	Spare	GND	Spare	MReg 3	GND	MReg4	FT_ECL +	GND	BGOVETO	19
20	Spare	GND	Spare	AI 1	GND	GND	GND	GND	FT_ECL -	20
21	Clk Prom	GND	Dprom_Write	GND	GND	GND	FT_ttl_buf	GND	Inhibit_buf	21
22	CS Prom	GND	DProm_Read	AI 2	GND	GND	VAL_buf	GND	AID 0	22
23	CCR 10	GND	CCR 11	GND	GND	DI 1	AID 1	GND	AID 2	23
24	CCR 12	GND	CCR 13	DI 2	GND	GND	AID 3	GND	AID 4	24
25	CCR 20	GND	CCR 21	MReg 5	GND	VI	AID 5	GND	AID 6	25
26	CCR 22	GND	CCR 23	MReg 6	GND	MReg7	AID 7	GND	AI1-OE12	26
27	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	27
28	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	28
29	CCR 30	GND	CCR 31	DATA 0	GND	DATA 1	AI1-OE34	GND	AI1-OE56	29
30	CCR 32	GND	CCR 33	DATA 2	GND	DATA 3	AI1-OE78	GND	AI2-OE12	30
31	CCR 40	GND	CCR 41	DATA 4	GND	DATA 5	AI2-OE34	GND	AI2-OE56	31
32	CCR 42	GND	CCR 43	DATA 6	GND	DATA 7	AI2-OE78	GND	SRCELI 0	32
33	CCR 50	GND	CCR 51	GND	GND	GND	SRCELI 1	GND	SRCELI 2	33
34	CCR 52	GND	CCR 53	DATA 8	GND	DATA 9	SRCELI 3	GND	Mux_ch_sel	34
35	CCR 60	GND	CCR 61	DATA 10	GND	DATA 11	LI1-OE12	GND	LI1-OE34	35
36	CCR 62	GND	CCR 63	DATA 12	GND	DATA 13	LI1-OE56	GND	LI1-OE78	36
37	CCR 70	GND	CCR 71	DATA 14	GND	DATA 15	LI2-OE12	GND	LI2-OE24	37
38	CCR 72	GND	CCR 73	EVT_IN0	GND	EVT_IN1	LI2-OE56	GND	LI2-OE78	38
39	CCR 80	GND	CCR 81	EVT_IN2	GND	EVT_IN3	AMD 0	GND	AMD 1	39
40	CCR 82	GND	CCR 83	SarocDtready 0	GND	SarocDtready 1	AMD 2	GND	AMD 3	40
41	Spare	GND	Spare	SarocEmpty 0	GND	SarocEmpty 1	MTOE12	GND	MTOE34	41
42	Spare	GND	Spare	Valack1	GND	Valack2	MTOE56	GND	MTOE78	42
43	Spare	GND	Spare	SAROCDtack	GND	Renin	MTOE1	GND	Spare	43
44	Spare	GND	Spare	RESET A_buf	GND	LPASS	Spare	GND	Spare	44
45	Latch_Card	GND	ADD1	GlobalReset	GND	R/W_buf	Anastrobe	GND	Vstrobe	45
46	ADD2	GND	ADD3	Valack3	GND	StartReadoutSaroc	Dload1	GND	Dload2	46
47	ADD4	GND	ADD5	LT_Reset	GND	Valack4	Spare	GND	Spare	47
48	ADD6	GND	ADD7	Valack5	GND	Conv_DTb	Spare	GND	Spare	48
49	+5 V	GND	+5 V	+5 V	GND	+5 V	+5 V	GND	+5 V	49
50	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	50
51	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	51
52	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	52
53	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	53
54	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	54
55	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	55
56	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	56

7.3. PPADC Cluster AP Description.(In progress)

• 1.1) AP1 :

- DCLKn **:** Clock signal to load the *DAC*s, this signal is common for the two channels *n* and *n+1* (see fig. *Dacs connections*).

- DDINn **:** serial data signal to load the *DACs*, this signal is common for the two channels *n* and *n+1* (see fig. *Dacs connections*).

- ASICDCSn **:** Chip Select signal to load the *ASIC DAC*s, there is one signal per ASIC Dac, n = 1 to 8 (see fig. *Dacs connections*).

- DACDCSn **:** Chip Select signal to load the individual *DAC*s, there is one signal per Dac, n = 1 to 8 (see fig. *Dacs connections*).

- CLKProm : serial PROM Clock signal of the *PPADC Analog* card.

- CSProm : serial PROM Chip Select signal of the *PPADC Analog* card.

- DProm_Write: serial PROM Data write to the *PPADC Analog* card.

- DProm_Read: serial PROM Data to be read out of the *PPADC Analog* card. (see E²Prom connection figure).

- CCRnm **:** Channel Control Register, each signal enable or disable a function on each channel of the *Analog* card; *n* is the channel number (1 to 8) and *m* the bit Register number. There are four registers per channel :

0 ==> en/dis* channel.
1 ==> en/dis* test generator channel.
2 ==> spare, free use.
3 ==> spare, free use.

- Latch_Card : This signal can be used to enable the data bus buffer on the *Analog* card. It is active, during a complete VME cycle, when the G.I.R. is selected

- ADD[7..1] : this is the lowest byte of the *VME* Address bus, it is enabled by the *LCA DECOD1*.

- Spare : these signals are not used in the *Euroball PPADC* card, they are controlled by the *LCA DECOD1*. They can be used by the *Analog* card for future applications.

- VPTAT1 : Voltage Proportional To Absolute Temperature signal of the sensor 1 from the *Analog* card and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER1 : high level temperature signal of the sensor 1 from the *Analog* card.

- UNDER1 : low level temperature signal of the sensor 1 from the *Analog* card.

- LED 1: display signal of a *LED* indicator driven by an open collector from *G.I.R*. to the front panel.

• 1.2) AP2 :

- 16 MHz: buffered *VME* System Clock signal.

- MRegn**:** 8 bits Module Register, each signal enable or disable a common function on the *Analog* card, *n* is the bit Register number.

0 ==> reject/mark* event on pileup.
1 ==> low/high* Timing Filter Amplifier gain.
2 ==> en/dis* Sliding Scale.
3 ==> high/zero* value fixed on Sliding Scale.
4, 5, 6, 7 ==> spare, free use.

- ADD[23..8] : these are the other 2 bytes of the *VME* Address bus, they are enabled by the *LCA DECOD1*.

- AIn **:** Analogue Inspection Lines, n is the inspection line indicator.

- DIn **:** Digital Inspection Lines, n is the inspection line indicator.

- VI : Voltage Inspection Line.

- DATA[15..0] : these are the lower sixteen bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *ASIC* and *FIFO* data bus during Readout mechanism.

- EVT_IN[3..0] : these lines are the current event number, they are given by the *MASTER Trigger* via the *VXI Local* bus to the Analog card during *Validation* (LBus [11..8]).

- R/W_buf : buffered *VME* read-write signal.

- Read [17..12,10..0] : these signals are spare signals for the internal Readout interface and are not defined until now in the *Euroball PPADC* card, they are controlled by the *LCA READOUT*. They will be defined later.

- SPARE : these signals are not used in the *Euroball PPADC* card, they are controlled by the *LCA DECODE2*. They can be defined for future applications.

- VPTAT2 : Voltage Proportional To Absolute Temperature signal of the sensor 2 from the *Analog* card and controlled by the *DSP* (via an *ADC*)(see fig. *Sensors connections*).

- OVER2 : high level temperature signal of the sensor 2 from the *Analog* card.

- UNDER2 : low level temperature signal of the sensor 2 from the *Analog* card.

- LED2 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

• 1.3) AP3 :

- DATA[31..16] : these are the sixteen higher bits of the *GIR* Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *ASIC* and *FIFO* data bus during Readout.

- EVT_OUT[3..0] : these lines are the event number that are sent with the data during acquisition mode, and are written in the *FIFO*.

- ReadOut [21..18] : these signals are dedicated for Readout interface and are not used in the *Euroball PPADC* card, they are controlled by the *LCA READOUT*. They can be defined for future applications.

- VETO : *Veto* signal given by the *BGO* card (shield) (this signal comes from the front panel for both the *Ge, & PPADC* boards, while for the *BGO* card this signal is generated from the internal mother Board).

- FT_ttl_buf : buffered *Fast Trigger* signal (positive TTL) from the *MASTER Trigger* (*starx* on the *VXI* back plane).

- Inhibit_buf : buffered *Inhibit* signal from the *MASTER Trigger* (on the *VXI* back plane).

- VAL_buf : buffered *Validation* signal from the *MASTER Trigger* (on the *VXI* back plane).

- FT_ECL -, FT_ECL+ : *Fast Trigger* signals (differential ECL) given by the *MASTER Trigger* (*starx* +/- on the *VXI* back plane). **These signals are not charged, the resistors MUST be placed on the Analog part.**

- FLAG1, 2, 3 : these signals are not used for the moment in *Euroball*. They can be used later as a connection between the *DSP*, and the *Analog* card. They are controlled by the *DSP*.

- LED3 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

All the signals below are controlled by the *LCA DECODE2*.

- AnaSelAn **:** select signal of the Analog multiplexers for the Analog Inspection Line 1, *n* is the multiplexer select bit (n = 0 to 3)(the multiplexers are the same which are used in *Eurogam* and are *TTL* input compatible).

- AnaSelBn **:** select signal of the Analog multiplexers for the Analog Inspection Line2, *n* is the multiplexer select bit (n = 0 to 3).

- AnEnAn **:** output enable signal of the Analog multiplexers for the Analog Inspection Line 1. There is one per multiplexer (4 are used for the PPADC Card).

- AnEnBn **:** output enable signal of the Analog multiplexers for the Analog Inspection Line . there is one per multiplexer (4 are used for the PPADC Card).

- DigSelAn **:** select signal of the digital multiplexers for the digital inspection line 1, *n* is the multiplexer select bit (n = 0 to 3).

- DigSelBn **:** select signal of the digital multiplexers for the digital inspection line 2, *n* is the multiplexer select bit (n = 0 to 3).

- DigOEAn**:** output enable signal of the digital multiplexers for the inspection line 1. There is one per multiplexer (4 are used for the PPADC Card).

- DigOEBn**:** output enable signal of the digital multiplexers for the inspection line 2. There is one per multiplexer (4 are used for the PPADC Card).

- VSel[3..0] : select bus of the voltage multiplexers. These signals must be common to all voltage multiplexers.

- Venablen **:** enable signal of the voltage multiplexers, 5 for the PPADC Card.

- Spare : these signals are not used in the *Euroball* PPADC Cards, they can be defined for future applications.

- Vstrobe: Strobe signal of all the voltage multiplexers.

- AnaStrobe: Strobe signal of all the Analog multiplexers.

- Dloadn**:** Strobe signal of digital multiplexers, n is digital inspection line number.

Pinouts of the AP Connector for the PPADC Cluster: (Table 4):

	AP1 Connector			AP2 Connector			AP3 Connector			
PIN NO.	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	PIN N
1	+5 V	VPTAT 1	+5 V	+5 V	VPTAT 2	+5 V	+5v	FLAG1	+5v	1
2	+5 V	+5v	+5 V	+5 V	+5v	+5 V	+5v	+5v	+5v	2
3	DCLK 1	OVER 1	DDIN 1	Spare	OVER 2	Spare	DATA 16	FLAG2	DATA 17	3
4	ASICDCS 1	UNDER 1	DCLK 2	Spare	UNDER 2	Spare	DATA 18	FLAG3	DATA 19	4
5	DDIN 2	LED 1	ASICDCS 2	Spare	LED 2	Spare	DATA 20	LED	DATA 21	5
6	DCLK 3	GND	DDIN 3	16 Mhz	GND	Spare	DATA 22	GND	DATA 23	6
7	ASICDCS 3	GND	DCLK 4	GND	GND	MReg0	GND	GND	GND	7
8	DDIN 4	GND	ASICDCS 4	ADD 8	GND	ADD 9	DATA 24	GND	DATA 25	8
9	DCLK 5	GND	DDIN 5	ADD 10	GND	ADD 11	DATA 26	GND	DATA 27	9
10	ASICDCS 5	GND	DCLK 6	ADD 12	GND	ADD 13	DATA 28	GND	DATA 29	10
11	DDIN 6	GND	ASICDCS 6	ADD 14	GND	ADD 15	DATA 30	GND	DATA 31	11
12	DCLK7	GND	DDIN 7	ADD 16	GND	ADD 17	GND	GND	GND	12
13	ASICDCS 7	GND	DCLK 8	ADD 18	GND	ADD 19	EVT_out0	GND	EVT_out1	13
14	DDIN 8	GND	ASICDCS 8	ADD 20	GND	ADD 21	EVT_out2	GND	EVT_out3	14
15	DACDS 1	GND	DACDS 2	ADD 22	GND	ADD 23	READ 18	GND	READ 19	15
16	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	16
17	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	17
18	DACDS 3	GND	DACDS 4	MReg 1	GND	MReg2	READ 20	GND	READ 21	18
19	DACDS 5	GND	DACDS 6	MReg 3	GND	MReg4	FT_ECL +	GND	VETO	19
20	DACDS 7	GND	DACDS 8	AI 1	GND	GND	GND	GND	FT_ECL -	20
21	Clk Prom	GND	Dprom_Write	GND	GND	GND	FT_ttl_buf	GND	Inhibit_buf	21
22	CS Prom	GND	DProm_Read	AI 2	GND	GND	VAL_buf	GND	AnaSelA 0	22
23	CCR 10	GND	CCR 11	GND	GND	DI 1	AnaSelA 1	GND	AnaSelA 2	23
24	CCR 12	GND	CCR 13	DI 2	GND	GND	AnaSelA 3	GND	AnaSelB 0	24
25	CCR 20	GND	CCR 21	MReg 5	GND	VI	AnaSelB 1	GND	AnaSelB 2	25
26	CCR 22	GND	CCR 23	MReg 6	GND	MReg7	AnaSelB 3	GND	AnEnA 1	26
27	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	27
28	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	28
29	CCR 30	GND	CCR 31	DATA 0	GND	DATA 1	AnEnA 2	GND	AnEnA 3	29
30	CCR 32	GND	CCR 33	DATA 2	GND	DATA 3	AnEnA 4	GND	AnEnB 1	30
31	CCR 40	GND	CCR 41	DATA 4	GND	DATA 5	AnEnB 2	GND	AnEnB 3	31
32	CCR 42	GND	CCR 43	DATA 6	GND	DATA 7	AnEnB 4	GND	DigselA 0	32
33	CCR 50	GND	CCR 51	GND	GND	GND	DigselA 1	GND	DigselA 2	33
34	CCR 52	GND	CCR 53	DATA 8	GND	DATA 9	DigselA3	GND	DigselB 0	34
35	CCR 60	GND	CCR 61	DATA 10	GND	DATA 11	DigselB 1	GND	DigselB 2	35
36	CCR 62	GND	CCR 63	DATA 12	GND	DATA 13	DigselB 3	GND	DigOEA 1	36
37	CCR 70	GND	CCR 71	DATA 14	GND	DATA 15	DigOEA 2	GND	DigOEA 3	37
38	CCR 72	GND	CCR 73	EVT_IN0	GND	EVT_IN1	DigOEA 4	GND	DigOEB 1	38
39	CCR 80	GND	CCR 81	EVT_IN2	GND	EVT_IN3	DigOEB 2	GND	DigOEB 3	39
40	CCR 82	GND	CCR 83	READ 0	GND	READ 1	DigOEB 4	GND	VSel 0	40
41	Spare	GND	Spare	READ 2	GND	READ 3	VSel 1	GND	Vsel 2	41
42	Spare	GND	Spare	READ 4	GND	READ 5	Vsel 3	GND	Venable 1	42
43	Spare	GND	Spare	READ 6_buf	GND	READ 7	Venable 2	GND	Venable 3	43
44	Spare	GND	Spare	READ 8_buf	GND	READ 9	Venable 4	GND	Venable 5	44
45	Latch_Card	GND	ADD1	READ 10_buf	GND	R/W_buf	Anastrobe	GND	Vstrobe	45
46	ADD2	GND	ADD3	READ 12	GND	READ 13	Dload1	GND	Dload2	46
47	ADD4	GND	ADD5	READ 14_buf	GND	READ 15	Spare	GND	Spare	47
48	ADD6	GND	ADD7	READ 16	GND	READ 17	Spare	GND	Spare	48
49	+5 V	GND	+5 V	+5 V	GND	+5 V	+5 V	GND	+5 V	49
50	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	50
51	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	51
52	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	52
53	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	53
54	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	54
55	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	55
56	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	56

8 Memory Map of the G.I.R. for the BGO Card

8.1 VXI Configuration Registers: (Inside the G.I.R.)

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11).

***VXI Base Address** first card*	***Description***	***DATA Format***
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8a	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

8.2 Channel Area Addresses

Channel 1 (0x1000 --0x10FE)	**Bus Width**	**Read/ Write**	**Function**
0x1000	16	w	Dac Adjustment no.1
0x1002	16	r/w	Channel Control Register 2 bits (bit0= enable/disable*) (bit1= set/reset*)
Channel 2 (0x1100 --0x11FE)	**16**	**r/w**	**Function**
0x1100	16	w	Dac Adjustment no.2
0x1102	16	r/w	Channel Control Register 2 bits (bit0= enable/disable*) (bit1= set/reset*)
Channel 20 (0x2300 --0x23FE)	**16**	**(r/w)**	**Function**
0x2300	16	w	Dac Adjustment no.20
0x2302	16	r/w	Channel Control Register 2 bits (bit0= enable/disable*) (bit1= set/reset*)

8.3 Common Area Addresses

8.3.1 Common DACs:

VME Address	Bus Width	R/W	Function
0x2400	16	w	FT Sample Adjustment
0x2500	16	w	ValSample Adjustment
0x2600	16	w	VETO Adjustment
0x2700	16	w	Spare Dac

8.3.2 Common Registers:

Global Addresses	Bus Width	Read/ Write	Function
0x10	16	r/w	Module Control Register (MCR)
0x20	16	r/w	Digital Inspection 1 channel select
0x22	16	r/w	Digital Inspection 1 parameter Select
0x24	16	r/w	Digital Inspection 2 channel select
0x26	16	r/w	Digital Inspection 2 parameter Select
0x28	16	r/w	Analog Inspection 1 channel select
0x2A	16	r/w	Analog Inspection 1 parameter Select
0x2C	16	r/w	Analog Inspection 2 channel select
0x2E	16	r/w	Analog Inspection 2 parameter Select
0x30	16	r/w	Voltage Inspection channel select
0x32	16	r/w	Voltage Inspection parameter Select
0x40--0x5E	16	r/w	Analogue Card Configuration Registers (XCProm)
0x60--0x70	16	r/w	Default DAC Buffer values in XCProm for non volatile mode
0x80--0x90	16	w only	Change Default DAC Buffer mode in Volatile mode
0xA0--0xBE	16/32	r/w	G.I.R. Readout Memory Map
0x100--0x17C	32	r/w	Saroc 1 Setup

0x180--0x1FC	32	r/w	Saroc 2 Setup
0x200--0x27C	32	r/w	Saroc 3 Setup
0x280-0x2FC	32	r/w	Saroc 4 Setup

8.3.2.1 Module Control Register: VME base Address : 0x10

Bit Number	Meaning when = 0	Meaning when = 1
0	not yet defined	not yet defined
1	not yet defined	not yet defined
2	Sliding Scale Counter Off	Sliding Scale Counter On
3	If SS off, force SS DAC to 0V	If SS on, force SS DAC to 9V
4	Analog Card PROM Write Disable	Analog Card PROM Write Enable
5	not yet defined	not yet defined
6	not yet defined	not yet defined
7	not yet defined	not yet defined
8	Reset FIFO Disable	FIFO Reset
9	Reset G.I.R. Disable	G.I.R. Reset
10	Not Last Card	Last Card (use terminators)
11	not yet defined	not yet defined
12	not yet defined	not yet defined
13	not yet defined	not yet defined
14	not yet defined	not yet defined
15	not yet defined	not yet defined

8.3.2.2 Digital inspection lines:

Digital Inspection line 1 : VME base Address : 0x20 (channel Select), and 0x22 (parameter Select)
To Disable the Digital inspection Line 1 write 0x00 at address 0x22. DigselA[5..0]
Digital Inspection line 2 : VME base Address : 0x24 (channel Select), and 0x26 (parameter Select).
To Disable the Digital inspection Line 2 write 0x00 at address 0x26. DigselB[5..0]

parameters Line1 = DigselA[5..0] Line2 = DigselB[5..0]	GIR Control Lines to Analogue Card DigselA[2..0] DigselB[2..0]	GIR Control Lines to Analogue Card DigselA[5..3] DigselB[5..3]	Data Value for channel Address	Data Value for Parameter Address
Disable	xxx	110	xxxx	00
TACS Channel 1 to 8	000..111	000	0x 00 to 0x07	01
TACS Channel 9 to g	000..111	010	0x08 to 0x0F	01
TACS Channel h, j, k	000..010	100	0x10 to 0x12	01
TACOR	011	100	0x 13	01
FTRINT	100	100	0x14	01
FTSAM	101	100	0x15	01
VALSAM	110	100	0x16	01
VETO	111	100	0x17	01
SEDO1 to 8	000..111	001	0x00 to 0x07	02
SEDO9 to g	000..111	011	0x08 to 0x0F	02
SEDOh, j, k,m	000..011	101	0x10 to 0x13	02
G.I.R. Parameters	**GIR Control Lines**		**Data Value for channel Address**	**Data Value for Parameter Address**
Fast_Trigger	0x001		0x 20	0x001
Inhibit	0x002		0x 20	0x002
Validation	0x003		0x 20	0x003
Veto	0x004		0x 20	0x004
OrValack	0x005		0x 20	0x005
OrDeadTime	0x006		0x 20	0x006
StartReadoutSAROC	0x007		0x 20	0x007
Renin (SAROC)	0x008		0x 20	0x008
SAROCDTready0	0x009		0x 20	0x009
SAROCDTready1	0x00A		0x 20	0x00A
SAROCDTready2	0x00B		0x 20	0x00B
SAROCDTready3	0x00C		0x 20	0x00C
SAROCDTack_buf	0x00D		0x 20	0x00D
SAROCEmpty0	0x00E		0x 20	0x00E
SAROCEmpty1	0x00F		0x 20	0x00F
SAROCEmpty2	0x010		0x 20	0x010
SAROCEmpty3	0x011		0x 20	0x011
SAROCLPASS	0x012		0x 20	0x012
CSA *(FifoChipSelect_A)	0x013		0x 20	0x013
CLKA(FifoClock_A)	0x014		0x 20	0x014

ENA(Fifo Enable Port_A)	0x015		0x 20	0x015
AS* (VME)	0x016		0x 20	0x016
DS (DS0* and DS1*) (VME)	0x017		0x 20	0x017
R/W* (VME)	0x018		0x 20	0x018
ModRoco	0x019		0x 20	0x019
CardRenin *(From ROCO)	0x01A		0x 20	0x01A
BLTACK (Card)	0x01B		0x 20	0x01B
BLTACK (Bus)	0x01C		0x 20	0x01C
OE_Ident*	0x01D		0x 20	0x01D
CSB* (FifoChipSelect_B)	0x01E		0x 20	0x01E
CLKB (FifoClock_B)	0x01F		0x 20	0x01F
ENB (Fifo Enable Port_B)	0x020		0x 20	0x020
OR_fifo (EmptyFlag)	0x021		0x 20	0x021
FDTACK	0x022		0x 20	0x022
DTACK* (VME)	0x023		0x 20	0x023
CardRenout(Bus Renout)	0x024		0x 20	0x024
SysClk	0x025		0x 20	0x025
LT_Reset*	0x026		0x 20	0x026
Reset_A*	0x027		0x 20	0x027
Reset_Fifo*	0x028		0x 20	0x028
Decode_Sel(CardChipSelect)	0x029		0x 20	0x029
Strobe_Dec2	0x02A		0x 20	0x02A
Dclk	0x02B		0x 20	0x02B
DCS*	0x02C		0x 20	0x02C
DDin	0x02D		0x20	0x02E

8.3.2.3 Analog inspection lines:

Analog Inspection line 1 : VME base Address: 0x28 (channel Select), & 0x2A (parameter Select).
To Disable the Analog inspection Line 1 write 0x00 at address 0x2A.
Analog Inspection line 2 : VME base Address: 0x2C (channel Select), & 0x2E (parameter Select).
To Disable the Analog inspection Line 2 write 0x00 at address 0x2E.

Parameters Line1 = AnaselA, AnEnA Line2 = AnaselB, AnEnB	GIR Control Lines to Analogue Card AnaselA[3..0] AnaselB[3..0]	GIR Control Lines to Analogue Card AnEnA[3..1] AnEnB[3..1]	Data Value for channel Address	Data Value for Parameter Address
TAO1 to 8	0000..0111	001	0x00 to 0x07	01
TAO9 to g	0000..0111	010	0x08 to 0x0F	01
TAOh, j, k,m	0000..0011	100	0x10 to 0x13	01
SUMO	0100	100	0x14	01
0V	0101	100	0x15	01
GIO1 to 8	1000..1111	001	0x00 to 0x07	02
GIO9 to g	1000..1111	010	0x08 to 0x0F	02
GIOh, j, k	1000..1010	100	0x10 to 0x12	02
GISum	1011	100	0x13	02

8.3.2.4 Voltage inspection line:

VME base Address : 0x30 (channel select), and 0x32 (parameter select).
To Disable the Voltage Inspection line : write 0x00 at address 0x32

parameters	GIR Control Lines to Analogue Card Vsel[3..0]	GIR Control Lines to Analogue Card Venable[2..1]	Data Value for channel Address	Data Value for Parameter Address
Discr. Thr. 1 to g	0000..1111	01	0x00 to 0x0F	01
Discr. Thr. h, j, k,m	0000..0011	10	0x10 to 0x13	01
FTRSPC	0100	10	0x14	01
VALSPC	0101	10	0x15	01
VETOC	0110	10	0x16	01
DAC24	0111	10	0x17	01
SLSCV	1000	10	0x18	01
+2.5 V	1001	10	0x19	01
0V	1010	10	0x1A	01

8.3.2.5 BGO Configuration Registers (Analogue part):

VXI Base Address	***Description***	***DATA Format***
0x40	In Read Mode this is the Man. ID	D7..D0 from XCPROM
0x42		
0x44		

0x46		
0x48	Read Only: Serial no.	Read 8 bits only from XCPROM d7 to d0
0x4a	Read Only: Modification Level	Read 8 bits only from XCPROM d7 to d0

8.3.2.6 BGO DAC Buffer Control Memory Map (non volatile):

Base Addresses	Bus Width	Read/ Write	Function
0x60	16	r/w	Default DAC Buffer **1** values from XCProm
0x62	16	r/w	Default DAC Buffer **2** values from XCProm
0x64	16	r/w	Default DAC Buffer **3** values from XCProm

8.3.2.7 BGO DAC Buffer Setup Memory Map (volatile):

Base Addresses	Bus Width	Read/ Write	Function
0x80	16	write only	Change Default DAC Buffer **1** mode in XCProm
0x82	16	write only	Change Default DAC Buffer **2** mode in XCProm
0x84	16	write only	Change Default DAC Buffer **3** mode in XCProm

8.3.2.8 G.I.R. Readout Memory Map : VME base Address : 0xA0 to 0xBE.

Base Addresses	Bus Width	Read/ Write	Function
0xA0	16	r/w	Event Counter Register
0xA2	16	r/w	Item + Group no. Register
0xA0	32	read only	Item + Group no. Register + Event Counter
0xA4	32	r/w	Fifo Test Enable
0xA8	16	r/w	G.I.R. Readout Control Register
0xAA	N.A.	r only w only	Start Readout Saroc in test mode End Readout Saroc in test mode
0xAC	16	r only	Readout, Temperature Status Register
0xAE to 0xBE	N.A.	r/w	Not yet Implemented

8.3.2.8.1 G.I.R. Readout Control Register (*not fixed*): VME base Address : 0xA8 to be upgraded

Bit Number	Meaning when = 0	Meaning when = 1
0	Run mode for SAROC readout	Test mode for SAROC readout
1	Run mode for External readout	Test mode for External readout
2	Disable Valack Timeout Reset	Enable Valack Timeout Reset
3	Not yet defined	Not yet defined
4	Not yet defined	Not yet defined
5	no pipelining at all (dead until VXI Readout ends)	Pipeline Readout stage (dead until data are in FIFO)
6	Event Number Readout off	Event Number Readout on
7	Readout mode 0	Readout mode 1
8	DSP set to Slave Mode	DSP set to Master Mode
9	DSP Slave is not last Slave Card	DSP Slave is the last Slave Card
10	Contrôle des fenêtres off	Contrôle des fenêtres on
11	Event Number Q = 00	Event Number Q = 11
12	Not yet defined	Not yet defined
13	Not yet defined	Not yet defined
14	Not yet defined	Not yet defined
15	Not yet defined	Not yet defined

8.3.2.8.2 G.I.R. Readout Status Register (*not fixed*): VME base Address : 0xAC

Bit Number	Meaning when = 0	Meaning when = 1
0	G.I.R. Temperature indicator is above the upper threshold	G.I.R. Temperature indicator is below the upper threshold
1	G.I.R. Temperature indicator is below the lower threshold	G.I.R. Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Valack Timeout deasserted	Valack Timeout asserted
8	Empty Flag of Fifo1 asserted	Empty Flag for Fifo1 deasserted
9	Full Flag of Fifo1 asserted	Full Flag for Fifo1 deasserted
10	Empty Flag of Fifo2 asserted	Empty Flag for Fifo2 deasserted
11	Full Flag of Fifo2 asserted	Full Flag for Fifo2 deasserted

12	Global Saroc_Empty asserted	Global Saroc_Empty deasserted
13	Status: No fault	Status: fault 0
14	Status: No fault	Status: fault 1
15	Status: No fault	Status: fault 2

9 Memory Map of the G.I.R. for the Ge Card

9.1 VXI Configuration Registers: (Inside the G.I.R.)

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11).

VXI Base Address *(slot 1)*	***Description***	***DATA Format***
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8a	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

9.2 Channel Area Addresses

Channel 1 (0x1000 --0x10FE)	**Bus Width**	**Read/ Write**	**Function**
0x1000	16	w	Dac Adjustment no.1 (see Dac Memory Map below)
0x1010	16	r/w	Channel Control Register 4 bits (bit0= enable/disable*, bit1= Test Gen. enable/disable*,bit2 & 3 free)
Channel 2 (0x1100 --0x11FE)	**16**	**r/w**	**Function**
0x1100	16	w	Dac Adjustment no.2(see Dac Memory Map below
0x1110	16	r/w	Channel Control Register 4 bits
Channel 8 (0x1700 --0x17FE)	**16**	**(r/w)**	**Function**
0x1700	16	w	Dac Adjustment no.8(see Dac Memory Map below
0x1710	16	r/w	Channel Control Register 4 bits

9.2.1 DAC Memory Map:

This applies to all channel DAC setup for Address 0x1000 to 0x100e , and 1100 to 110e (channel 1&2) up to (channel 7& 8), because every two channels share two DACs A&B.

Channel 1 (0x1000 --0x10FE)	**DAC A/B**	**G.I.R. DAC parameter Value**	**DAC Parameter Name**
0x1000	A	0	CFD Threshold channel 1
0x1002	A	4	CFD Output DELAY Channel 1
0x1004	A	2	PZ Threshold Channel 1
0x1006	A	6	FT Sample Threshold Channel 1
0x1008	B	0	Val Threshold Channel 1
0x100a	B	4	Pileup Threshold Channel 1
0x100c	B	2	WatchDog Threshold Channel 1
0x100e	B	6	Bipolar Cross over Channel 1
0x1100	A	1	CFD Threshold channel 2
0x1102	A	5	CFD Output DELAY Channel 2
0x1104	A	3	PZ Threshold Channel 2
0x1106	A	7	FT Sample Threshold Channel 2
0x1108	B	1	Val Threshold Channel 2
0x110a	B	5	Pileup Threshold Channel 2
0x110c	B	3	WatchDog Threshold Channel 2
0x110e	B	6	Bipolar Cross over Channel 1

9.2.2 DAC Memory Map:

This Table shows the hardware parameter's list of the DACs parameters w.r.t. their effective position.

Channel 1 (0x1000 --0x10FE)	**DAC A/B**	**G.I.R. DAC parameter Value**	**DAC Parameter Name**
0x1000	A	0	CFD Threshold channel 1
0x1100	A	1	CFD Threshold channel 2
0x1004	A	2	PZ Threshold Channel 1
0x1104	A	3	PZ Threshold Channel 2

0x1002	A	4	CFD Output DELAY Channel 1
0x1102	A	5	CFD Output DELAY Channel 2
0x1006	A	6	FT Sample Threshold Channel 1
0x1106	A	7	FT Sample Threshold Channel 2
0x1008	B	0	Val Threshold Channel 1
0x1108	B	1	Val Threshold Channel 2
0x100c	B	2	WatchDog Threshold Channel 1
0x110c	B	3	WatchDog Threshold Channel 2
0x100a	B	4	Pileup Threshold Channel 1
0x110a	B	5	Pileup Threshold Channel 2
0x100e	B	6	Bipolar Cross over Channel 1
0x110e	B	7	Bipolar Cross over Channel 2

9.3 Common Area Addresses

9.3.1 Common DACs:

VME Address	Bus Width	R/W	Function
0x0000	16	w	CFD Width Adjustment
0x0002	16	w	Test Generator amplitude Adjustment

9.3.2 Common Registers:

Global Addresses	Bus Width	Read/ Write	Function
0x10	16	r/w	Module Control Register (MCR)
0x20	16	r/w	Digital Inspection 1 channel select
0x22	16	r/w	Digital Inspection 1 parameter Select
0x24	16	r/w	Digital Inspection 2 channel select
0x26	16	r/w	Digital Inspection 2 parameter Select
0x28	16	r/w	Analog Inspection 1 channel select
0x2A	16	r/w	Analog Inspection 1 parameter Select
0x2C	16	r/w	Analog Inspection 2 channel select
0x2E	16	r/w	Analog Inspection 2 parameter Select
0x30	16	r/w	Voltage Inspection channel select
0x32	16	r/w	Voltage Inspection parameter Select
0x40--0x5E	32	r/w	Test acces to data FIFO
0x60--0x70	16	r only	Read Default DAC Buffer values from XCProm
0x60--0x70	16	w only	Set Default DAC Buffer Values in XCPROM for non volatile mode
0x80--0x90	16	w only	Change Default DAC Buffer Setup in Volatile mode
0xA0--0xBE	16/32	r/w	Readout Setup
0x100--0x17C	32	r/w	Saroc 1 Setup
0x180-0x1FC	32	r/w	Saroc 2 Setup

9.3.2.1 Module Control Register: VME base Address : 0x10 **a vérifier avec Nab**

Bit Number	Meaning when = 0	Meaning when = 1
0	Mark Pileup & Veto Events	Reject Pileup & Veto Events
1	TFA Gain setting X 1	TFA Gain setting X 3
2	Sliding Scale Counter Off	Sliding Scale Counter On
3	If SS off, force SS DAC to 0V	If SS on, force SS DAC to 9V
4	Not Allocated	Not Allocated
5	Pipeline Off (dead until data in STR8080)	Pipeline On (dead until data in GIR FIFO)
6	Event Number Readout On	Event Number Readout Off
7	Common Deadtime Readout	Parallel Readout
8	Reset FIFO Disable	Reset FIFO
9	Reset G.I.R. Disable	G.I.R. Reset
10	Not Last Card	Last Card (use terminators)
11	Not Allocated	Not Allocated
12	Not Allocated	Not Allocated
13	Not Allocated	Not Allocated
14	Event Number Q set by 0x12	Use real Event Number Q
15	Status: FIFO empty	Status: FIFO not empty

9.3.2.2 Digital inspection lines:

Digital Inspection line 1 : VME base Address : 0x20 (channel Select), and 0x22 (parameter Select)
To Disable the Digital inspection Line 1 write 0x00 at address 0x22. LI1_OEx-x+1[3..0]
Digital Inspection line 2 : VME base Address : 0x24 (channel Select), and 0x26(parameter Select).

<u>To Disable the Digital inspection Line 2 write 0x00 at address 0x26.</u> LI2_OEx-x+1[3..0]

parameters Line1 = LI1_OEx-x+1[3..0] Line2 = LI2_OEx-x+1[3..0]	**GIR Control Lines to Analogue Card SRCELI [3..0]**	**GIR Control Lines to Analogue Card LI1-OEx-x+1[3..0] LI2-OEx-x+1[3..0]**	**GIR Control Lines MUX_CH_SEL**	**Data Value for channel Address**	**Data Value for Parameter Address**
Disable	0x0	0x0	1	0x00	xx
End of FlatTop(Shap.Amp.)1	0x1	0x1	0	0x01	0x01
LT Reset output 1	0x2	0x1	0	0x01	0x02
FT sample 1	0x3	0x1	0	0x01	0x03
Val sample 1	0x4	0x1	0	0x01	0x04
4MeV serial D out of ADC 1	0x5	0x1	0	0x01	0x05
Tac Reset (Start TAC) 1	0x6	0x1	0	0x01	0x06
Valack 1	0x7	0x1	0	0x01	0x07
Pre-pulse Pileup Indicator 1	0x8	0x1	0	0x01	0x08
Convert input to ADC 1	0x9	0x1	0	0x01	0x09
ADC Clock 1	0xA	0x1	0	0x01	0x0A
CFD Delayed 1	0xB	0x1	0	0x01	0x0B
CFD Direct 1	0xC	0x1	0	0x01	0x0C
End of FlatTop(Shap.Amp.)2	0x1	0x1	1	0x02	0x01
LT Reset output 2	0x2	0x1	1	0x02	0x02
FT sample 2	0x3	0x1	1	0x02	0x03
Val sample 2	0x4	0x1	1	0x02	0x04
4MeV serial D out of ADC 2	0x5	0x1	1	0x02	0x05
Tac Reset (Start TAC) 2	0x6	0x1	1	0x02	0x06
Valack 2	0x7	0x1	1	0x02	0x07
Pre-pulse Pileup Indicator 2	0x8	0x1	1	0x02	0x08
Convert input to ADC 2	0x9	0x1	1	0x02	0x09
ADC Clock 2	0xA	0x1	1	0x02	0x0A
CFD Delayed 2	0xB	0x1	1	0x02	0x0B
CFD Direct 2	0xC	0x1	1	0x02	0x0C
Channel 3 & 4 same values	see above	0x2	see above	0x03 to 0x04	see above
Channel 5 & 6 same values	see above	0x4	see above	0x05 to 0x06	see above
Channel 7 & 8 same values	see above	0x8	see above	0x07 to 0x08	see above
Not Used all Chan(Disable)	0x0	0x0	x	0x01 to 0x08	0x0D to 0x1F
G.I.R. Global Parameters	**GIR Control Lines**			**Data Value for channel Address**	**Data Value for parameter Address**
Disable				*0x20*	*0x000*
Fast_Trigger	0x001			0x20	0x001
Inhibit_buf (M.T.)	0x002			0x20	0x002
Validation	0x003			0x20	0x003
Veto	0x004			0x20	0x004
OrValack	0x005			0x20	0x005
Conversion DTime (coding)	0x006			0x20	0x006
StartReadoutSAROC	0x007			0x20	0x007
Renin (SAROC)	0x008			0x20	0x008
SAROCDTready0	0x009			0x20	0x009
SAROCDTready1	0x00A			0x20	0x00A
OR8CFD-Delay	0x00B			0x20	0x00B
Inhibit Card	0x00C			0x20	0x00C
SAROCDTack_buf	0x00D			0x20	0x00D
SAROCEmpty0	0x00E			0x20	0x00E
SAROCEmpty1	0x00F			0x20	0x00F
Readout Event Fault	0x010			0x20	0x010
Readout Event No. Match	0x011			0x20	0x011
SAROCLPASS	0x012			0x20	0x012
CSA *(FifoChipSelect_A)	0x013			0x20	0x013
CLKA(FifoClock_A)	0x014			0x20	0x014
ENA(Fifo Enable Port_A)	0x015			0x20	0x015
AS* (VME)	0x016			0x20	0x016
DS (DS0* and DS1*) (VME)	0x017			0x20	0x017
R/W* (VME)	0x018			0x20	0x018
ModRoco	0x019			0x20	0x019
CardRenin *(From ROCO)	0x01A			0x20	0x01A
BLTACK (Card)	0x01B			0x20	0x01B
BLTACK (Bus)	0x01C			0x20	0x01C
OE_Ident*	0x01D			0x20	0x01D
CSB* (FifoChipSelect_B)	0x01E			0x20	0x01E
CLKB (FifoClock_B)	0x01F			0x20	0x01F
ENB (Fifo Enable Port_B)	0x020			0x20	0x020

OR_fifo (EmptyFlag)	0x021			0x20	0x021
FDTACK	0x022			0x20	0x022
DTACK* (VME)	0x023			0x20	0x023
CardRenout(Bus Renout)	0x024			0x20	0x024
SysClk	0x025			0x20	0x025
LT_Reset*	0x026			0x20	0x026
Reset from Readout logic	0x027			0x20	0x027
Reset_Fifo*	0x028			0x20	0x028
DecodeSel(CardChipSelect)	0x029			0x20	0x029
Strobe_Dec2	0x02A			0x20	0x02A
Dclk	0x02B			0x20	0x02B
DCS*	0x02C			0x20	0x02C
DDin	0x02D			0x20	0x02D
No Readout match in last 16	0x02E			0x20	0x02E
Not Used (DI Disable)	Disable			0x20	0x002F to 0xFFFF

9.3.2.3 Analog inspection lines:

Analog Inspection line 1 : VME base Address: 0x28 (channel Select), & 0x2A (parameter Select).
To Disable the Analog inspection Line 1 write 0x00 at address 0x28. AID[3..0], AI1-OEx_x+1[3..0]
Analog Inspection line 2 : VME base Address : 0x2C (channel Select), and 0x2E (parameter Select).
To Disable the Analog inspection Line 2 write 0x00 at address 0x2C. AID[7..4], AI2-OEx-x+1[3..0]

Parameters for channel 1 & 2	GIR Control Lines to Analogue Card AID [3..0] AID [7..4]	GIR Control Lines to Analogue Card AI1-OEx-x+1 [3..0] AI2-OEx-x+1 [3..0]	Data Value for channel Address	Data Value for Parameter Address
4 MeV energy 1	1111	0001	0x01	00
20 MeV energy 1	1110	0001	0x01	01
Bip. Sig for Peak tim. 1	1101	0001	0x01	02
TFA output 1	1100	0001	0x01	03
TAC output 1	1011	0001	0x01	04
FT ramp 1	1010	0001	0x01	05
VAL ramp 1	1001	0001	0x01	06
Pre-amp Sig (1st Buf) 1	1000	0001	0x01	07
4 MeV energy 2	0111	0001	0x02	00
20 MeV energy 2	0110	0001	0x02	01
Bip. Sig for Peak tim. 2	0101	0001	0x02	02
TFA output 2	0100	0001	0x02	03
TAC output 2	0011	0001	0x02	04
FT ramp 2	0010	0001	0x02	05
VAL ramp 2	0001	0001	0x02	06
Pre-amp Sig (1st Buf) 2	0000	0001	0x02	07
Not used(Disable) 1 & 2	0111	0000	xxxx	08 to FF

For the others channels, the AI1-OE [3..0] lines are changed :

AI1-OE [3..0], AI2-OE [3..0] = 0x0010 for the channels 3 - 4
AI1-OE [3..0], AI2-OE [3..0] = 0x0100 for the channels 5 - 6
AI1-OE [3..0], AI2-OE [3..0] = 0x1000 for the channels 7 - 8

9.3.2.4 Voltage inspection line:

VME base Address : 0x30 (channel select), and 0x32 (parameter select).
To Disable the Voltage Inspection line : write 0x00 at address 0x30.

parameters	GIR Control Lines to Analogue Card AMD [3..0]	GIR Control Lines to Analogue Card MTOEx-x+1 [3..0]	Data Value for Channel Address	Data Value for Parameter Address
CFD Threshold 1	0000	0001	0x01	00
CFD Threshold 2	0001	0001	0x02	00
CFD out delay Thres. 1	0010	0001	0x01	01
CFD out delay Thres. 2	0011	0001	0x02	01
PZ Adjustment 1	0100	0001	0x01	02
PZ Adjustment 2	0101	0001	0x02	02
FT SampleThreshold 1	0110	0001	0X01	03
FT SampleThreshold 2	0111	0001	0x02	03
Val Sample Threshold 1	1000	0001	0x01	04
Val Sample Threshold 2	1001	0001	0x02	04
Watchdog Timer Thres. 1	1010	0001	0x01	05
Watchdog Timer Thres. 2	1011	0001	0x02	05
Pileup Threshold 1	1100	0001	0x01	06

Pileup Threshold 2	1101	0001	0x02	06
Bip. Crossover Thres. 1	1110	0001	0x01	07
Bip. Crossover Thres. 2	1111	0001	0X02	07
Not used (Disable) 1	xxxx	0000	0x01	08 to 0F
Not used (Disable) 2	xxxx	0000	0x02	08 to 0F
Same Values **Same Values** **Same Values**	See upper See upper See upper	0010 0100 1000	0x03 to 0x04 0x05 to 0x06 0x07 to 0x08	See upper See upper See upper
Global parameters	**GIR Control Lines to Analogue Card AMD [3..0]**	**GIR Control Lines to Analogue Card MTOE 1**	**Data Value for Channel Address**	**Data Value for Parameter Address**
Vee 24	0000	1	0x09	0x10
Vee 18	0001	1	0x09	0x11
Vee 12	0010	1	0x09	0x12
Vee 5.2	0011	1	0x09	0x13
Vee 5 Analogue	0100	1	0x09	0x14
Vee 2	0101	1	0x09	0x15
0 v	0110	1	0x09	0x16
Vcc 5 Analogue	0111	1	0x09	0x17
Vcc 5	1000	1	0x09	0x18
Vcc 12	1001	1	0x09	0x19
Vcc 18	1010	1	0x09	0x1A
Vcc 20	1011	1	0x09	0x1B
Vcc24	1100	1	0x09	0x1C
Test Generator Level	1101	1	0x09	0x1D
CFD Width	1110	1	0x09	0x1E
0 v	1111	1	0x09	0x1F
Not used (Disable)	xxxx	0	0x09	0x20 to 0xFFFF

9.3.2.5 Ge Configuration Registers (Analogue part):

VXI Base Address	*Description*	*DATA Format*
0x40	In Read Mode this is the Man. ID	D7..D0 from XCPROM
0x42		
0x44		
0x46		
0x48	Read Only: Serial no.	Read 8 bits only from XCPROM d7 to d0
0x4a	Read Only: Modification Level	Read 8 bits only from XCPROM d7 to d0

9.3.2.6 Ge DAC Buffer Control Memory Map (non volatile):

Base Addresses	Bus Width	Read/ Write	Function
0x60	16	r/w	Default DAC Buffer **1** values from XCProm
0x62	16	r/w	Default DAC Buffer **2** values from XCProm
0x64	16	r/w	Default DAC Buffer **3** values from XCProm
0x66	16	r/w	Default DAC Buffer **4** values from XCProm
0x68	16	r/w	Default DAC Buffer **5** values from XCProm
0x6A	16	r/w	Default DAC Buffer **6** values from XCProm
0x6C	16	r/w	Default DAC Buffer **7** values from XCProm
0x6E	16	r/w	Default DAC Buffer **8** values from XCProm
0x70	16	r/w	Default DAC Buffer **Common parameters** from XCProm

9.3.2.7 Ge DAC Buffer Setup Memory Map (volatile):

Base Addresses	Bus Width	Read/ Write	Function
0x80	16	write only	Change Default DAC Buffer **1** mode in XCProm
0x82	16	write only	Change Default DAC Buffer **2** mode in XCProm
0x84	16	write only	Change Default DAC Buffer **3** mode in XCProm
0x86	16	write only	Change Default DAC Buffer **4** mode in XCProm
0x88	16	write only	Change Default DAC Buffer **5** mode in XCProm
0x8A	16	write only	Change Default DAC Buffer **6** mode in XCProm
0x8C	16	write only	Change Default DAC Buffer **7** mode in XCProm
0x8E	16	write only	Change Default DAC Buffer **8** mode in XCProm
0x90	16	write only	Change Default DAC Buffer **Common parameters** mode in XCProm

9.3.2.8 G.I.R. Readout Memory Map : VME base Address : 0xA0 to 0xBE.

Base Addresses	Bus Width	Read/ Write	Function

0xA0	16	r/w	Event Counter Register
0xA2	16	r/w	Item + Group no. Register
0xA0	32	read only	Item + Group no. + Event Counter
0xA4	32	r/w	Fifo Test Enable
0xA8	16	r/w	G.I.R. Readout Control Register
0xAA	N.A.	r only w only	Start Readout Saroc in test mode End Readout Saroc in test mode
0xAC	16	r only	Readout, Temperature Status Register
0xAE to 0xBE	N.A.	r/w	Not yet Implemented

9.3.2.8.1 <u>G.I.R. Readout Control Register (*not fixed*):</u> VME base Address : 0xA8

Bit Number	Meaning when = 0	Meaning when = 1
0	Run mode for SAROC Readout	Test mode for SAROC Readout
1	Run mode for External Readout	Test mode for External Readout
2	Disable Valack Timeout Reset	Enable Valack Timeout Reset
3	Not yet defined	Not yet defined
4	Not yet defined	Not yet defined
5	no pipelining at all (dead until data in STR8080)	Pipeline Readout stage (dead until data are in GIR FIFO)
6	Event Number Readout On	Event Number Readout Off
7	Common deadtime Readout	Parallel Readout
8	DSP set to Slave Mode	DSP set to Master Mode
9	DSP Slave is not last Slave Card	DSP Slave is the last Slave Card
10	Contrôle des fenêtres off	Contrôle des fenêtres on
11	Event Number Q set by 0x12	Use real Event Number Q
12	Not yet defined	Not yet defined
13	Not yet defined	Not yet defined
14	Not yet defined	Not yet defined
15	Not yet defined	Not yet defined

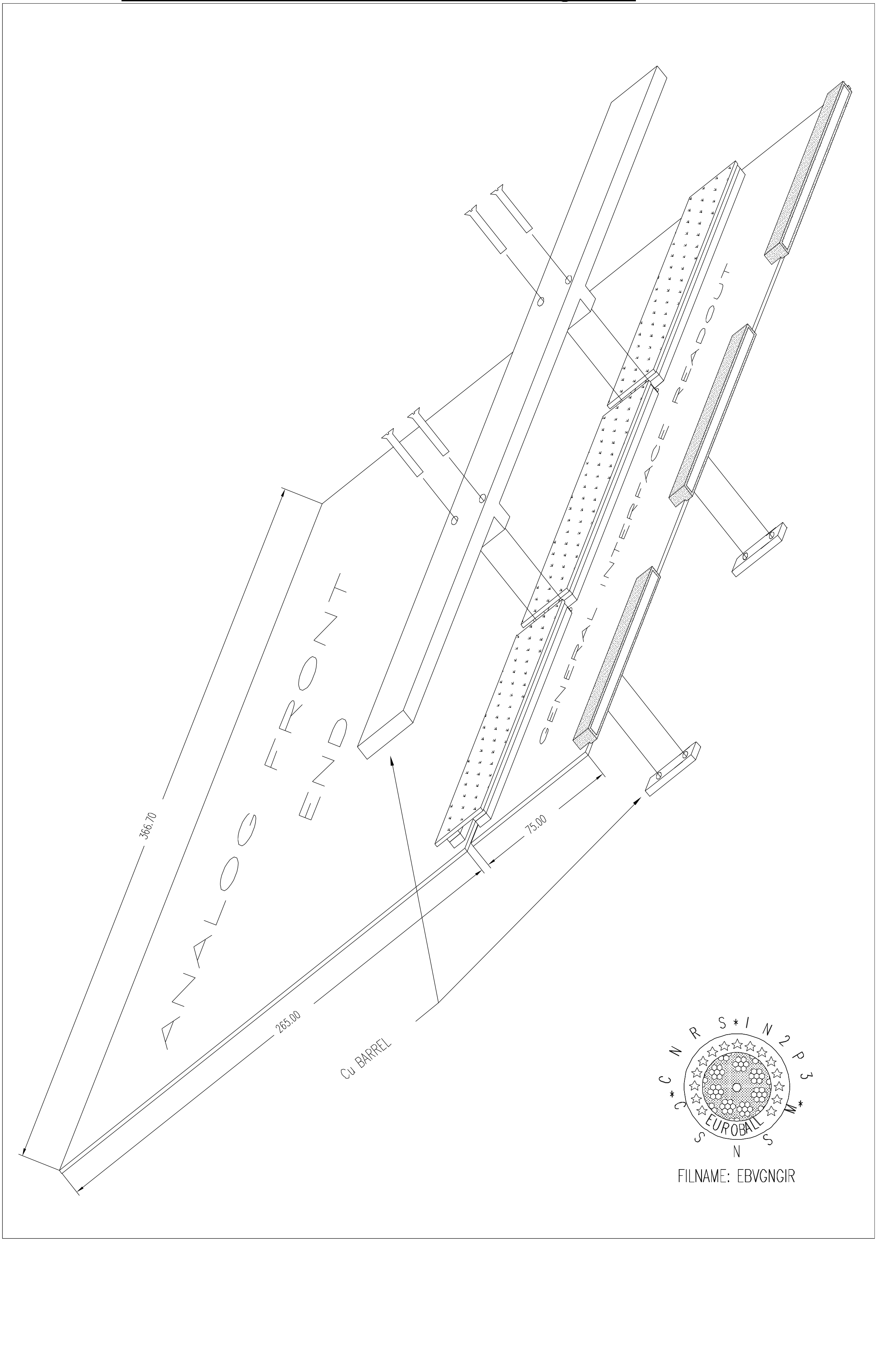
9.3.2.8.2 <u>G.I.R. Readout Status Register (*not fixed*):</u> VME base Address : 0xAC

Bit Number	Meaning when = 0	Meaning when = 1
0	G.I.R. Temperature indicator is above the upper threshold	G.I.R. Temperature indicator is below the upper threshold
1	G.I.R. Temperature indicator is below the lower threshold	G.I.R. Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Valack Timeout deasserted	Valack Timeout asserted
8	Empty Flag of Fifo1 asserted	Empty Flag for Fifo1 deasserted
9	Full Flag of Fifo1 asserted	Full Flag for Fifo1 deasserted
10	Empty Flag of Fifo2 asserted	Empty Flag for Fifo2 deasserted
11	Full Flag of Fifo2 asserted	Full Flag for Fifo2 deasserted
12	Global Saroc_Empty asserted	Global Saroc_Empty deasserted
13	Status: No fault	Status: Event fault 0
14	Status: No fault	Status: Event fault 1
15	Status: No fault	Status: Event fault 2

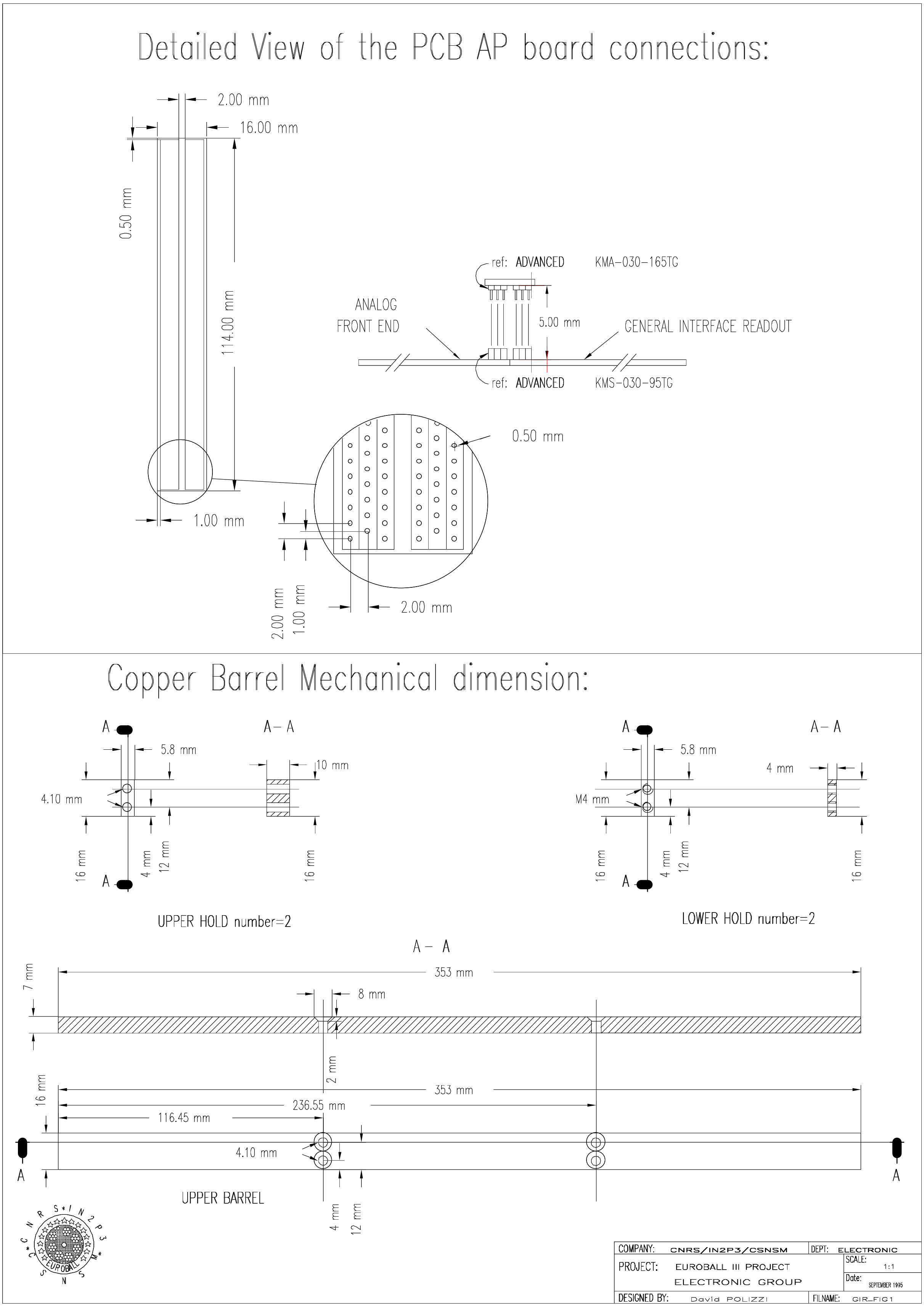
Event Fault 0 = local event number fails to match broadcast event number.
Event Fault 1 = Resynchronised by exactly 1 count (latched).
Event Fault 2 = Resynchronised by more than 1 count (latched).

10. General Figures:

10.1. Isometric View of the G.I.R. & the Analog card:



10.2. Copper Barrel Mechanical Dimensions,& PCB_AP board connections:



10.3. Ge & BGO Dac, PPADC Asic Dac connection figure Serial E²Prom,

& Temperature Sensor Connection figure :