DT32 to VME Buffer (D2VB) Specification

P.J.Coleman-Smith, V.F.E.Pucknell Version 1 14/4/94

Introduction

The D2VB, DT32 bus to VME buffer, is a double height VME card situated in an Event Builder crate interfacing the Eurogam data sources to the Event builder processors.

It features capabilities which include -

- DT32 bus controller.
- 2 Mbyte static RAM buffer.
- VME slave A32/D64/D32 for Buffer access, and supports burst mode at better than 40Mbytes/sec.
- VME slave A24/D32/D16 for control
- Buffer available for testing via VME.
- DT32 bus access uses chained lists providing block start address, high water mark, cut-off, and control information. List store is separate from the buffer. After each block has been used the word count and status will be updated in the list store.
- Interrupts may be generated at the end of a block, end of chain, and on error conditions.
- Both Read and Write functions may be concurrent.
- DT32 bus to buffer Write is 10MHz (DT32 bus spec.)
- VME Read from buffer exceeds 10MHz during bursts.
- Daisy chain connection for multiple DT32 bus masters to share control of the DT32 bus.
- Inspection lines for access to DT32 bus control signals.
- Ability to synchronise multiple D2VB interfaces.

Capabilities described

Physical size and appearance.

The D2VB is implemented to fit into a double height VME crate. It occupies 2 slots due to constraints of the front panel layout.

DT32 bus

The D2VB is a DT32 bus master as described in EDOC075. It can thus control the reading of events from the EUROGAM data sources. It is intended to make this interface as flexible as possible to allow interfacing to other differential ECL busses with changes only made to programmable circuits.

RAM buffer

The buffer is implemented as static RAM to remove the need for ‘refresh’. This is 2 blocks of 256K x 32 bits. .

Buffer write control

The control of DT32 bus writes to the buffer is handled by a sequencer using a chain list in a separate RAM from the buffer. This allowsmaximum use to be made of the available buffer area, without waiting for slow processors to release the blocks they are using.

The software is required to set up the list entries with the following information.

Start Address	Buffer address of the start of this block of events.
High water mark	Buffer address after which the next event is to be stored in a new block.
Cut-off	Buffer address at which storage of data from the DT32 is suspended, and thrown away. The next buffer is then started. This could start with the data coming in, if it still is, or more properly with the next event. This would be an error condition if this address was reached. The actions taken at this point can be chosen by software.
Next entry pointer	Address of the next list entry in the list RAM. This is set to -1 to indicate the last entry in a chain

The pointer used by the sequencer for accessing the list table is available to software for use in determining the blocks that have been filled.

The sequencer is started by being enabled with its list table pointer containing an entry address not equal to -1.

Access to the buffer RAM is controlled so as to allow both read, and write accesses at the speeds of the respective busses.

VME control interface

VME slave A24/D32/D16 for control. Access to the List RAM, and setting up of interrupts, and the sequencer. All registers are read/write.

VME interrupts

Vectored interrupt generation on enabled error conditions, end of buffer or end of chain list reached by the sequencer. Interrupt is on a level selected by software. Vector is generated using the highest priority condition. Other conditions set at the same time do not cause a further interrupts.

VME buffer interface

A32/D64/D32 slave. This is available in 2 modes,

1) When the DT32 bus sequencer is active, read only, and read only burst. Interface is designed to have a data rate of better than 10Mhz during the burst.

2) At other times the buffer is read/write for clearing and testing.

Inspection lines

The DT32 bus control signals, certain of the sequencer and other internal signals to be brought out to a front panel connection for display on a local ‘scope or logic analyser.

Multiple DT32 bus masters protocol

This defines an interface between several D2VBs. The purpose of the interface is to pass mastership of the DT32 bus between them. This is handled by means of passing a token round a loop. The token then enables the holder to control the bus.

The full details of this interface will be published at a later date.

USE WITH OTHER INTERFACES

It is proposed to use this store with interfaces other than the DT32. For this purpose it will be possible to connect a second VME card in place of the ouput of the DT32 ECL recievers. The connectors will be in place to accomodate this. The action of connecting will disconnect the DT32 bus.

This connection will be a TTL version of the DT32 bus so it will be a requirment that the new card provides data to the D2VB in an identical manner to that used for the DT32 bus.

With this facility in place it becomes possible to connect cards with other capabilities in the same way. Examples of this are Data processors, and analysers.They could plug into the VME backplane for control and power.