CDOC219

CHARISSA DATA ACQUISITION SYSTEM

Register Definitions for the LeCroy 2277 TDC

Edition 1.0

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Nuclear Physics Support Group

Central Laboratory of the Research Councils
Daresbury Laboratory

Registers for the LeCroy 2277 TDC module

This document should be read in conjunction with the document **EDOC210** which describes the **Register Server** implementation for **CAMAC**.

This is a 32 channel TDC module with CAMAC data readout.

All register attributes include -c (crate address) and -n (station address)

Registers using the **xCAMAC** class of the **CAMAC** Register Server

status register read by f(1) a(0) and write by f(17) a(0)

The data value stored in the status register is interpreted by the module as a bit pattern.

bits 0,1	Tester hit burst	00 = 1 hit 01 = 2 hits 10 = 4 hits 11 = 8 hits
bits 2,3	Tester hit duration	00 = 128 nsec 01 = 256 nsec 10 = 1024 nsec 11 = 2048 nsec
bits 4,5,6	unused	=0
bit 7	Trigger mode	0 = pulse: 1 = latch
bit 8	odd channel test input	0 = disable 1 = enable
bit 9	even channel test input	0 = disable 1 = enable
bit 10	hit trailing edge recording	0 = disable 1 = enable
bit 11	hit leading edge recording	0 = disable 1 = enable
bits 12-14	common start timeout	000 = front panel 001 = 1024 nsec 010 = 2048 nsec 011 = 4096 nsec 100 = 8192 nsec 101 = 16384 nsec 110 = 32768 nsec 111 = 65536 nsec
bit 15	mode	0 = common stop 1=common start

lc2277#*.status attributes -a 0 -f 1 -w 16 -p rw -l 0 -b 0 -z x -i 0
lc2277#*.status.mode attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 15 -z d -i 1
lc2277#*.status.timeout attributes -a 0 -f 1 -w 16 -p rw -l 3 -b 12 -z d -i 5
lc2277#*.status.leading attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 11 -z d
lc2277#*.status.trailing attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 10 -z d -i 1
lc2277#*.status.eventest attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 9 -z d

lc2277#*.status.oddtest attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 8 -z d
lc2277#*.status.trigmode attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 7 -z d
lc2277#*.status.testhit attributes -a 0 -f 1 -w 16 -p rw -l 2 -b 2 -z d
lc2277#*.status.testhitlen attributes -a 0 -f 1 -w 16 -p rw -l 2 -b 0 -z d

Channel data read by f(0) a(0)

Data readout via the **CAMAC** dataway. Module returns Q=1 if valid data is present; Q=0 if FIFO is empty.

lc2277#*.data attributes -a 0 -f 0 -w 24 -p ro -l 0 -b 0 -z x -q 1

Registers using the **cCAMAC** class of the **CAMAC** Register Server

These registers do not require data and have no initial value. However read-register operations may return Q and X as data.

Clear write or read by f(9) a(0)

Module clear. F(9) does not affect the status register.

lc2277#*.clear attributes -a 0 -f 9

Test LAM read by f(8) a(0)

returns Q=1 if the module LAM is set

lc2277#*.testlam attributes -a 0 -f 8

Clear LAM read by f(10) a(0)

clears the module LAM

lc2277#*.clearlam attributes -a 0 -f 10

Disable LAM read by f(24) a(0)

Disables the module LAM. The state of the module LAM enable will be arbitary after power on.

lc2277#*.disable attributes -a 0 -f 24

Enable LAM read by f(26) a(0)

Enables the module LAM.

lc2277#*.enable attributes -a 0 -f 26

Test cycle read by f(25) a(0)

Test cycle.

lc2277#*.test attributes -a 0 -f 25

Test “buffering in progress” read by f(27) a(0)

returns Q=1 if true

lc2277#*.testbuffering attributes -a 0 -f 27

Test Busy read by f(27) a(1)

returns Q=1 if Busy is true.

lc2277#*.testbusy attributes -a 1 -f 27