CDOC217

CHARISSA DATA ACQUISITION SYSTEM

Register Definitions for the Event Controller

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Nuclear Physics Support Group

Central Laboratory of the Research Councils
Daresbury Laboratory

Registers for the Charissa Event Control module

This document should be read in conjunction with the document **EDOC210** which describes the **Register Server** implementation for **CAMAC**.

All register attributes include -c (crate address) and -n (station address)

Registers using the **xCAMAC** class of the **CAMAC** Register Server

control register write by f(17) a(2)

Only bits 11 to 15 are used. The control register bits enable action if set as follows

bits 1-10	unused	=0
bit 11		enable cache read error LAM
bit 12		enable Read and Store timeout error LAM
bit 13		enable FERA timeout error LAM
bit 14		enable Trigger timeout error LAM
bit 15		enable Operation - enter EMO state

EC.control	attributes -a 2 -f 17 -w 16 -p wo -l 0 -b 0 -i 0
EC.control.enable	attributes -a 2 -f 17 -w 16 -p wo -l 4 -b 11
EC.control.Cacheerr	attributes -a 2 -f 17 -w 16 -p wo -l 1 -b 11
EC.control.RSMerr	attributes -a 2 -f 17 -w 16 -p wo -l 1 -b 12
EC.control.FERAerr	attributes -a 2 -f 17 -w 16 -p wo -l 1 -b 13
EC.control.Trigerr	attributes -a 2 -f 17 -w 16 -p wo -l 1 -b 14
EC.control.EMO	attributes -a 2 -f 17 -w 16 -p wo -l 1 -b 15

Digital Discriminator read by f(0) a(2) & write by f(16) a(2)

The digital threshold is written in an 8 bit register.
This register can only be accessed when the Event Controller is not in the Module Operation (EMO) state.

EC.dd attributes -a 2 -f 0 -w 16 -p rw -l 8 -b 0 -i 4

The Event Control Module contains a **total** register and a **fera** register.
The **total** register defines the total number of bytes that should be transferred per event between the EC module and the trigger interface and also the number of bytes of hit pattern which should be sent to the RSM. The value actually written to the hardware register is 1 less than this number.It is thus the total number of data channels rounded up to a multiple of 8, divided by 8 and less 1.

The **fera** register is similar but defines just those bytes which are reserved for FERA devices. It is thus the total number of fera channels rounded up to a multiple of 8, divided by 8 and less 1.

Total limit & control status read by f(1) a(1)

The current value of the **total** register is returned in the least significant 8 data bits and the control status is returned in the most significant 8 data bits.

The control status bits indicate status if set as follows

bit 8	Module not busy
bit 9	Delay Mode
bit 10	Accept All Data
bit 11	Channel Number incorrect for FERA read
bit 12	Timing Error in Read and Store cycle
bit 13	Timing Error in FERA cycle
bit 14	Timing Error in Trigger cycle
bit 15	Module Operation Enabled (EMO state)

EC.rd_total	attributes -a 1 -f 1 -w 16 -p ro -l 8 -b 0 -z d
EC.status	attributes -a 1 -f 1 -w 16 -p ro -l 8 -b 8 -z x
EC.status.bit8	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 8 -z d
EC.status.bit9	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 9 -z d
EC.status.bi10	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 10 -z d
EC.status.bit11	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 11 -z d
EC.status.bit12	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 12 -z d
EC.status.bit13	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 13 -z d
EC.status.bit14	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 14 -z d
EC.status.EMO	attributes -a 1 -f 1 -w 16 -p ro -l 1 -b 15 -z d

Cache limit & control status read by f(1) a(2)

The current value of the **fera** register is returned in the least significant 8 data bits and the control status is returned in the most significant 8 data bits.

EC.rd_cache	attributes -a 2 -f 1 -w 16 -p ro -l 8 -b 0 -z d

Cache & Total limits write by f(17) a(1)

The value of the **fera** register is written in the least significant 8 data bits and the value of the **total** register is written in the most significant 8 data bits.
This register can only be accessed when the Event Controller is not in the Module Operation (EMO) state.

EC.cache attributes -a 1 -f 17 -w 16 -p wo -l 8 -b 0 -i 0
EC.total attributes -a 1 -f 17 -w 16 -p wo -l 8 -b 8 -i 0

Registers using the **cCAMAC** class of the **CAMAC** Register Server

These registers do not require data and have no initial value. However read-register operations may return Q and X as data.

enable LAM write or read by f(26) a(0)

enable module LAM

EC.enable attributes -a 0 -f 26

disable LAM write or read by f(24) a(0)

disable module LAM

EC.disable attributes -a 0 -f 24

test LAM read by f(8) a(0)

returns Q=1 if the module LAM is set

EC.testlam attributes -a 0 -f 8

test LAM and clear read by f(10) a(0)

returns Q=1 if the module LAM is set and clears the LAM

EC.testclearlam attributes -a 0 -f 10

reset module read by f(11) a(1)

Complete clear of module
This register can only be accessed when the Event Controller is not in the Module Operation (EMO) state.

EC.reset attributes -a 1 -f 11

clear error status write or read by f(11) a(2)

Clear all the error status bits in the Control Status register only

EC.clear attributes -a 2 -f 11

test EMO state read by f(27) a(1)

returns Q=1 if the module is in the Enable Module Operation (EMO) state.

EC.test_EMO attributes -a 1 -f 27

test TEST state read by f(27) a(2)

returns Q=1 if the module is in the TEST state.

EC.test_TEST attributes -a 2 -f 27

Simulate STROBE write or read by f(25) a(0)

Simulate a Strobe input.
This register can only be accessed when the Event Controller is not in the Module Operation (EMO) state.

EC.strobe attributes -a 0 -f 25