EDOC215
CDOC215

CHARISSA DATA ACQUISITION SYSTEM

Register Definitions for the LeCroy 2375 module

Edition 1.0

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Registers for the LeCroy 2375 Data Stack Module

This document should be read in conjunction with the document **EDOC210** which describes the **Register Server** implementation for **CAMAC**.

This is a fast 256 x 16 memory with separate read and write ECL ports used for data readout from modules having FERA outputs.

All register attributes include -c (crate address) and -n (station address)

Registers using the **xCAMAC** class of the **CAMAC** Register Server

Memory Address Read Pointer (RP) read by f(0) a(1) & write by f(16) a(1)

The 8bit internal Read Pointer is used to define the next offset for read access to the data stack memory.

DS.rp attributes -a 1 -f 0 -w 16 -p rw -l 8 -b 0 -i 0 -z d -i 0

Memory Address Write Pointer (WP) read by f(0) a(4) & write by f(16) a(4)

The 8bit internal Write Pointer is used to define the next offset for write access to the data stack memory.

DS.wp attributes -a 4 -f 0 -w 16 -p rw -l 8 -b 0 -i 0 -z d -i 0

Memory Access read by f(0) a(0) & write by f(16) a(0)

Read or write a 16-bit dataword from memory as addressed by the Read Pointer (RP) or the Write Pointer (WP) and increment the Read or Write Pointer.

DS.data attributes -a 0 -f 0 -w 16 -p rw -l 0 -b 0 -z x

Registers using the **cCAMAC** class of the **CAMAC** Register Server

These registers do not require data and have no initial value. However read-register operations may return Q and X as data.

reset write or read by f(9) a(0)

module reset

DS.reset attributes -a 0 -f 9