EDOC213
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EUROGAM DATA ACQUISITION SYSTEM
CHARISSA DATA ACQUISITION SYSTEM

Register Definitions for the Silena 4418/V ADC

Edition 1.0

April 1995

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Registers for the Silena 4418/V ADC module

This document should be read in conjunction with the document **EDOC210** which describes the Register Server implementation for **CAMAC**.

This is a 8 channel ADC module with FERA and CAMAC data readout.

All register attributes include -c (crate address) and -n (station address)

Registers using the **xCAMAC** class of the **CAMAC** Register Server

status register read by f(4) a(14) & write by f(20) a(14)

The status register is composed of two distinct sections. The least significant 8 bits contain the Virtual Station Number (VSN) which determines the address of the data source during FERA readout. The most significant 8 bits determine the readout modes.

bit 8	unused	=0
bit 9	SUB	Channel Subaddress Enable, enabled with SUB=0. channel address is inserted into bits 12-14 of the 16 bit ADC data word.
bit 10	EEN	ECL port Enable: when EEN=1 ECL port readout is permitted, when EEN=0 CAMAC readout is permitted.
bit 11	OVF	Overflow Indication Enable, enabled with OVF=0. overflow indication is inserted into bit 15 of the 16 bit ADC data word
bit 12	CCE	CAMAC data Compression Enable: when CCE=1, data zeros or data zeros-and-overflows are suppressed for CAMAC sequential readout
bit 13	CSR	CAMAC Sequential Readout: when CSR=0, CAMAC random access readout is enabled; when CSR=1, CAMAC sequential readout is enabled
bit 14	CLE	CAMAC Lam Enable: when CLE=1, LAM is enabled
bit 15	unused	=0

```
s4418#*.status       attributes  -a 14  -f 4  -w 16  -p rw  -l 0  -b 0  -z x -i 0
s4418#*.status.vsn   attributes  -a 14  -f 4  -w 16  -p rw  -l 8  -b 0  -z x
s4418#*.status.mode  attributes  -a 14  -f 4  -w 16  -p rw  -l 8  -b 8  -z x
s4418#*.status.sub   attributes  -a 14  -f 4  -w 16  -p rw  -l 1  -b 9  -z d
s4418#*.status.een   attributes  -a 14  -f 4  -w 16  -p rw  -l 1  -b 10  -z d
s4418#*.status.ovf   attributes  -a 14  -f 4  -w 16  -p rw  -l 1  -b 11  -z d
s4418#*.status.cce   attributes  -a 14  -f 4  -w 16  -p rw  -l 1  -b 12  -z d
s4418#*.status.csr   attributes  -a 14  -f 4  -w 16  -p rw  -l 1  -b 13  -z d
s4418#*.status.cle   attributes  -a 14  -f 4  -w 16  -p rw  -l 1  -b 14  -z d
```

Upper Level Discriminator read by f(1) a(x) & write by f(17) a(x)

The upper threshold memory (8 bits) is accessed for channel x (0-7) using subaddress x. Values 0-255 correspond to 85% to 100% of full scale.

s4418#*.adc*.uld attributes -a x -f 1 -w 16 -p rw -l 8 -b 0 -i 255

Initial value is the current default used by the Charissa DA system.

Lower Level Discriminator read by f(1) a(8+x) & write by f(17) a(8+x)

The lower threshold memory (8 bits) is accessed for channel x (0-7) using subaddress 8+x. Values 0-255 correspond to 0% to 10% of full scale.

s4418#*.adc*.lld attributes -a 8+x -f 1 -w 16 -p rw -l 8 -b 0 -i 1

Initial value is the current default used by the Charissa DA system.

Common Threshold read by f(4) a(9) & write by f(20) a(9)

The common threshold memory (8 bits) applies to all channels.

s4418#*.threshold attributes -a 9 -f 4 -w 16 -p rw -l 8 -b 0 -i 28

Initial value is the current default used by the Charissa DA system.

Offset Memory read by f(4) a(x) & write by f(20) a(x)

The offset memory (8 bits) is accessed for channel x (0-7) using subaddress x. Values 0-255 correspond to -3% to +3% of full scale. Value 128 is offset 0.

s4418#*.adc*.offset attributes -a x -f 4 -w 16 -p rw -l 8 -b 0 -i 128

Initial value is the current default used by the Charissa DA system.

ADC data read by f(0) a(x) or f(2) a(x)

Random access or sequential readout of the 8 ADC values via the CAMAC dataway. Channel x (0-7) is selected using subaddress x in random access readout only (CSR=0). In sequential mode (CSR=1) the subaddress is ignored.
Readout using f(2) clears the module.

s4418#*.adc*.data attributes -a x -f 0 -w 16 -p ro -l 0 -b 0
s4418#*.adc*.data+clr attributes -a x -f 2 -w 16 -p ro -l 0 -b 0

Header word data read by f(0) a(14) or f(2) a(14)

Reads the event header word data f(0) a(14) or reads the event header word data and clears the module f(2) a(14).

s4418#*.hdr.data attributes -a 14 -f 0 -w 16 -p ro -l 0 -b 0
s4418#*.hdr.data+clr attributes -a 14 -f 2 -w 16 -p ro -l 0 -b 0

Pattern word data read by f(0) a(15) or f(2) a(15)

Reads the event pattern word data f(0) a(15) or reads the event pattern word data and clears the module f(2) a(15).

s4418#*.patt.data attributes -a 15 -f 0 -w 16 -p ro -l 0 -b 0
s4418#*.patt.data+clr attributes -a 15 -f 2 -w 16 -p ro -l 0 -b 0

Registers using the **cCAMAC** class of the **CAMAC** Register Server

These registers do not require data and have no initial value. However read-register operations may return Q and X as data.

reset write or read by f(9) a(0)

module reset

s4418#*.reset attributes -a 0 -f 9

test LAM read by f(8) a(0)

returns Q=1 if the module LAM is set

s4418#*.testlam attributes -a 0 -f 8

test LAM and clear read by f(10) a(0)

returns Q=1 if the module LAM is set and clears the LAM

s4418#*.testclearlam attributes -a 0 -f 10

test module read by f(25) a(0)

returns Q=1 if BUSY =0, returns Q=0 if the module is not in the “ready” state.

s4418#*.test attributes -a 0 -f 25