EDOC212

EUROGAM DATA ACQUISITION SYSTEM

Register Definitions for the LeCroy 4300B ADC

Edition 1.0

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Registers for the LeCroy 4300B ADC module

This document should be read in conjunction with the document **EDOC210** which describes the **Register Server** implementation for **CAMAC**.

This is a 16 channel ADC module with FERA and CAMAC data readout.

All register attributes include -c (crate address) and -n (station address)

Registers using the **xCAMAC** class of the **CAMAC** Register Server

status register **read by f(0) a(0) & write by f(16) a(0)**

The status register is composed of two distinct sections. The least significant 8 bits contain the Virtual Station Number (VSN) which determines the address of the data source during FERA readout. The most significant 8 bits determine the readout modes.

bit 8	EPS	ECL port Pedestal Subtraction: when EPS=1, pedestals are subtracted for ECL port readout
bit 9	ECE	ECL port data Compression Enable: when ECE=1, data zeros or zeros-and-overflows are suppressed for ECL port readout
bit 10	EEN	ECL port Enable: when EEN=1, ECL port readout is permitted
bit 11	CPS	CAMAC Pedestal Subtraction: when CPS=1, pedestals are subtracted for CAMAC readout
bit 12	CCE	CAMAC data Compression Enable: when CCE=1, data zeros or data zeros-and-overflows are suppressed for CAMAC sequential readout
bit 13	CSR	CAMAC Sequential Readout: when CSR=0, CAMAC random access readout is enabled; when CSR=1, CAMAC sequential readout is enabled
bit 14	CLE	CAMAC Lam Enable: when CLE=1, LAM is enabled
bit 15	OFS	OverFlow Suppression: when OFS=1, data readouts are suppressed during ECL port readout in conjunction with ECE=1 and for CAMAC sequential readout in conjunction with CCE=1

lc4300b#*.status	attributes -a 0 -f 0 -w 16 -p rw -l 0 -b 0 -z x -i 0
lc4300b#*.status.vsn	attributes -a 0 -f 0 -w 16 -p rw -l 8 -b 0 -z x
lc4300b#*.status.mode	attributes -a 0 -f 0 -w 16 -p rw -l 8 -b 8 -z x
lc4300b#*.status.eps	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 8 -z d
lc4300b#*.status.ece	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 9 -z d
lc4300b#*.status.een	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 10 -z d
lc4300b#*.status.cps	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 11 -z d
lc4300b#*.status.cce	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 12 -z d

lc4300b#*.status.csr attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 13 -z d
lc4300b#*.status.cle attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 14 -z d
lc4300b#*.status.ofs attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 15 -z d

Pedestal memory read by f(1) a(x) and write by f(17) a(x)

The pedestal memory (8 bits) is accessed for channel x (0-15) using subaddress x.

lc4300b#*.adc*.pedestal attributes -a x -f 1 -w 16 -p rw -l 8 -b 0 -i 1

ADC data read by f(2) a(x)

random access or sequential readout of the 16 ADC values via the CAMAC dataway. Channel x (0-15) is selected using subaddress x in random access readout only (CSR=0). In sequential mode (CSR=1) the subaddress is ignored.

lc4300b#*.adc*.data attributes -a x -f 2 -w 16 -p ro -l 0 -b 0

Registers using the **cCAMAC** class of the **CAMAC** Register Server

These registers do not require data and have no initial value. However read-register operations may return Q and X as data.

reset write or read by f(9) a(0)

module reset

lc4300b#*.reset attributes -a 0 -f 9

test LAM read by f(8) a(0)

returns Q=1 if the module LAM is set

lc4300b#*.testlam attributes -a 0 -f 8

test LAM and clear read by f(10) a(0)

returns Q=1 if the module LAM is set and clears the LAM

lc4300b#*.testclearlam attributes -a 0 -f 10

test module read by f(25) a(0)

returns Q=1 if BUSY =0, returns Q=0 if the module is not in the “ready” state.

lc4300b#*.test attributes -a 0 -f 25