Eurogam Project: Specification of Histogrammer

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Version 2

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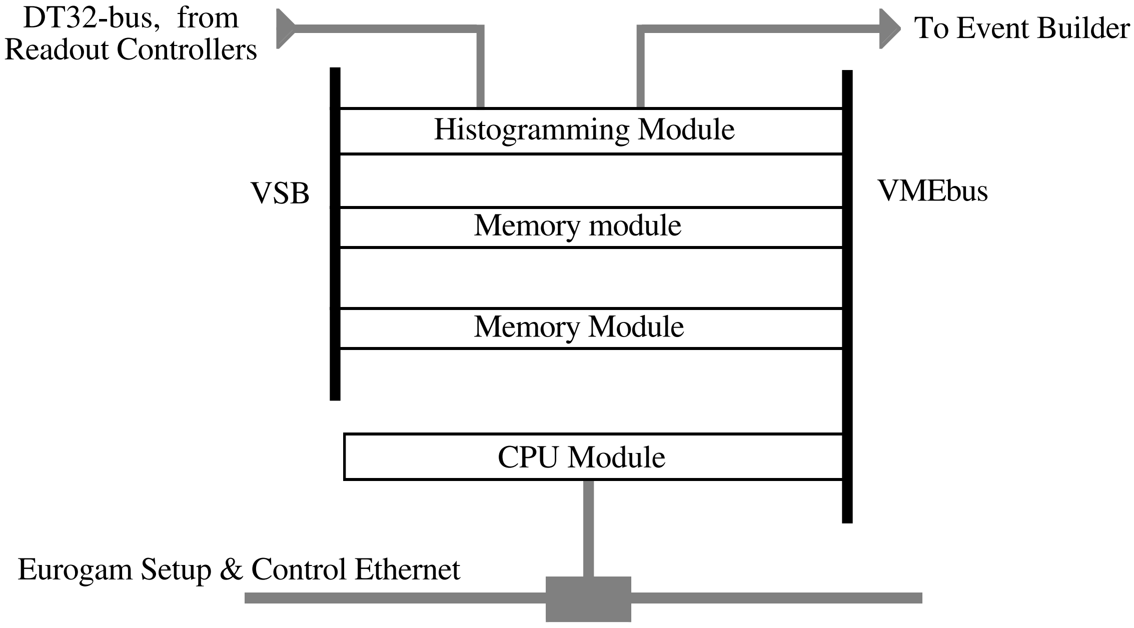
Version 2 is an update, written after the October 1990 Eurogam general meeting, and after discussions with J. Thornhill of Liverpool University (who will be designing the Histogramming Module). Changes are mainly of a detailed nature.

Version 1 was based on my previous paper "Discussion Paper on Eurogam Histogramming Module", and included decisions taken at the July 1990 Eurogam general meeting. Sections 1 and 2 were essentially the same as in that paper; section 3 was totally revised.

1. Overview of Histogramming in Eurogam

- Only those parameters which are collected as part of multi-parameter events will be histogrammed, – i.e. 'true' singles histogramming will not be implemented.
- Histogramming will be implemented at a *single* point in the system: the histogramming unit, which will be connected to the DT32-bus (defined in reference 1), at a point between the Readout Controllers and the Event Builder. The histogramming unit will 'spy' on the event data, and will not normally participate in controlling the flow of data from Readout Controllers to Event Builder.
- The histogramming unit will be controlled via the Eurogam Setup and Control Ethernet. Control functions will include the starting and stopping of histogram collection, and the selection of which parameters are to be histogrammed. (N.B. a parameter is identified by the 14-bit address field within the 32-bit parameter word).
- Histograms will be read out from the histogramming unit via the Setup and Control Ethernet. This will be possible at any time, including during histogram collection.
- The histogramming unit will be built in VMEbus mechanics, probably in the format illustrated in Figure 1 (the final choice will be left with the designer). It is expected that all units, except the Histogramming Module, will be commercial items. The number of memory modules used will depend upon their capacity, and on the number of concurrent histograms required for a particular experiment.

Fig 1. Suggested configuration of the Histogramming Unit



- **Data Rates**

The maximum 'burst' data rate on the DT32-bus will be 10 MHz; but the average rate of event data will be less. This average rate is not completely specified. At the Eurogam meeting in Strasbourg (March 1990) a minimum data rate of 200 K parameters per second was requested; with the possibility of 2 M parameters per second to be considered. These are the data rates required *on magnetic tape, after* any data rate reduction within the Event Builder, – and therefore the rates on the DT32-bus will be greater than these, by a factor which is not currently known.

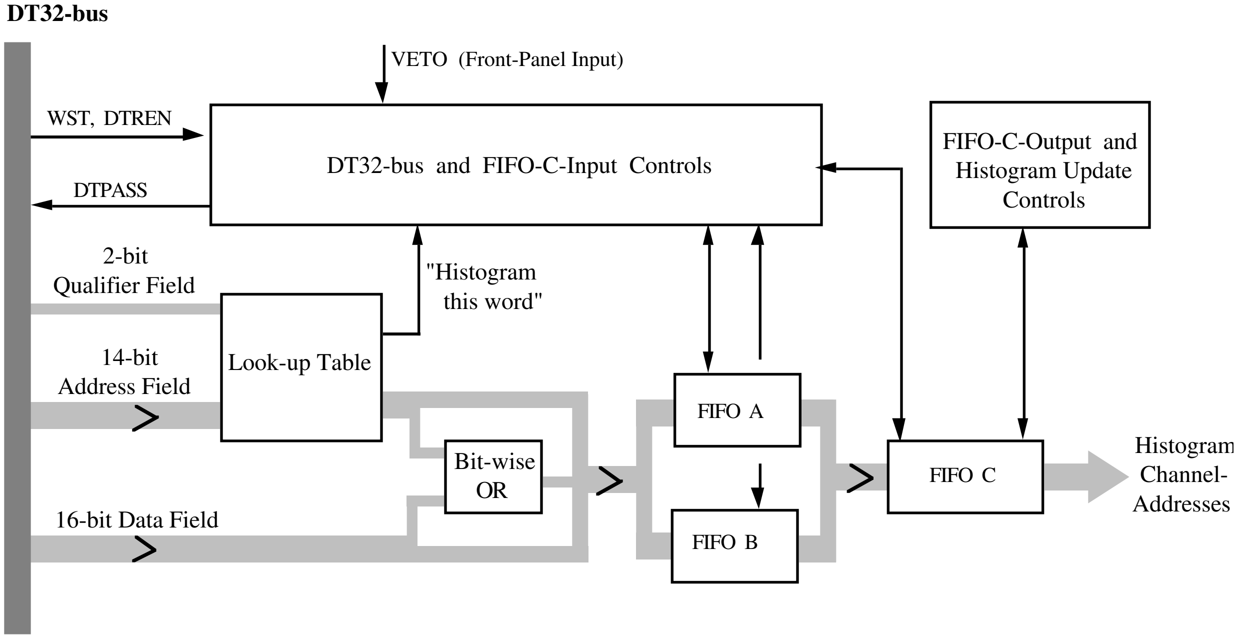
As an indication of the likely histogram update rate which can be achieved, work already done at Daresbury for Gamic (the precursor of Eurogam) indicates that it should be possible to increment a location in a commercial memory board, via the VSB, in 750 nS. This gives a histogram update rate of 1·3 MHz; – which is therefore the *average* DT32-bus data rate which can be handled if every parameter is to be histogrammed; but of course a higher (average) data rate can be handled if only a subset of the parameters are to be histogrammed.

If the histogramming unit cannot support the required average data rate, several histogramming units can be connected to the DT32-bus in parallel. Software must then allocate a subset of the parameters to be histogrammed to each unit, in such a way that no unit exceeds its maximum rate. The units can all be accommodated in the same VME crate; but each obviously requires its own VSB backplane.

2. Description of the Histogramming Module

The required operation of the Histogramming Module is described in this section, with the aid of Figure 2, – which shows a suggested implementation of the module.

Fig 2. Suggested Implementation of the Histogramming Module



FIFO[1] C acts as a de-randomising buffer between the 10 MHz burst data rate on the DT32-bus and the average, slower, rate at which histogram updates are performed. The use of FIFOs A and B is described in section 3.4.

A software-programmable look-up table is used to examine the address and qualifier fields of each parameter on the DT32 bus. The most significant output from the look-up table is used to indicate whether the parameter is to be histogrammed or not: if it *is* to be histogrammed, then the base-address of the histogram (also stored in the look-up table) is combined with the data field of the parameter to form the address of the histogram channel which is to be incremented. (The base address and data are combined as specified in the next section.) This channel address is then entered into the FIFO. All this must be achieved within the 100 nS interval between parameter transfers on the DT32-bus.

When the channel-address reaches the output of FIFO C, the control logic there increments the 32-bit memory location which the address specifies. If the module is designed to work with 'standard' (non-incrementing) memory modules, it reads the value in the selected location, increments it by 1, and then writes back the new value.

1 "First In First Out" memory unit

3. Specification of the Histogramming Module

3.1 DT32-bus connections

These must meet the requirements of reference 1. All DT32-bus signals must be passed from input to output unaltered and with equal delays (within the limits specified in reference 1); except as described in section 3.4 for DTREN to DTPASS.

(Functionally, the Histogramming Module only needs a 'T' connection to the DT32-bus' data lines, but to preserve the electrical characteristics of the bus both the input and the output connectors *are* required.)

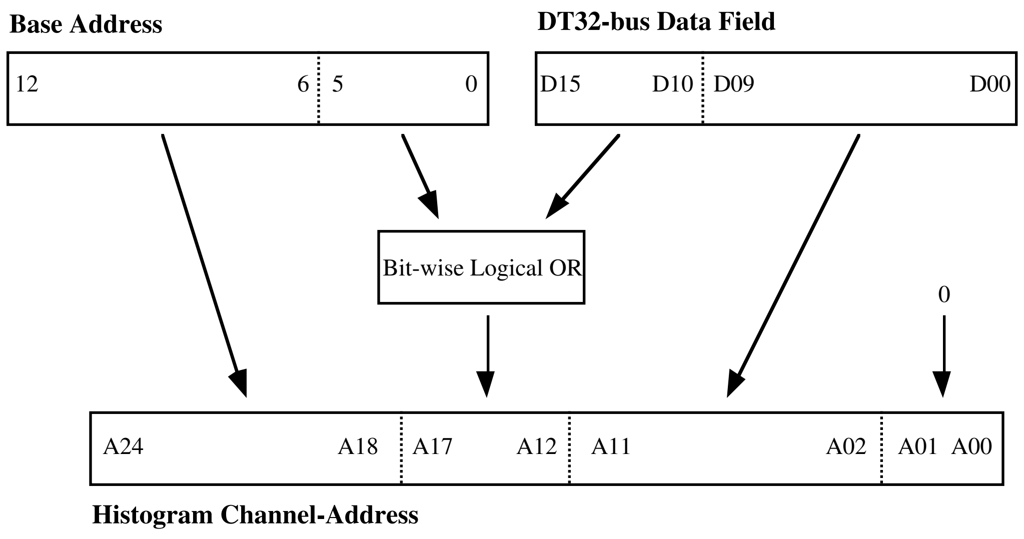
3.2 Look-up Table

The look-up table should be a RAM whose inputs (when the Histogramming Module is operating) are the 16 most significant data bits from the DT32-bus (i.e. D31 to D16). It must be possible to program all RAM locations via the VMEbus.

The most significant bit of the look-up table's output must be used to indicate whether the DT32-bus word is to be histogrammed or not: a '1' specifying that it *is* to be histogrammed. In addition, at least 13 output bits must be provided to specify a histogram's base-address, (the derivation of this number is explained in the next section).

3.3 Generation of Histogram Channel-Addresses

Figure 3. Generation of Histogram Channel-Addresses



The base-address from the look-up table must be combined with the data field from the DT32-bus, to form the histogram channel-address, as illustrated in Figure 3. Each of the bottom 6 bits of the base-address must be logically OR-ed with the corresponding bit from the top 6 bits of the data field (i.e. bit 0 is OR-ed with D10, bit 1 is OR-ed with D11, etc.).

This scheme permits software to adapt the base-address to be compatible with the size of the data parameter, – by putting 0's in the base-address where it overlaps those data bits which are used. **It also requires that data sources, such as Ge and BGO cards, put 0's in the upper, unused, bits of their data fields.**

The bottom 2 bits of the channel-address are set to 0 so as to select a 4-byte (32-bit) memory location, – i.e. a channel has a maximum count of 4 G-counts.

The minimum size of 13 bits for the base-address allows for 8 M[1]-channels of histogram. This is sufficient for the known requirements of Eurogam:

Ge detectors:	70×4	14-bit ADCs	=	4480	K[2] channels
BGO detectors:	70×2	10-bit ADCs [3]	=	140	K channels
	70×1	11-bit ADC [4]	=	140	K channels
		Total:		4760	K channels

It is preferable that the Histogramming Module also includes a programmable register to specify the upper address lines (A31 to A25), – which will therefore be common to all channel addresses.

3.4 Overflow counter

A counter of 32 bits must be provided to count the number of histogram updates which cannot be made because the Histogramming Module's buffer FIFO ("C' in Figure 1) is full. Since histograms are statistical information, a few missed counts (at random times and in random channels) should not matter. The counter can be used to monitor the histogrammer's performance.

3.5 Histogram-update VETO Input

The Histogramming Module must have a front-panel VETO input, which accepts NIM input levels via a single-pin LEMO 00 socket. The effect of this input must be to veto *all* histogram updates associated with an event. The VETO input should be valid, and must be sampled by the module, when all the data for an event has been collected: this is signalled to the module by the assertion of DTREN (since it is situated after the last Readout Controller on the DT32-bus).

One way of achieving the veto function is to use two FIFOs ('A' and 'B' in figure 1), each of which can hold the data associated with one complete event. During readout of an event, over

[1] "M" = 2^{20}
[2] "K" = 2^{10}
[3] Energy ADC, and BGO shield hit-pattern
[4] Time ADC

the DT32-bus, those parameters which are to be histogrammed are stored in FIFO A or B (whichever is free at the beginning of the event). Then, if the VETO input is active when DTREN is received, the FIFO is cleared; if not, the data from the FIFO is allowed to pass into FIFO C. Data for the *next* event can then be stored in the other FIFO (A or B) while the first event's data is still being transferred into FIFO C.

If DTREN is received (at the end of the second event) before the first FIFO has been emptied, then the Histogramming Module should block DTPASS until the first FIFO *has* been emptied, – so as to delay the readout of the next event until a FIFO (A or B) is empty. (Note that this should not occur frequently, and when it does the delay will not be large, as data can be transferred between FIFOs at a higher rate than it will be received from the DT32-bus.)

Whenever FIFO C is full, the blocking of DTPASS must be disabled – since this is an overflow condition, and must not impede the operation of the DT32-bus. It is also desirable that the Histogramming Module can be programmed to ignore the VETO input, and therefore *always* pass DTREN to DTPASS without delay, when the veto function is not being used.

Note that if the VETO signal cannot be generated quickly enough to precede the arrival of DTREN at the Histogramming Module, then extra delay will have to be inserted into the DTREN daisy-chain by an external unit (typically this would be the unit generating the VETO signal, which would be situated immediately prior to the Histogramming Module on the DT32-bus).

3.6 VMEbus Interface

Control and programming of the Histogramming Module must be via the VMEbus. Provision must be made for:

- Writing and reading a 'histogramming-enable' bit. When set to 1 this must permit histogramming. The bit must be set to 0 by SYSRESET.
- Reading and (separately) clearing the overflow counter.
- Writing and reading the look-up table; and high-order base-address register if provided.

Writing the look-up table, and high-order base-address register, must only be effective when the histogramming-enable bit is at 0. Locations within the table should either be selected by mapping them onto VMEbus addresses; or by the use of an address counter which can be written to, and which increments (to the next channel address) after each read or write operation on the look-up table.

It is suggested that the Histogramming Module should also implement commands for clearing selected blocks of histogram memory.

4. References

1. "Eurogam Project: Specification of the DT32-bus" by J. Alexander
2. Minutes of the October 1990 Eurogam general meeting's plenary session on DT32-bus data formats.