Eurogam Hardware Meeting at CNRS Strasbourg

Ian Lazarus

Held 17th and 18th October 1990

The meeting was attended by the following:

John Alexander
Nabil Karkour
Jean-Claude Gouillaud †
Charles Ring
Patrick Coleman-Smith
John Lisle †
Germain Bosson
George McPherson
Les Wilkinson
Daniel Lecouturier †
Jean-Louis Pedroza †
Christoph Ender †
Zdravko Zojceski
Alphonse Richard
Ian Lazarus
Paul Nolan †

The † symbol indicates those who were unable to attend the entire meeting.
The meeting was chaired by George McPherson and Charles Ring.

1. **Preamplifiers**
   (a) **Ge** presented by Lisle:
   Ge preamps have been specified to Ortec as follows:
   Sensitivity 200mV/MeV ±10%; time constant $50\mu s$ ±8%; Negative output.
   No written requirement for DC offset was stated although Ortec have subsequently been told by telephone that we want under 50mV DC offset. Intertechnique will be given the same specification which requires a change from positive to negative output. This was agreed between Beck and Intertechnique in parallel with this meeting.
   The first 5 Ortec preamps all have under 50mV DC offset. Richard commented that a small modification to the input hybrid circuit in the Ge card could be made to overcome the DC offset problem if it proves necessary.
   Actions: None.

   (b) **BGO** presented by Bosson:
   Questions raised:
   - Is preamp mounted inside PMT base or externally?
   - Is anode at ground or HV?

   Answers were that preamps will be mounted outside the PMT bases and that the anode is thought to be grounded.
   Action: Wilkinson to confirm that anode is grounded and tell Bosson.
   Action: Bosson to supply Wilkinson with PCB for preamp as soon as possible.
   Action: Wilkinson to devise a method of mounting preamplifiers outside PMT bases.
   Action: Bosson to supply Wilkinson with 10 working pre-amps to test with a Eurogam shield. Target date is mid-November.

   (c) **Power requirements**
   Ge preamp requires approx 25mA from -24V and 50mA from +24V. BGO requires

8mA from +24V. Cabling to the array must be added to carry these power supplies. It was agreed that we cannot assume that external amplifiers in NIM will supply the power and other supplies must be found.

Action: McPherson Investigate cabling and grounding requirements for both BGO and Ge preamplifiers. Investigate a suitable power source (VXI suggested).

Test pulsers in the preamplifers were agreed to be very useful. Decision made to make a strong recommendation to plenary session that funds be made available for additional cabling and circuitry to allow the inclusion of test pulsers at the preamp level.

(At plenary session the physicists reaction was not favourable to this suggestion.)

2. **Ge Card**

A status report on all aspects of the Ge card was distributed at the meeting by Richard.

(a) **Hybrids for Input/PZ adjustment, Filter amplifier, BLR, Output Amplifier, Peak Detection.** Presented by Ring.

These 5 hybrids have been delayed because of component supply problems. All 5 will be made on one substrate to save time and cost.

Question was asked as to whether 25ppm resistors are necessary in view of their cost (£80 per channel). The answer was yes they are and a suggestion of a cheaper supplier was made.

A NIM module is available to test these hybrids as soon as they are ready.

Action: Ring to supply hybrids as soon as possible for testing. (No target date could be agreed because there is no reliable component delivery date.)

Shaping time. Richard requires a firm decision within 1 month on the shaping time. Present physicists estimates (Lisle and Nolan) are 1 to 1.5μs shaping time constant.

Action: Lisle to supply Richard with the physicists final agreed value for the shaping time within 1 month (Mid-November). (Preferred method of definition is width at half max rather than time constant.)

(b) **TFA** Presented by Richard.

A paper was distributed at the meeting containing details of the TFA and its characteristics. Rise time is under 10ns and may be integrated if required. 1 or 2 prototypes are due next week in Orsay of the TFA hybrid. The surface mount prototype is OK and has same pinout as hybrid.

Actions: none.

(c) **ADC** Presented by Ring.

Test results presented for the surface mount ADC board tested in a NIM module (without ROCI or PDS hybrid, so using additional components for sliding scale and peak detection).

DNL: ±0.7 to 0.8%. DNL: 1.7% over 16K channels. INL: ±0.005%

Actions: none.

(d) **Readout ASIC (4 channel ROCI)** presented by Ring.

Status is that wafer was made during the week 8-12 Oct; the chips were encapsulated during week 15-19 Oct and 20 prototypes are due during the week 22-26 Oct. A VME card is available for digital checking of the ROCI but the analogue checking with the sliding scale and ADC to test linearity is a problem. The problem is that there is no spare manpower in Strasbourg to design a test board on the

necessary timescale. Bordeaux might have manpower available and offered to investigate feasibility of producing such a test board. Until these tests are conducted satisfactorily it is not possible to commence the layout of the Ge card because this requires the pinout of the ROCI to be fixed, but the 4 and 6 channel chips are not the same and so one must be proven to work and then selected.
Action: Gouillaud Investigate whether manpower is available to Bordeaux to produce the test card for 4 channel ROCI, ADC and sliding scale.

(e) **CFD** presented by Richard.
The CFD is finished. 2 working surface mount pcbs have been built and tested with pulsers. One was shown to the meeting. 8 more units due in November. Tests with detectors will start 23 Oct using TFA, CFD and TAC on NIM test card. Question asked by Richard as to whether the delay should be 50ns or 60ns. Lisle replied that it doesn't matter and Richard may choose.
Actions: none.

(f) **Crossover Detector** presented by Richard.
This will be implemented as a surface mount card. The crossover detector is very small so additional functions will also be implemented on the same board viz. 2 buffers for analogue multiplexers and 2 monostables (for crossover TAC delayed start and for pileup). Crossover threshold is still to be decided and the present suggestion is approximately 10keV.
Actions: none.

(g) **Ballistic Deficit** presented by Richard.
Correction coefficient has been calculated and checked. BDC hardware will be mounted on a small surface mount pcb.
Actions: none.

(h) **DAC's and registers** presented by Richard.
Engineer responsible is Karkour. 2 LCA's will be used for registers and to drive DAC bus. There was discussion of DAC sizes and it was agreed that:

- CFD threshold changes back from 12 to 8 bits. (0 to 1.25 MeV by 5 keV steps or 0 to 5 Mev by 20 keV depending on TFA gain selection.)
- Local trigger timing DACs changed from 12 to 8 bits (Fast trigger sample point now 0 to $2\mu s$ in 8ns steps; Validation 2-$10\mu s$ in 40ns steps). Note that channel to channel matching on any nominal value will be only 1 or 2% because of the internal timing ramp.

Thus all DACs are now 8 bits except the test generator amplitude DAC which is 16 bits. The 8 bit DACs may use octal packages which will save space as compared to the quad 12 bit packages.
Actions: none.

(i) **VME Control Interface** presented by Richard.
Engineer responsible is Deschamps. Implemented in an LCA and has been completely simulated. PROM will hold serial number, revision level and similar configuration information. A paper was available at the meeting describing the basic design although some details were out of date since the slight changes agreed between Alexander and Ring have also been implemented in the LCA but not reflected in the document. Alexander will provide the VME readout specification

during week 22-26 October.
Actions: none.

(j) **ROCI readout control** presented by Richard.
Engineer responsible is Karkour. Paper distributed at the meeting describes proposals for this part of the design.
Actions: none.

(k) **Analogue Multiplexer** presented by Richard.
Multiplexing and buffering will deal with pairs of channels which will share an 8 channel multiplexer. The question was asked as to whether users will accept the use of odd numbered channels connected to one inspection line and even numbered channels connected to the other. This means that channel 1 and channel 4 could be compared, but not channel 1 and channel 5. It was agreed that this is too restrictive to users and that we should allow a channel to be compared with any of the other channels. It is accepted that this will require more components, hence more board space and more cost.
Not all users appear to realise that the analogue multiplexing has been reduced from 5 to 4 points (20 MeV output, 4 MeV output, PZ adjust and TAC output) and that TFA output is no longer monitored.
Actions: none.

(l) **Digital Multiplexer** presented by Richard.
Question asked as to whether we check timing windows in trigger with separate logic inspection lines or the composite 'controle des fenetres' signal. The slot 0/RM card can cope with both, so it was agreed that the Ge card can use either (or both) at the designer's discretion.
Actions: none.

(m) **Local Trigger** presented by Karkour.
Document distributed describing the Local trigger. The surface mount board has been delayed due to component delivery problems but is ready for testing from week 22-26 Oct. The board was shown to the meeting.
The effect of the VXI inhibit line was clarified: the inhibit input to the local trigger is fed from an OR of the VXI inhibit line with the veto signal (due to suppression by BGO or pileup) if it is enabled from software.
Actions: none.

(n) **Test Generator** presented by Bosson.
Test generator surface mount board is finished and was shown to the meeting. There is to be one per shield on BGO and one per channel on Ge. There is a stability problem in that the 80ppm temperature coefficient is not good enough for use with Ge. 2 solutions were proposed: use 1 better test generator per board, buffered to all 6 channels or else design a better test pulser on the same pinout thus enabling design to proceed and using the present design as an interim solution. The second solution was agreed.
Actions: none.

(o) **TAC ASIC** presented by Bosson.
TAC ASIC is available and was shown to the meeting. It has 2 problems which need to be recified; firstly the -5.2V supply must be run at -4.0V because of a breakdown problem and secondly the INL is 4.2% on the $2\mu s$ range. The reason

for the second problem is not understood and a rework cannot be undertaken until a mechanism is understood. A document explaining the TAC circuits and operation was distributed at the meeting.
Actions: none.

(p) **External Amplifiers** presented by Lisle.
A quotation has been received from Tennelec for repackaged TC245 shaping amplifiers with ballistic deficit correction (2 channels per single width NIM module) at a cost of £1900 per channel including VAT. Whether we use these amplifiers or gated integrators the delivery time will be minimum 6 months from order.
Actions: none.

(q) **Main PCB and Front Panel** presented by Zojceski.
The timescale for work is dependent on the timescale of the choice of ROCI ASIC. Design entry will have reached the point where PCB layout can begin in mid-November if a ROCI has been tested and selected. This would meet the revised target date of prototypes in February.
A front panel layout was shown together with a model of a board.
Actions: none.

While discussing the Ge card it became clear that several aspects of the design were held up pending a decision on whether we should attempt to allow parallel operation during phase 1 or whether we should stay with common deadtime as originally proposed. There are implications in the choice of ROCI (cannot be shared between channels in parallel mode), in the ROCI readout interface, in the board layout and in the VME control. There would be a minimum of 1 month additional delay required to investigate parallel operation with no guarantee of success. The engineers unanimously agreed to make a strong recommendation to the plenary session that we decide today to use only common deadtime and accept that reworked PCBs will be required for parallel operation although most components will be reusable. (This was later agreed at the pleanary session.)

It was also noted that in 5 hybrids and the local trigger we have experienced delays due to component supply problems. McPherson urged that we pre-order components as early as possible to prevent the recurrence of such delays.

3. **BGO card**

(a) **Dual Line receiver and Discriminator** presented by Bosson.
This is a surface mount board for which the layout is finished and the pcb should be available in mid-November. Prototypes will be sent to Liverpool and Daresbury in early December after tests in Grenoble for further tests on the BGO shields. On successful completion of testing, 70 further pcbs will be ordered and populated for 2 prototype cards.
Actions: none.

(b) **Pattern Unit** presented by Bosson.
Layout of surface mount pcb will be completed during week 22-26 Oct. Component supply problems, so no target date quoted for delivery of prototypes.
Actions: none.

(c) **Spectroscopy Amplifier** presented by Bosson.
Layout of surface mount board finished. 2 prototypes due mid-November and

planned to be commissioned for early December.
Actions: none.

(d) **Test Generator** see Ge card.

(e) **Peak Detector** see Ge card.

(f) **Local Trigger** see Ge card.

(g) **TAC** see Ge card.

(h) **ADC** see Ge card.

(i) **Readout ASIC (6 channel ROCI)** presented by Bosson.
Design complete, tested and simulted. Sent to ES2 on 16 Oct. 20 devices due in early December. In the meantime the engineer will build a test card to test ROCI with ADC so this will not introduce a delay. Each ROCI is planned to cover 2 BGO shields which precludes parallel operation without redesign.
Actions: none.

(j) **Analogue Multiplexing and Digital Multiplexing** presented by Bosson.
List of signals is presented in BGO specification and was agreed to be sufficient. It was agreed that no signals will be removed from this list without consultation.
Actions: none.

(k) **DACs and Registers** see Ge card.

(l) **VME control interface** see Ge card.

(m) **ROCI readout interface** see Ge card.

(n) **Main PCB and front panel** presented by Bosson.
On target for February prototype.
Actions: none.

It was pointed out that the BGO card requires an extra DAC to program the width of the current pulse to the sumbus (20 to 200ns range is sufficient for physicists so 8 bits, 1ns per bit is enough.). Also the VETO pulse to front panel and LBUS needs to be programmable in width from 100 to 500ns (physicists will accept 100ns steps).

4. **Resource Manager**

(a) **VME buffer board** Presented by Coleman-Smith.
This has been built and prototypes are under test in England and France.
Actions: none.

(b) **CPU board** Presented by Coleman-Smith.
It was pointed out that any CPU board may be connected but that for boards other than the MVME 147 the user should consider carefully the cabling implications from the outer rows of P2 to the front panel. Struck will fully guarantee units for which they themselves have encapsulated the CPU cards.
Actions: none.

(c) **Slot 0 board** Presented by Coleman-Smith.
Pre-production prototypes of both P2 and P3 boards exist. 2 have been ordered from Struck; one for England and one for France. These are to be tested and all requested changes will be collated and applied to production units. (Costings assume 1 rework.) Richard requested that LBUS5 and LBUS6 be swapped if

possible to reduce noise problems (Controle des fenetres moves to LBUS5 and Voltage Inspection to LBUS6.)

It was pointed out that price will vary with quantity and so we should order as many as possible!

Action: Richard to inform Coleman-Smith or McPherson as soon as possible how many RM cards are required by IN2P3.

(d) **Flash ADC card** presented by Ender.

Presentation of specification of FADC card:

- 2 FADCs, each 8 bits running at between 100MHz and 6.25MHz (programmable).
- memory depth 4Kbytes per FADC. (40μs at 100MHz).
- Can be interlaced to operate as one 8 bit FADC at 200 MHz.
- Sampling edge or level sensitive.
- Glitch detector
- Digital triggering with 2 or 4 comparators for windowing.

'Optimistic' timescale target dates quoted: begin testing first prototype at end of November; working prototype by end of December, pre-production modules (3 or 4) available for use end of January. The software is proceeding in parallel but is awaiting a decision on graphics from the Eurogam software group.

Actions: none.

5. **Readout Controller (ROCO)**

Pedroza presented his proposals for a readout controller arising out of a recent meeting in Strasbourg. This led to a philosophical discussion of data flow in a system which resulted in agreement that the unit further up the hierarchy (i.e. nearer the tapes) should always request data rather than being sent it in an unsolicited manner since only the data receiver knows how much free buffer space it has. This agrees with Alexander's DT32 specification but not the proposed Readout controller. In view of this fundamental difference of opinion and and to ensure compatibility with Alexander's definitions of the DT32 bus and the VME readout scheme it was agreed that Alexander should visit Pedroza to resolve these issues and agree a detailed diagram for the readout controller.

Action: Alexander and Ring to visit Bordeaux for as long as is necessary to ensure that the ROCO interfaces to VME and DT32 are compatible with the Eurogam design, and to agree a detailed diagram of ROCO implemention.

Action: Alexander to ensure that both DT32 and VME readout are fully specified.

6. **VXI line usage**

It was agreed that since TTL trigger lines are actually TTLTRIG* (active low) so we should rename signals using them as: CODING*, READOUT*, TRANSFER_SCALERS*, CLEAR*, GO*/STOP, EVENT_REJECT*, VALIDATION3*, INHIBIT*. The event number is timed in Eurogam from an ECL validation (VALIDATION1) so it was agreed that they should also remain in ECL although we could consider changing to TTL if the ECL signals prove susceptible to VME noise. LBUS5 and LBUS6 were changed from 'not agreed' to 'agreed' in the 'Eurogam VXI line Usage' document by Lazarus on the grounds that the Eurogam RM card accepts them anyway! The proposed change so that LBUS5 becomes Controle des fenetres and LBUS6 becomes Voltage Inspection was again noted and agreed. It will be implemented on the PCB if any other changes are required on the P2 card in the RM which justify a rework.

It was agreed that the Inhibit function be separated from the Inhibit request function. Inhibit (from the trigger via RM cards) will use TTLTRIG7* (INHIBIT*) and the Inhibit request (from RM, ROCO, Ge/BGO in pipeline mode) will use ECLTRIG2 (INHIBIT_REQ). These definitions supercede the old Inhibit_C and Inhibit_D names.
Action: Coleman-Smith to write a paper to explain the use of the INHIBIT* and INHIBIT_REQ lines.

7. **Histogramming** presented by Alexander.
The specification for the histogrammer is complete and work is commencing at Liverpool to implement Alexander's specification. There was some discussion as to whether the histogrammer simply spies on the DT32 bus as a Tee connection or whether the DT32 bus loops in and out in the same way as a ROCO. Since 8 connections may be made in this regenerative loop mode before timing realignment is necessary, it was agreed that the second method is acceptable for Eurogam, having the benefit of longer possible cable runs from histogramer to event builder.
Actions: none.

8. **Trigger** presented by Lazarus.
Specification for master trigger module was distributed. Overall system will handle all proposed experiments discussed at September physics meeting. Gate and delay problems discussed arising from unpublished quirks of the AD9500; possible solution under investigation is the use of an Orsay gate and delay hybrid designed by Richard for another project. On target for February prototype. Request was made for front panel fast NIM input, INHIBIT_REQ, to allow non-VXI devices to temporarily pause trigger generation.
Actions: none.

9. **Cabling** presented by McPherson.
Plans for Daresbury cabling were explained. Richard suggested earthing the patch panels directly rather than relying on braid on RG174 to BGO front panel and superscreened coax to Ge front panel. Passed back to Horrabin for consideration.
Actions: none.

10. **System Aspects**
It was agreed that the BGO card in the Ge/BGO pair will be on the left, i.e. nearer the ROCO. This provides some extra shielding for the first Ge card from the ROCO.

    Discussed VME noise problems at various points in the meeting. Inhibit changes already noted. Main discussion was in plenary sessions.

    (During the discussion of event formats in another sub-group, Alexander and Ring and some of the software engineers agreed to add a Stop line to the DT32 bus specification to replace the Stop token.)

    Ring proposed change to ALexander's DT32 specification by adding a 'Pause' line. This led into inconclusive discussion of synchronous versus asynchronous data transfer.
Action: Alexander (with Pedroza) to a paper about DT32 data transfer based on Alexander's DT32 spec and this discussion.

11. **Crates, racks and power supplies** presented by McPherson.
    Water cooled racking proposed and agreed.
    Preamp power supplies require sensing of ±24V.
    Action McPherson to investigate cable ladders on the front of racks.

12. **Other sources of Data** presented by Lazarus.
    3 ways of bringing in data from non-Eurogam apparatus were discussed. The first 2 are possible methods for the Daresbury RMS and the third is the subject of a joint project between Strasbourg and Institute of Nuclear Physics, Cracow in Poland.

    (a) Use general purpose input card to feed data to VXI backplane and read like any other data source (Ge, BGO). (Brief specification circulated by Lazarus.)
    (b) NIM-DT32 bus converter (ROCO with NIM front end instead of VXI) to feed data onto DT32 bus.
    (c) FERA-DT32 bus converter (ROCO with FERA front end instead of VXI) to feed data onto DT32 bus. Prototype expected by end of December 1990.

    It was agreed that Strasbourg will continue work on option 3 and that DL will investigate options 1 and 2 further. It was agreed that option 1 is useful anyway for other things.
    Actions: none.

13. **Any Other Business**
    It was agreed that we need a system interconnection diagram for RM, Trigger ROCO, EB etc.
    Action: Lazarus, Alexander and Coleman-Smith to produce a system diagram.