EDOC009

EUROGAM PROJECT

NSF DATA ACQUISITION SYSTEM

Germanium Card Specification

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NSF Eletronics Development Group
UK Science and Engineering Research Council
Daresbury Laboratory

Ge Card Specification (Combined French and UK version)

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1 Introduction

This document brings together the UK and French engineer's specifications for the Eurogam Ge card and how it will fit into the system. It is an amalgamation of the French and UK documents already produced by the authors into one specification.

2 Overview of Ge card

The Ge card will be made up of several channels, each comprising several functional blocks implemented in SMT or hybrids. Each Ge card will handle between 4 and 8 channels depending on the power dissipation and space requirements of each channel. The best solution would be to have all the Eurogam Ge electronics in a single VXI crate.

Eurogam plans include large coaxial Ge detectors, and also stacks of planar detectors. Each of the 70 Ge positions in the array feeds 1 pre-amplifier when equipped with a coaxial Ge or 2 pre-amplifiers for a stack detector (assuming 4 planars in 2 pairs). A slightly different Ge card might be required for stack detectors to accommodate differences in triggering (2 pre-amplifiers produce an output from the same gamma ray), in timing (combine the 2 pre-amplifiers) and in energy (take separate energy measurements from the 2 pre-amplifiers). This will probably be possible by making changes to the coaxial card using wire links and perhaps swapping hybrids. Decision to be made in July. It is anticipated that both detector types will be used, so both types of Ge card must be built, however early orders will be for coaxial detectors, so the first Ge cards to be designed and built will be of the coaxial type.

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Figure 1 shows an overview of the card with some detail included in one Ge channel showing:

- Analogue Pulse Processing
  - Receiver and buffer
  - Shaping Amplifier (Unipolar)
  - Bipolar Amplifier
  - Timing Crossover detection (TCO)
  - Peak Detect and Hold
  - Timing Filter Amplifier (TFA)
  - Constant Fraction Discriminator (CFD)

  - Time to Amplitude Converter (TAC)

- Digitization
  - ADC
  - Sliding scale correction and serial to parallel conversion
- Readout
  - Channel Readout
  - Card Readout
- Local Trigger
- Diagnostics and Testing Facilities

In brief, the Eurogam Ge card works as follows. It accepts analogue inputs from Ge preamplifiers and produces 5 digitized outputs per input. The first three outputs are the main data: two energy outputs with low (20 MeV) and high (4 MeV) gain and one timing output which is derived from the timing of the Ge input relative to a common signal. In addition there are 2 outputs to allow ballistic deficit correction in software which are described later in this section.

The internal pulse shaping is semi-gaussian with fixed gain and fixed time constant. In the future (but not during the Daresbury phase) it will be possible to change time constants, and perhaps gain too, by swapping hybrids. It is possible to replace the filter stage with an external amplifier, for example a gated integrator.

The energy and timing outputs are only produced if a user defined global trigger condition is satisfied. In order to generate this trigger the Ge card sends information to and receives trigger signals from the system's central trigger unit. The digitized data are transferred to the crate readout controller after each event.

Ballistic Deficit and Charge Trapping Correction

With larger HPGe coaxial detectors the problems of ballistic deficit and of charge trapping become significant and must be corrected. The Ge card described in this document provides two possible methods for this, firstly the external amplifier and secondly additional internal electronics. The facility for an external amplifier allows the user to bypass the internal shaping amplifier and replace it with an external NIM unit such as the Ortec 973 Gated Integrator. The 973 is a state of the art module using novel pulse shaping before the gated integrator section. The second method uses a bipolar shaping module and a TCO pickoff module to detect a peak in the shaped input pulse. A TAC measures the time from a discriminator (CFD) to the peak, i.e. the peaking time. It is then possible to calculate and add back, in software, the charge deficit due to trapping and to ballisitic deficit based on the peak shift in time from an ideal full energy peak. The TAC word is included during readout as an extra parameter as is the digitised height of the bipolar pulse. This permits both the Goulding and Landis (Ortec 675) method and the Hinshaw (Tennelec) method of deficit correction to be used. An alternative to digitizing the bipolar pulse height is to digitize the difference between the fast bipolar pulse and the conventionally shaped pulse. The range is then much smaller.

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3 Analogue Pulse Processing

This is the section of the card which deals with the preamplifier input signal. It is the most noise sensitive in the card because of the low signal levels (typical preamplifier signal is around 400 mV for a 2 MeV gamma ray). The receiver circuit buffers the preamplifier input to the shaping amplifiers and the TFA for energy and timing respectively. The shaping amplifiers are followed by the peak detect and hold circuit which holds the analogue input for the digitizing section of the card. The TFA is followed by the CFD and the TAC from which timing information is available. The previous section describes the use of the bipolar shaping and the TCO together with a second TAC for software charge deficit correction.

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3.1 Receiver and buffer

The receiver circuit will be implemented in a hybrid. It will accept either unbalanced differential signals or a single ended signal (with the second input grounded). Output level is 4V at 20 MeV. This is the best tradeoff between S/N ratio and pileup saturation.

3.2 Semi-Gaussian Shaping Amplifier

The processing currently performed in a NIM shaping amplifier takes place in this section of the card. There are four stages of processing: firstly a differentiator with gain and PZ adjustment, secondly a semi-gaussian filter, thirdly a base line restore circuit and finally an extra gain stage for low energy gamma rays. Physicists have requested an 800 keV range to enable the use of the front element in stack detector as a low energy detector. It is not clear that VXI noise levels are low enough to implement such a high gain amplifier with a very low input signal level. Initially it is proposed that the 800 keV range is provided externally (see next section). When we have experience of implementing the 20 MeV and 4 MeV amplifiers in VXI we will be in a position to judge the feasibility of implementing the 800 keV range on the Ge card itself.

3.2.1 Gain Stage

The input stage will be implemented in a hybrid. It will differentiate the signal ready for filtering and provide pole zero compensation. The gain will be fixed and will give a 12V output for a 20 MeV gamma ray. The gain stage will saturate at 15V (i.e. 25 MeV).

The pole zero adjustment will rely on the accuracy of the preamplifier decay time constant being under ±8%, preferably under ±5%, so that only a fine adjustment is needed. Adjustment will be by a FET used as a variable resistor controlled by a DAC from software. Non-linearity will not be a problem due to the low voltage drop across the FET (few tens of mV).

3.2.2 Semi-gaussian filter

This hybrid circuit will shape the analogue pulse using a fixed time constant and a 6th order semi-gaussian shaping function. The gain will also be fixed at 1. The only way to change the time constant will be to change the module. The output level will be 12V for 20 MeV. There will also be a clipped output which can be switched to the monitoring line for PZ adjustment.

3.3 20 MeV output stage

The filter output will be buffered to provide the low gain output signal. This is a level of 12V for 20 MeV which must be attenuated to 8V for the peak detection circuit and then to 3V for the ADC.

3.3.1 Gain Stage for low energy gamma rays

There are two possible methods to provide a high gain (4 MeV) range. The first is to implement two complete energy channels, splitting after the receiver, each with its own gain and filter stages. The second method is to split after the filter hybrid with the low gain (20 MeV) channel buffered to a peak detection circuit and the high gain channel passing through an additional gain stage. The second method uses less components and hence less power and board space. It has potential problems, however, in recovery time after saturation and in amplifying noise so tests have been performed to check performance. Results are in Appendix 1 and show that the second method gives acceptable performance.

The additional gain stage for low energy gamma rays will be a hybrid implementing a fast recovery amplifier with a gain of approximately 3 giving an output level of 8V for a 4 MeV gamma ray. Bandwidth will be sufficient to handle an external gated integrator signal (see section 3.4).

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3.3.2 Baseline restore

The BLR circuit is necessary to remove baseline shifts caused by counting rate or by low frequency noise. The BLR will be implemented in a hybrid which will work by using an automatic counting rate adjustment with a fixed threshold set at around 10 keV. The BLR circuit senses the output of the high gain stage to achieve the greatest accuracy. The compensation is applied to the 20 MeV output stage which of course feeds the high gain stage. Test results are in Appendix 1. The BLR circuit will be disabled by the software command which switches to the external amplifier.

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3.4 External Amplifier (Gated Integrator)

As an interim solution, until a miniature Gated Integrator is designed for Eurogam, it will be possible to bypass the shaping amplifier stages by cabling through[1] an external NIM module such as the Ortec 973 gated integrator. This will also allow the coverage of the 800 keV range externally should it prove difficult to achieve in VXI. The external input will be connected instead of the output of the filter stage, switched by a changeover relay contact under software control. The external input will be buffered and inverted by an op-amp so as to make the conventional 0-10V input compatible with the inverted signal used internally at this point in the circuits.

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The external amplifier will feed both the 20 MeV and 4 MeV output/gain stages so that if it is set to 20 MeV full scale then we get 20 MeV and 4 MeV outputs; if it is set to 4 MeV full scale then we get 4 MeV and 800 kev outputs.

When using the external amplifier it is not useful to collect the 2 ballistic deficit data words. Either we will be using a gated integrator which compensates intrinsically, or else we

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[1] This requires that the preamplifier has two outputs; one for the GI and the other for the VXI Ge card's receiver stage which must still provide triggering and timing information.

will use very high gain and a small detector such as the front element of a stack where there is no ballistic deficit problem.

Controllable parameters are determined by the functionality of the external amplifer or gated integrator. For example the Ortec 973 provides switches for:

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- Integration time: selection of 2.5μs or 5μs.
- Gain: continuously variable from x 1.25 to x 375[2].
- PZ adjustment for preamp decay time constants from 40μs to ∞.
- PZ adjust/GI output selection switch.
- Switches for input polarity and normal/differential inputs.

3.5 Peak Detect and Hold

Both energy ranges will have their own peak detection circuit. This is a hybrid which tracks the pulse shaping output and holds the peak value for use by the ADC. It starts looking for a peak in the shaped signal when the CFD fires and stops just before the channel control logic indicates that the ADC should begin conversion.

The maximum input level will be around 8V for optimum S/N ratio. The output will pass through an attenuator to limit the maximum signal to 3V which is the limit of the ADC range.

3.6 Timing Filter Amplifier (TFA)

The TFA will be made in two different versions (both in hybrids) to cope with either stacks or coaxial detectors. The difference will be in the preset time constants for integration and differentiation (10ns integration and 100ns differentiation are the current 'best guess' for coaxial detectors). To change time constants it will be necessary to change the entire module. PZ cancellation will not be adjustable and will be preset for the nominal 50μs time constant used in the preamplifiers.

The physicists request for a 1000:1 dynamic range in the CFD cannot be implemented, but if the TFA could be built with a selectable gain, changeable by a fixed factor of 5, the CFD dynamic range requirement would be reduced to 200:1 and could be met. This is *not* a variable gain, but a factor of 5 which would be switched on or off from software.

The output will be a maximum of 5 v into 100Ω.

3.7 Constant Fraction Discriminator (CFD)

The CFD will be implemented in surface mount technology. Two versions of the CFD will be produced to match the two versions of the TFA, each having a fixed delay. The design will not include slow rise time rejection and so will behave like a leading edge discriminator at low energy[3]. The dynamic range requested by physicists of 1000:1 is not achievable; a realistic figure is between 200:1 and 300:1.

There will be several programmable parameters associated with the CFD:

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[2] With preamplifier sensitivity of 200mV per MeV, a gain of 1.25 means that a full scale 10V output represents 40 MeV, and with a gain of 375 full scale represents 133 keV. This means that the 973 can also cover the 800 keV range requirement.

[3] A more complex design will be implemented later to improve low energy behaviour.

- Threshold (12 bit DAC = 4096 steps, each step 0.5 keV over range 10 keV to 2 MeV for high gain TFA setting and 50 keV to 2 MeV for low gain TFA setting.) *12 bits is a revision to the specification suggested at March meeting.*
- Pulse Width (8 bit DAC = 256 steps over range 0 to 255ns in 1ns steps, common to all channels on a card.)[4]
- Output Delay for time alignment of pulses. (8 bit DAC. 0 to 100ns in 0.5ns steps.)

The CFD output (and the LE discriminator output) will be available via the front panel as differential ECL logic signals for anti-comptoning and rate monitoring or other operations required by users. The CFD output pulse will also switch a current source (1 mA/channel) onto the VXI analogue sumbus for a fast Ge multiplicity calculation. *Change 31 May*

3.8 Time to Amplitude Converter (TAC)

The TAC will be implemented in a Thomson ceramic resistor/transistor array. The range is 0 to 2μs with a precision of 1ns. There is also a shorter 200ns range which may be selected by changing an external capacitor (using an on-board switch). This might be useful for short lived isomers. The TAC accepts start and stop inputs of $\geq$5ns. If it receives a start and no stop it will clear itself when it goes overrange. It also accepts a reset input with pulses $\geq$10ns.
Start will be a fixed input from the CFD pulse.
Stop will be a fixed input from the front edge of the fast trigger pulse, i.e. common stop[5].

Note that the present trigger specification allows for a worst case channel to channel skew of 5ns in the fast trigger signal (TAC stop). Within a single channel the successive pulses will all arrive with exactly the same delay relative to the generation of the fast trigger pulse so there is virtually no variation with time (except for drift with voltage or temperature), only from detector to detector. The effect would only be seen when superimposing spectra and would not have any effect on the shape of any single time spectrum. The channel to channel skew comes from the crate backplane, from the board to board variation and from cables which are not matched exactly. It will be reduced by a small programmable delay in the slot 0/RM card which distributes the trigger within a crate. The problem is compounded by the fact that TAC chips will be matched to 2% from chip to chip, so typically 10ns extra channel to channel misalignment will be introduced between spectra. Again, the shape is unaffected but there is a fixed shift in position from channel to channel. *Is this a problem? If so, why and what skew would be acceptable?* *Change 31 May*

4 Digitization

Implementation is intended to be on a hybrid combining ADC, sliding scale DAC and adder, and serial to parallel chip. The sliding scale circuit is required to obtain a differential non-linearity of better than ±1%.

4.1 ADC

Each Ge channel will have 2 high resolution ADCs for the 2 energy ranges. The chosen high *Change 31 May*

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[4] The CFD pulse width defines the Ge coincidence window. Is 255ns wide enough?

[5] This means that we start the TAC with the lower rate signal and stop with the higher rate signal since the coincidence rate will usually be greater than the singles rate.

resolution ADC is the Burr Brown PCM78P 16 bit successive approximation ADC. Its input range is ± 3v, but it is intended to use only the positive half of this range unless resolution problems are encountered with this restricted range. The ADC will not be required to work to 16 bits of accuracy; the two lsbs will be discarded, leaving 13 bits of data. The PCM78P has no internal sample and hold stage, so the voltage for conversion must be held externally; in this system it will be in the Peak Detect and Hold circuit (section 3.3). The ADC converts in under 5μs using the internal clock, and may be made to convert faster using an external clock which would also synchronise all the ADCs in a crate. The ADC output is serial (MSB first), and emerges as it is generated during conversion. There are no controllable parameters in this ADC.

The Ge TAC and the ballistic deficit TAC and energy measurements will be made using low resolution ADCs. These will be 12 bit Burr Brown ADS 7800 devices which are physically smaller than the PCM78P, have built in peak detection and have a latched parallel output.

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4.2 Sliding scale correction and serial to parallel conversion

The serial to parallel conversion of hogh resolution ADC output and most of the sliding scale circuit are implemented in the same ASIC, each chip handling 8 ADCs with a common sliding scale counter. The chip also provides programmable digital upper and lower thresholds. These can be used to select certain energy or time ranges, and maybe could remove a channel from readout if the TAC indicated the detection of a neutron rather than a γ-ray? The sliding scale counter and digital subtraction stages are in the ASIC and it provides a serial output to the external DACs generating the analogue value to be added to the ADC input. The ASIC also holds the 14 bit ADC address in a register.

The low resolution ADCs will have a different readout ASIC with no serial to parallel conversion and no sliding scale.

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5 Readout

5.1 Channel Readout

Channel readout involves the reading of all ADCs on the board via the serial/parallel conversion ASICs, using the on chip windows to perform an expanded type of ‘zero suppression’ which could optionally remove empty channels and channels outside the programmable digital window. The data from the serial to parallel ASICs will be available for diagnostic purposes via VME, the ADC being selected by VME address. Channel readout takes place under the control of the local trigger section of the Ge card. Full 16 bit data is produced by the serial to parallel ASICs even if only 13 bits contain valid data.

5.2 Card Readout

Data from ADCs is matched up with 2 qualifier bits (pileup indication from local trigger section) to form a set of 32 bit words held in a FIFO. The FIFO is accessible from VME and maybe also from the VXI local bus depending on discussions currently taking place. Card readout is initiated by the central trigger unit via a readout controller in each crate.

6 Local Trigger

This is the section of the channel which controls its operation. It will be implemented as a sub-module using either an ASIC or SMT. It contributes to the formation of the global fast trigger decision and acts on the results. It also detects and signals pileup. A full description is given in a separate document describing the Eurogam Local Trigger.

Timing will be performed using a ramp generator started by the CFD over a range up to $10\mu s$. Timing points will be defined by DAC/comparator combinations using 10 bit accuracy to resolve down to 10ns. Note that the $10\mu s$ range limits the time we can wait for validations. The system trigger specification allows this time to be as long as required at the expense of deadtime, but this implementation of the Ge card will limit it to $10\mu s$. *The $10\mu s$ limit comes from the comparator having a 3V range and 3mV sensitivity which defines a 10 bit range. We can then choose to run for $5\mu s$ with 5ns steps (too short), $10\mu s$ with 10ns steps (the selected mode of operation) or longer than $10\mu s$ with coarser resolution (not worthwhile to degrade step size to cater for tiny fraction of experiments).*

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A second ramp with a range of $2\mu s$ will probably be added to give greater precision in the fast trigger timing.

6.1 Compton Suppression

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Compton Suppression will be performed in hardware using individual suppression as a method of data rate reduction. Shared suppression will be implemented in software.

For Compton Suppression the Ge card must supply a CFD output pulse for each Ge channel via the front panel for connection to an anti-Compton decision module. Anti-Compton processing is explained more fully in a separate document. For other 'user triggers' the Ge card should also provide Leading Edge discriminator outputs for each Ge channel.

It is possible that by using the 1:1 pairing of Ge:BGO cards in a crate that anti-Compton logic signals could be passed from BGO to Ge over the VXI local bus instead of over front panel cables. This option depends on the result of the local bus/VME readout decision.

6.2 Pileup

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Pre-pulse pileup is detected by using the BLR lower level threshold as a method of detecting the tail of the previous pulse. If this threshold is exceeded when the CFD fires then we have pre-pulse pileup. (The new pulse will not cause the threshold to be exceeded until $0.5\mu s$ after the CFD fires.)

Post-pulse pileup is detected by looking for a second firing of the CFD during the time that the peak detection gate is open (i.e. from initial CFD pulse to peaking time).

The effect of pileup detection is to set one of the 2 qualifier bits in the top 2 bits of the 32 bit data word. It may be possible to also reset the channel as if an 'Event reject' signal had arrived from the central trigger. The rejection would be enabled and disabled from software.

7 Diagnostics and Testing Facilities

Monitoring points will be switched to one of two VXI local bus line for observation on an oscilloscope. One or two of the following signals from any channel may be selected by software:

- Shaping amplifier gain stage output (clipped) for PZ adjustment.

- Output from shaping amplifier filter stage.
- CFD output
- TFA output
- TAC output

There will also be a test input, isolated by a relay, which provides pulses to the receiver hybrid in place of a preamplifier. The pulse amplitude will be programmable with 16 bit precision. The pulses will be provided from a transistor chopper circuit synchronised to a VXI line to allow timing setup.

8 Setup

Setup will be described in a separate document (Eurogam Setup by Mike Bentley and Ian Lazarus). The Ge card must provide facilities to allow matching of time between detectors, both within a card and from card to card.

9 Setup of Ge cards

9.1 Programmable Parameters

- Pole zero adjustment: 8 bit DAC (1 per channel)
- CFD threshold: 8 (or 12) bit DAC (1 per channel)
- CFD Output delay: 8 bit DAC (1 per channel)
- CFD width adjust: 8 bit DAC (1 per module)
- Test generator: 16 bit DAC (1 per module)
- ADC low window: separate address (4 per channel)
- ADC high window: separate address (4 per channel)
- Channel inhibit: separate address (Full word per channel)
- Channel enable: separate address (Full word per channel)
  (*Why isn't this the same address as channel inhibit with different data?*)
- Test enable: separate address (Full word per module (or channel?))
- Test disable: separate address (Full word per module (or channel?))
  (*Why isn't this the same address as test enable with different data?*)
- ADC Identifier: separate address (5 per channel)
- TFA gain (1 per channel) *Change*
- Internal/External amplifier selected. (1 per channel) *31 May*

- Local trigger parameters (all are comparator inputs to generate timings by comparing DAC output voltage with timing ramp voltage):
  - Fast trigger window end (sample point): 10 bit DAC (1 per module)
  - Validation window end (sample point): 10 bit DAC (1 per module)
  - Hold shaped signal and start conversion: 10 bit DAC (1 per module) *(Is this necessary?)*
  - Width of internal busy/deadtime signal (10 bits DAC?)
  - Start of Readout time: 10 bit DAC (1 per module)[6]

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All these parameters will be readable, returning the same value as was written to them.

The Ge card will conform to the VXI configuration and communication register scheme as set out in section C of the VXI specification.

9.2 Other settings

The following settings may be adjusted by electronics support staff (**NOT** users):

- Link (or switch) to ground one side of receiver input to change from differential input to single ended.
- Link (or switch) capacitors to swap TAC range between 200 ns and 2 μs.

10 Mechanical and Electrical Specification

This section defines the electrical and mechanical interface for all signals which will pass through either the front panel or the VXI bus.

10.1 Mechanical Interface

- All VXI connections are fully defined mechanically in the VXI bus Specification and require no further definition.
- Front panel connectors are used for inputs from preamplifiers and external shaping amplifiers (GI) and for outputs from the CFDs used in anti-Compton logic and the LE signals for user triggers.
  - All signals from preamplifiers will come into the unit via BNC sockets, 2 per preamplifier (to allow differential operation). Total 8–16 BNC sockets. *Only 4–8 with BNC sockets floating instead of grounded. Is this useful/desirable? What about interference and EPD?*
  - All Gated Integrator ouputs will come into the unit via BNC sockets, one per channel. Total 4-8 BNC sockets.
  - All front panel CFD and LE outputs will go through IDC ribbon cable connectors (e.g. 3M M50 system). Total one 34 way connector including grounds and 8-16 differential signals.

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[6] May be derived from ADC EOC output or something similar without timing.

10.2 Electrical Interface

All VXI signals will conform to the VXI bus specification. VXI Local Bus signals will be either single ended ECL or IEEE P1194 BTL (Futurebus) drivers except for the analogue monitoring line (section 7). *Change 31 May*

Analog sumbus will receive 1 mA per active Ge channel.

Front panel CFD and LE outputs will be differential ECL.

11 Software Interface

Each board, i.e. 4 to 8 Ge channels, will occupy one VXI Logical Address. The board will provide configuration registers within the 64 byte area allocated to its Logical Address in accordance with the VXI specification.

The map of internal registers will be defined later. The setup parameters to be included will be found in section 9.1. In addition there will be 20 VME addresses (one per ADC) for diagnostic data readout and one VME address from which the card readout FIFO is accessible. There are over 100 VME addresses per board, so the offset register at 06_{16} will be used to point to the area of memory space containing the registers. *Should we put either commonly used registers or registers common to all Ge channels in the device dependent register area of the 64 byte address space?*

The Ge boards will be Register based VXI devices. *Does anyone think they should be message based devices? Why? Dynamic configuration doesn't appear to be worth the extra complication either so is not planned.*

Appendix 1. Test Results

The following test results were obtained by Alphonse Richard and his engineers using a NIM prototype of the pulse shaping circuits connected to a GeLi detector using a preamplifier set to 100mV/MeV. Amplifier time constant was set to 2μs.

Using single extra gain stage for 4 MeV energy and shared filter

- **Noise** due to amplifier on 4 MeV range measured at about 0.3 keV which does not significantly affect the resolution. (This is 10μV rms referred to the input.) *Change 31 May*
- **Energy Resolution** measured to be the same as commercial Intertechnique 7200 and Silena 7611 amplifiers (2.5 keV with old GeLi).
- **Rate degradation**. Up to 20K counts/second the energy resolution degradation is 10%.
- **Overload** of 4 MeV channel with 20 MeV gamma ray results in pulse recovery time lengthening by 3μs (1.5 τ).
- **Power dissipation** measured at 2 watts.

Baseline restore

The BLR circuit was tested up to 20K counts/sec and performance is comparable to the commercial amplifiers mentioned in the previous section.