8 Memory Map of the G.I.R. for the BGO Card

8.1 VXI Configuration Registers: (Inside the G.I.R.)

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11).

***VXI Base Address** first card*	***Description***	***DATA Format***
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8a	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

8.2 Channel Area Addresses

Channel 1 (0x1000 --0x10FE)	**Bus Width**	**Read/ Write**	**Function**
0x1000	16	w	Dac Adjustment no.1
0x1002	16	r/w	Channel Control Register 2 bits (bit0= enable/disable*) (bit1= set/reset*)
Channel 2 (0x1100 --0x11FE)	**16**	**r/w**	**Function**
0x1100	16	w	Dac Adjustment no.2
0x1102	16	r/w	Channel Control Register 2 bits (bit0= enable/disable*) (bit1= set/reset*)
Channel 20 (0x2300 --0x23FE)	**16**	**(r/w)**	**Function**
0x2300	16	w	Dac Adjustment no.20
0x2302	16	r/w	Channel Control Register 2 bits (bit0= enable/disable*) (bit1= set/reset*)

8.3 Common Area Addresses

8.3.1 Common DACs:

VME Address	**Bus Width**	**R/W**	**Function**
0x2400	16	w	FT Sample Adjustment
0x2500	16	w	ValSample Adjustment
0x2600	16	w	VETO Adjustment
0x2700	16	w	Spare Dac

8.3.2 Common Registers:

Global Addresses	**Bus Width**	**Read/ Write**	**Function**
0x10	16	r/w	Module Control Register (MCR)
0x20	16	r/w	Digital Inspection 1 channel select
0x22	16	r/w	Digital Inspection 1 parameter Select
0x24	16	r/w	Digital Inspection 2 channel select
0x26	16	r/w	Digital Inspection 2 parameter Select
0x28	16	r/w	Analog Inspection 1 channel select
0x2A	16	r/w	Analog Inspection 1 parameter Select
0x2C	16	r/w	Analog Inspection 2 channel select
0x2E	16	r/w	Analog Inspection 2 parameter Select
0x30	16	r/w	Voltage Inspection channel select
0x32	16	r/w	Voltage Inspection parameter Select
0x40--0x5E	16	r/w	Analogue Card Configuration Registers (XCProm)
0x60--0x70	16	r/w	Default DAC Buffer values in XCProm for non volatile mode
0x80--0x90	16	w only	Change Default DAC Buffer mode in Volatile mode
0xA0--0xBE	16/32	r/w	G.I.R. Readout Memory Map
0x100--0x17C	32	r/w	Saroc 1 Setup

0x180--0x1FC	32	r/w	Saroc 2 Setup
0x200--0x27C	32	r/w	Saroc 3 Setup
0x280-0x2FC	32	r/w	Saroc 4 Setup

8.3.2.1 <u>Module Control Register:</u> VME base Address : 0x10

Bit Number	Meaning when = 0	Meaning when = 1
0	not yet defined	not yet defined
1	not yet defined	not yet defined
2	Sliding Scale Counter Off	Sliding Scale Counter On
3	If SS off, force SS DAC to 0V	If SS on, force SS DAC to 9V
4	Analog Card PROM Write Disable	Analog Card PROM Write Enable
5	not yet defined	not yet defined
6	not yet defined	not yet defined
7	not yet defined	not yet defined
8	Reset FIFO Disable	FIFO Reset
9	Reset G.I.R. Disable	G.I.R. Reset
10	Not Last Card	Last Card (use terminators)
11	not yet defined	not yet defined
12	not yet defined	not yet defined
13	not yet defined	not yet defined
14	not yet defined	not yet defined
15	not yet defined	not yet defined

8.3.2.2 <u>Digital inspection lines:</u>

<u>Digital Inspection line 1 :</u> VME base Address : 0x20 (channel Select), and 0x22 (parameter Select)
<u>To Disable the Digital inspection Line 1 write 0x00 at address 0x22.</u> DigselA[5..0]
<u>Digital Inspection line 2 :</u> VME base Address : 0x24 (channel Select), and 0x26 (parameter Select).
<u>To Disable the Digital inspection Line 2 write 0x00 at address 0x26.</u> DigselB[5..0]

parameters Line1 = DigselA[5..0] Line2 = DigselB[5..0]	GIR Control Lines to Analogue Card DigselA[2..0] DigselB[2..0]	GIR Control Lines to Analogue Card DigselA[5..3] DigselB[5..3]	Data Value for channel Address	Data Value for Parameter Address
Disable	xxx	110	xxxx	00
TACS Channel 1 to 8	000..111	000	0x 00 to 0x07	01
TACS Channel 9 to g	000..111	010	0x08 to 0x0F	01
TACS Channel h, j, k	000..010	100	0x10 to 0x12	01
TACOR	011	100	0x 13	01
FTRINT	100	100	0x14	01
FTSAM	101	100	0x15	01
VALSAM	110	100	0x16	01
VETO	111	100	0x17	01
SEDO1 to 8	000..111	001	0x00 to 0x07	02
SEDO9 to g	000..111	011	0x08 to 0x0F	02
SEDOh, j, k,m	000..011	101	0x10 to 0x13	02
G.I.R. Parameters	**GIR Control Lines**		**Data Value for channel Address**	**Data Value for Parameter Address**
Fast_Trigger	0x001		0x 20	0x001
Inhibit	0x002		0x 20	0x002
Validation	0x003		0x 20	0x003
Veto	0x004		0x 20	0x004
OrValack	0x005		0x 20	0x005
OrDeadTime	0x006		0x 20	0x006
StartReadoutSAROC	0x007		0x 20	0x007
Renin (SAROC)	0x008		0x 20	0x008
SAROCDTready0	0x009		0x 20	0x009
SAROCDTready1	0x00A		0x 20	0x00A
SAROCDTready2	0x00B		0x 20	0x00B
SAROCDTready3	0x00C		0x 20	0x00C
SAROCDTack_buf	0x00D		0x 20	0x00D
SAROCEmpty0	0x00E		0x 20	0x00E
SAROCEmpty1	0x00F		0x 20	0x00F
SAROCEmpty2	0x010		0x 20	0x010
SAROCEmpty3	0x011		0x 20	0x011
SAROCLPASS	0x012		0x 20	0x012
CSA *(FifoChipSelect_A)	0x013		0x 20	0x013
CLKA(FifoClock_A)	0x014		0x 20	0x014

ENA(Fifo Enable Port_A)	0x015		0x 20	0x015
AS* (VME)	0x016		0x 20	0x016
DS (DS0* and DS1*) (VME)	0x017		0x 20	0x017
R/W* (VME)	0x018		0x 20	0x018
ModRoco	0x019		0x 20	0x019
CardRenin *(From ROCO)	0x01A		0x 20	0x01A
BLTACK (Card)	0x01B		0x 20	0x01B
BLTACK (Bus)	0x01C		0x 20	0x01C
OE_Ident*	0x01D		0x 20	0x01D
CSB* (FifoChipSelect_B)	0x01E		0x 20	0x01E
CLKB (FifoClock_B)	0x01F		0x 20	0x01F
ENB (Fifo Enable Port_B)	0x020		0x 20	0x020
OR_fifo (EmptyFlag)	0x021		0x 20	0x021
FDTACK	0x022		0x 20	0x022
DTACK* (VME)	0x023		0x 20	0x023
CardRenout(Bus Renout)	0x024		0x 20	0x024
SysClk	0x025		0x 20	0x025
LT_Reset*	0x026		0x 20	0x026
Readout_Event_Match	0x027		0x 20	0x027
Reset_Fifo*	0x028		0x 20	0x028
Decode_Sel(CardChipSelect)	0x029		0x 20	0x029
Strobe_Dec2	0x02A		0x 20	0x02A
Dclk	0x02B		0x 20	0x02B
DCS*	0x02C		0x 20	0x02C
DDin	0x02D		0x20	0x02D
Coding_Bus	0x02E		0x20	0x02E
Coding_GIR	0x02F		0x20	0x02F
Event Fault more than one	0x030		0x20	0x030
Readout Event Fault	0x031		0x20	0x031
Vme Address 1	0x032		0x20	0x032
Vme Address 2	0x033		0x20	0x033
Vme Address 3	0x034		0x20	0x034
Vme Address 4	0x035		0x20	0x035
Vme Address 5	0x036		0x20	0x036
Not Used (DI Disable)	Disable		value not = 0x20	xxxx

8.3.2.3 Analog inspection lines:

Analog Inspection line 1 : VME base Address: 0x28 (channel Select), & 0x2A (parameter Select).
To Disable the Analog inspection Line 1 write 0x00 at address 0x2A.
Analog Inspection line 2 : VME base Address: 0x2C (channel Select), & 0x2E (parameter Select).
To Disable the Analog inspection Line 2 write 0x00 at address 0x2E.

Parameters Line1 = AnaselA, AnEnA Line2 = AnaselB, AnEnB	GIR Control Lines to Analogue Card AnaselA[3..0] AnaselB[3..0]	GIR Control Lines to Analogue Card AnEnA[3..1] AnEnB[3..1]	Data Value for channel Address	Data Value for Parameter Address
TAO1 to 8	0000..0111	001	0x00 to 0x07	01
TAO9 to g	0000..0111	010	0x08 to 0x0F	01
TAOh, j, k,m	0000..0011	100	0x10 to 0x13	01
SUMO	0100	100	0x14	01
0V	0101	100	0x15	01
GIO1 to 8	1000..1111	001	0x00 to 0x07	02
GIO9 to g	1000..1111	010	0x08 to 0x0F	02
GIOh, j, k	1000..1010	100	0x10 to 0x12	02
GISum	1011	100	0x13	02

8.3.2.4 Voltage inspection line:

VME base Address : 0x30 (channel select), and 0x32 (parameter select).
To Disable the Voltage Inspection line : write 0x00 at address 0x32

parameters	GIR Control Lines to Analogue Card Vsel[3..0]	GIR Control Lines to Analogue Card Venable[2..1]	Data Value for channel Address	Data Value for Parameter Address
Discr. Thr. 1 to g	0000..1111	01	0x00 to 0x0F	01
Discr. Thr. h, j, k,m	0000..0011	10	0x10 to 0x13	01
FTRSPC	0100	10	0x14	01
VALSPC	0101	10	0x15	01
VETOC	0110	10	0x16	01
DAC24	0111	10	0x17	01
SLSCV	1000	10	0x18	01

+2.5 V	1001	10	0x19	01
0V	1010	10	0x1A	01

8.3.2.5 BGO Configuration Registers (Analogue part):

VXI Base Address	*Description*	*DATA Format*
0x40	In Read Mode this is the Man. ID	D7..D0 from XCPROM
0x42		
0x44		
0x46		
0x48	Read Only: Serial no.	Read 8 bits only from XCPROM d7 to d0
0x4a	Read Only: Modification Level	Read 8 bits only from XCPROM d7 to d0

8.3.2.6 BGO DAC Buffer Control Memory Map (non volatile):

Base Addresses	Bus Width	Read/ Write	Function
0x60	16	r/w	Default DAC Buffer **1** values from XCProm
0x62	16	r/w	Default DAC Buffer **2** values from XCProm
0x64	16	r/w	Default DAC Buffer **3** values from XCProm

8.3.2.7 BGO DAC Buffer Setup Memory Map (volatile):

Base Addresses	Bus Width	Read/ Write	Function
0x80	16	write only	Change Default DAC Buffer **1** mode in XCProm
0x82	16	write only	Change Default DAC Buffer **2** mode in XCProm
0x84	16	write only	Change Default DAC Buffer **3** mode in XCProm

8.3.2.8 G.I.R. Readout Memory Map : VME base Address : 0xA0 to 0xBE.

Base Addresses	Bus Width	Read/ Write	Function
0xA0	16	r/w	Event Counter Register
0xA2	16	r/w	Item + Group no. Register
0xA0	32	read only	Item + Group no. Register + Event Counter
0xA4	32	r/w	Fifo Test Enable
0xA8	16	r/w	G.I.R. Readout Control Register (RCR)
0xAA	N.A.	r only w only	Start Readout Saroc in test mode End Readout Saroc in test mode
0xAC	16	r only	Readout, Temperature Status Register
0xAE	16	r/w	Valack Timeout Register (multiple of 62.5 ns) (100 <t< 4 sec.) (active when bit2 of RCR is 1) e.g. to have 100 us timeout write the value 0x640 (1600).
0xB0	32	r only	Qstat1,Qstat0 counter (16 bit each). The Qstat1 counter is to count the number of event faults difference more than one. Qstat0 counter for the number of event faults
0xB4 to 0xBE	N.A.	r/w	Not yet Implemented

8.3.2.8.1 G.I.R. Readout Control Register (RCR) (*not fixed*):

VME base Address : 0xA8 to be upgraded

Bit Number	Meaning when = 0	Meaning when = 1
0	Run mode for SAROC readout	Test mode for SAROC readout
1	Run mode for External readout	Test mode for External readout
2	Disable Valack Timeout Reset	Enable Valack Timeout Reset
3	Enable Readout from G.I.R.	Disable Readout from G.I.R. (card is bypass)
4	Not yet defined	Not yet defined
5	no pipelining at all (dead until VXI Readout ends)	Pipeline Readout stage (dead until data are in FIFO) (N.A.Y.)
6	Event Number Readout off	Event Number Readout on
7	Common Deadtime Readout mode (Eurogam I & II)	Euroball Readout mode
8	DSP set to Slave Mode(N.A.Y.)	DSP set to Master Mode(N.A.Y.)
9	DSP Slave is not last Slave Card(N.A.Y.)	DSP Slave is the last Slave Card(N.A.Y.)
10	Contrôle des fenêtres off(N.A.Y.)	Contrôle des fenêtres on(N.A.Y.)

11	Use Event Number Q = 00 given by 0xa2 register	Use Event Number Q from G.I.R. (qstat1,qstat0) (see table below)
12	Not yet defined	Not yet defined
13	Not yet defined	Not yet defined
14	Not yet defined	Not yet defined
15	Not yet defined	Not yet defined

(N.A.Y.) (Not Available Yet)

8.3.2.8.1.1 G.I.R. Qstatus Table:

Qstat1:Qstat0	**Meaning When Set**
00	Trigger Broad cast nibble is equal to G.I.R. event counter Least Significant Nibble
01	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **more than one**
10	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **one**

8.3.2.8.2 G.I.R. Readout Status Register (*not fixed*): VME base Address : 0xAC

Bit Number	**Meaning when = 0**	**Meaning when = 1**
0	G.I.R. Temperature indicator is above the upper threshold	G.I.R. Temperature indicator is below the upper threshold
1	G.I.R. Temperature indicator is below the lower threshold	G.I.R. Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Valack Timeout deasserted	Valack Timeout asserted
8	Empty Flag of Fifo1 asserted	Empty Flag for Fifo1 deasserted
9	Full Flag of Fifo1 asserted	Full Flag for Fifo1 deasserted
10	Empty Flag of Fifo2 asserted	Empty Flag for Fifo2 deasserted
11	Full Flag of Fifo2 asserted	Full Flag for Fifo2 deasserted
12	Global Saroc_Empty asserted	Global Saroc_Empty deasserted
13	Status: No fault	Status: fault 0
14	Status: No fault	Status: fault 1
15	Status: No fault	Status: fault 2