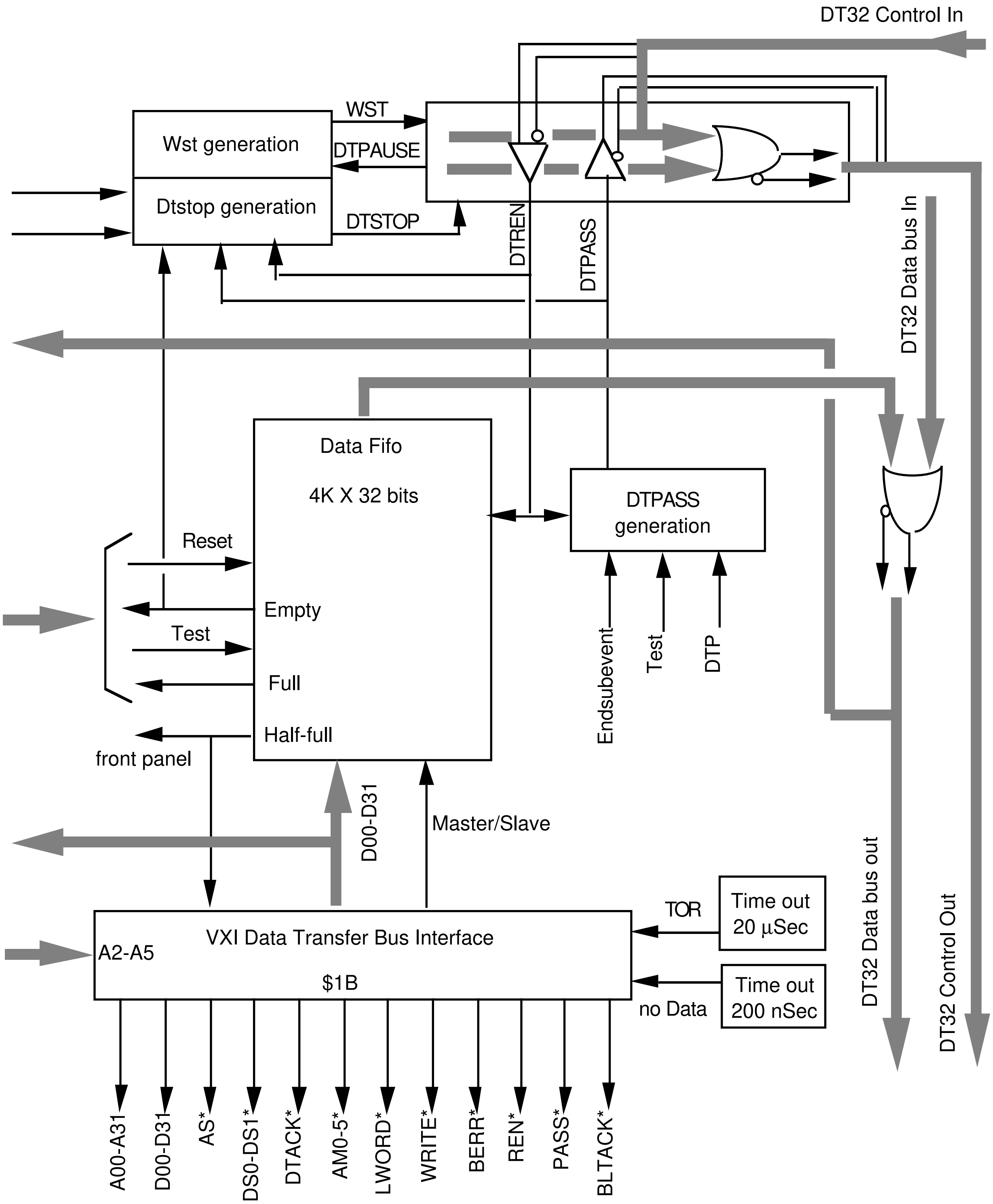
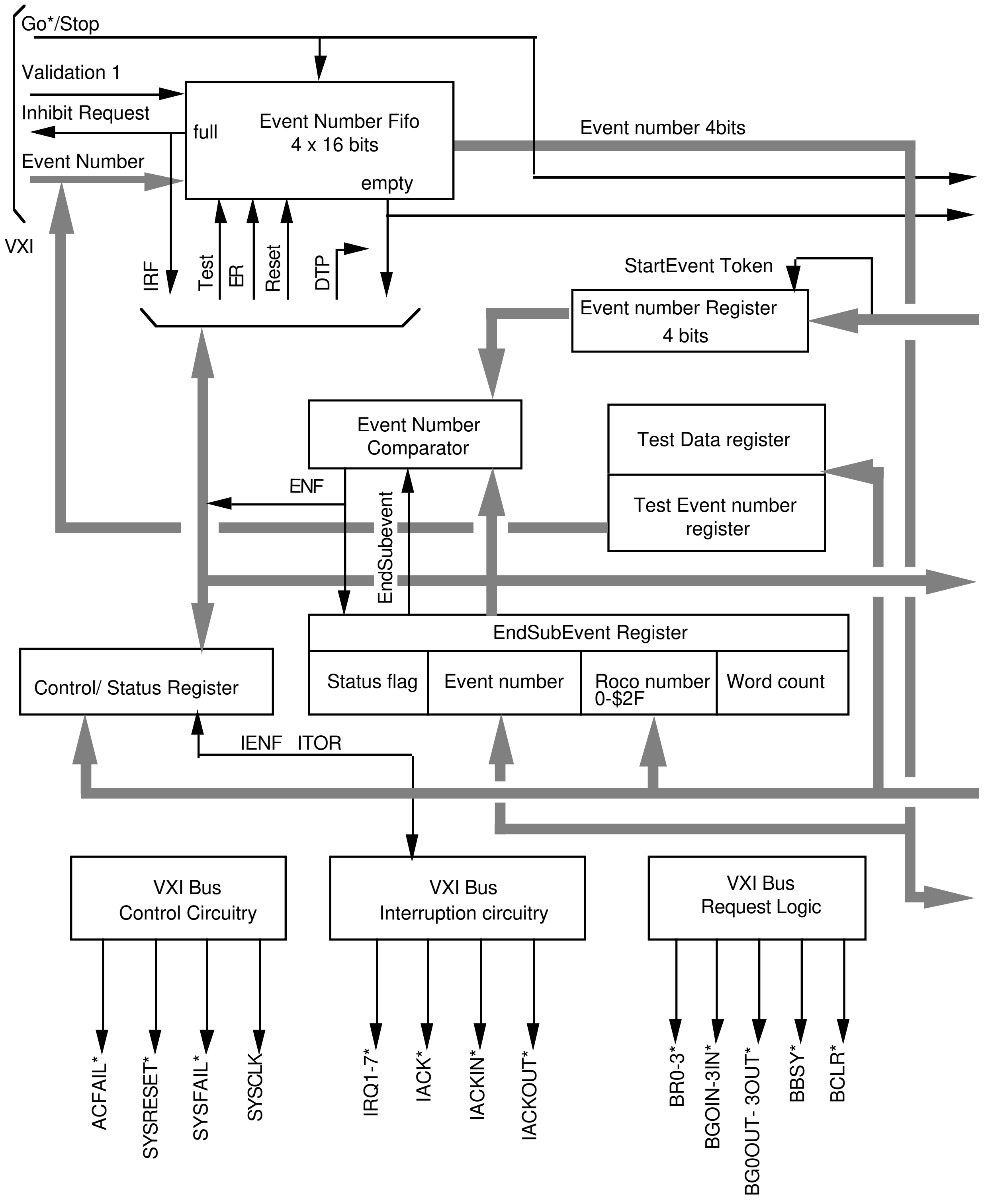


<u>Figure 7: Architecture</u> (Without VXI registers) (Sheet 2 of 2)



<u>Figure 7: Architecture</u> (Without VXI registers) (Sheet 1 of 2)

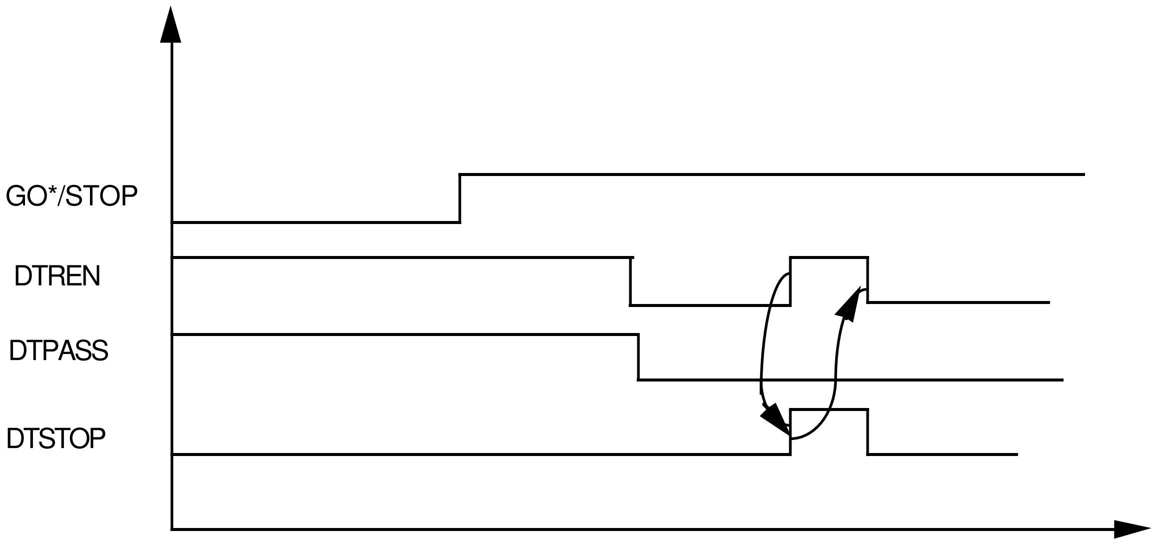
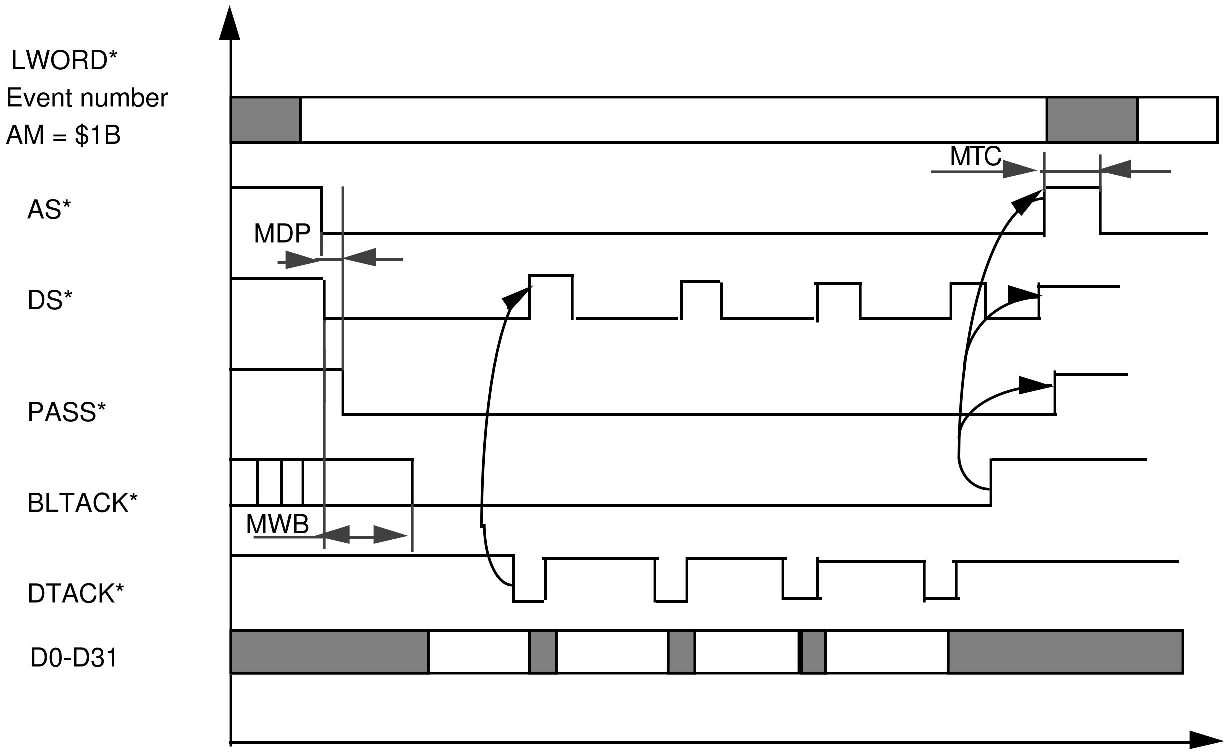
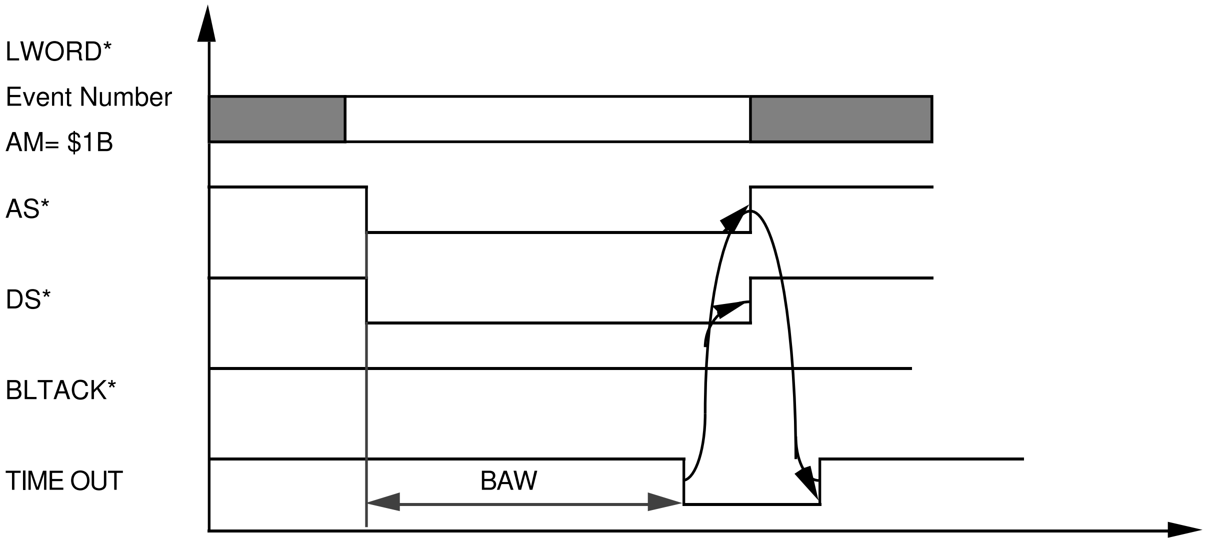


Figure 6 DTSTOP DTREN handshake



MDP : Maximum delay Pass 10 nSec
MWB: Maximum Wait Bltack* 200 nSec
MTC : Minimun time between Ren-Readout cycles 100 nSec

Figure 4 Readout timing



BAW: BLTACK* ASSERTION WAIT Minimum 200 nSEc

Figure 5 Readout timing without data

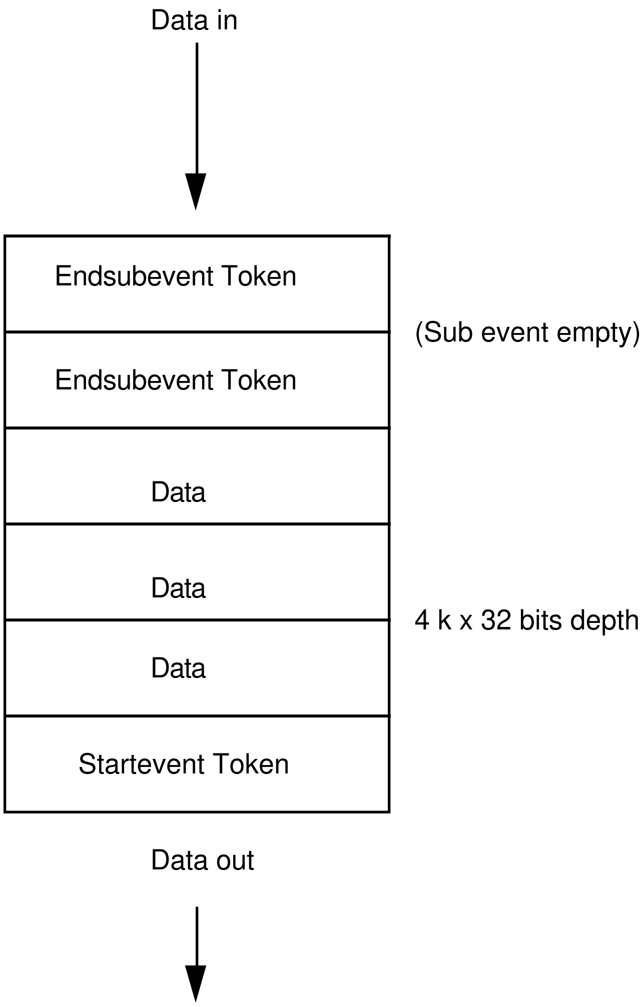


figure 3: data structure of the data fifo (a sample)

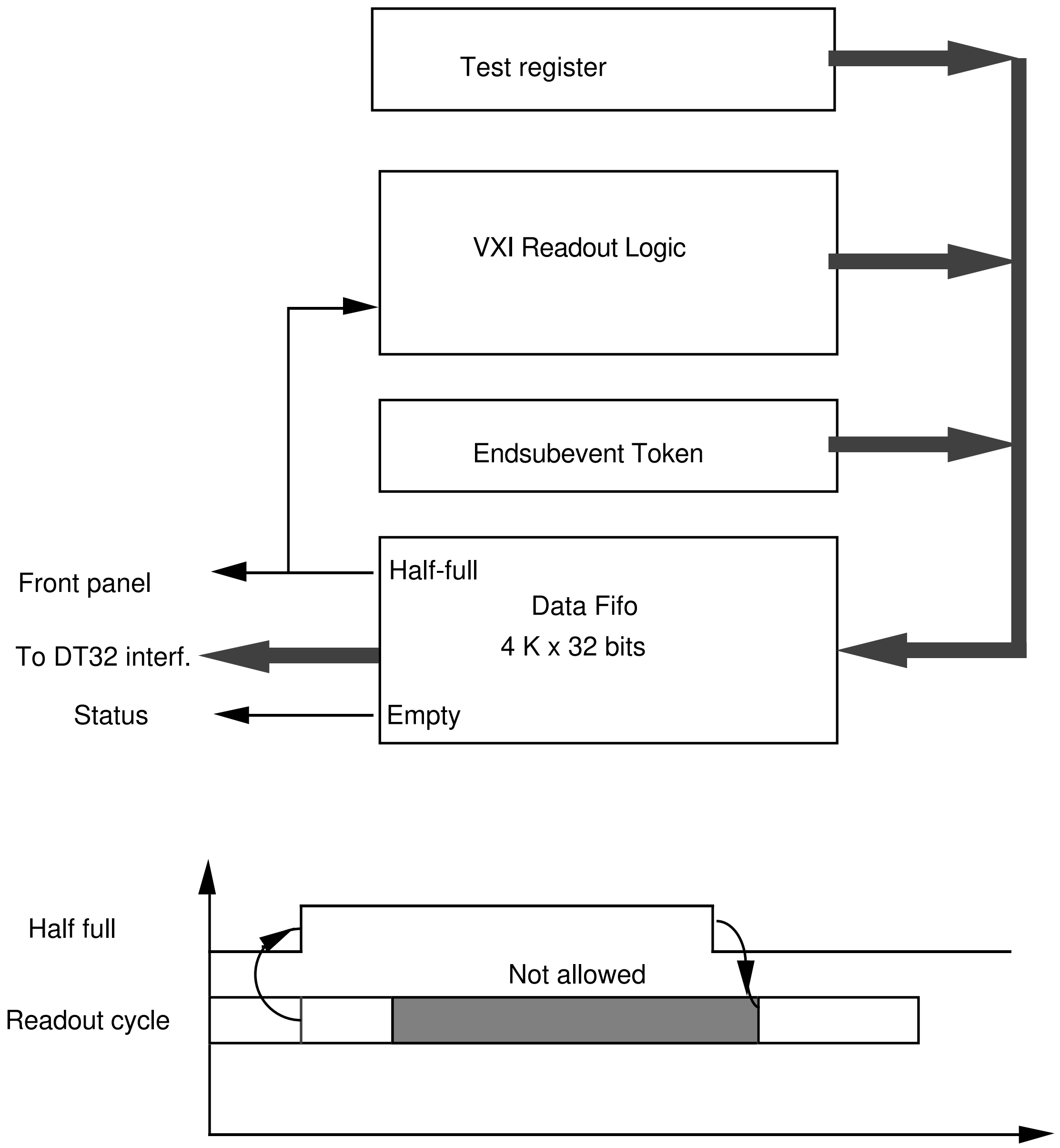
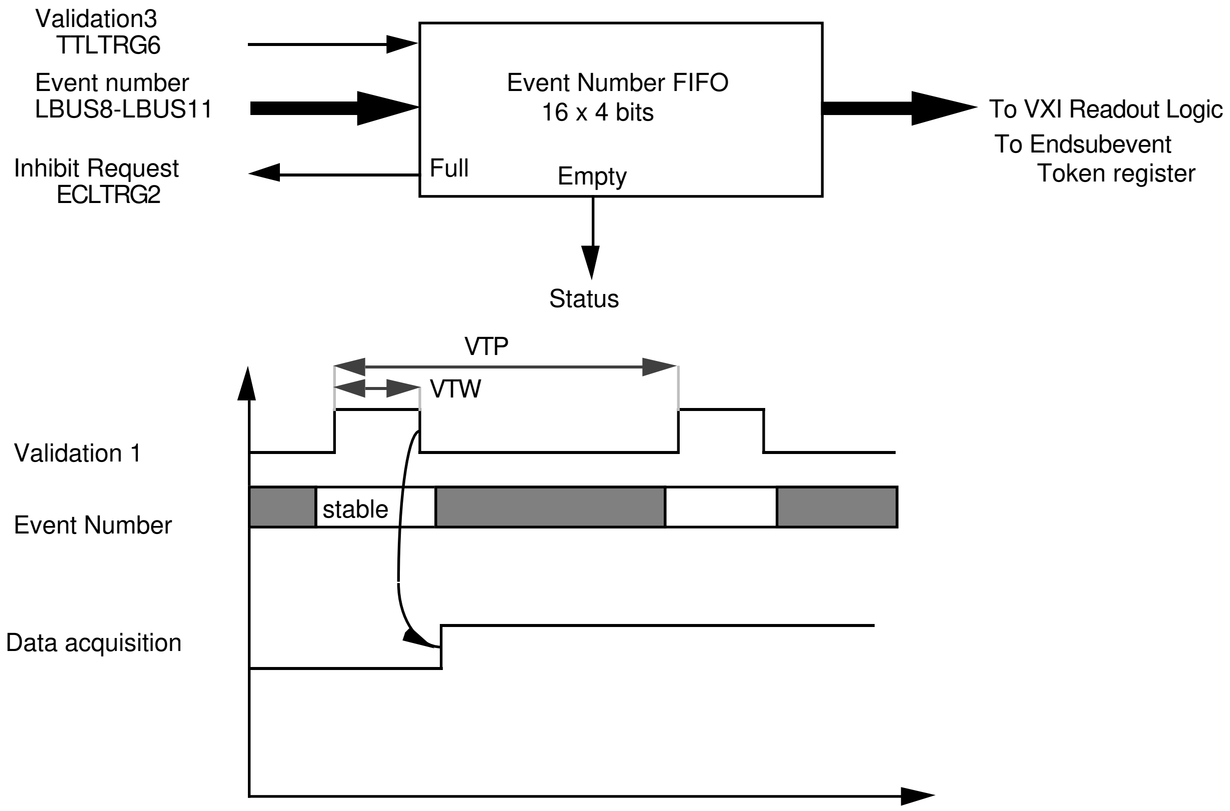


Figure 2: Data Fifo block diagram



VTW Validation Typic Width 200 nSec.
VTP Validation Typic Period 2 µSec.

<u>Figure 1 Master trigger interface</u>

VIII-4)VXI readout interface

```
if  (ROCO master on VME bus AND Data Fifo NOT Half-Full)
      if Event number ready from Event number fifo
               assert (AM0-AM5=$1B AND A02-A05=Event number AND LWORD*)
               assert (AS* AND DS0* AND DS1* AND PASS*)
               while (NOT BLTACK* OR delay ≤ 200 ns)
                         wait
               end(of while)
               while  (NOT BERR* OR NOT local time out)
                         while BLTACK*
                                   if NOT (DS0* AND DS1*)
                                             assert (DS0* AND DS1*)
                                   end(if)
                                   while NOT DTACK*
                                   end(of while)
                                   pass D00-D31 to data fifo logic
                                   deassert (DS0* AND DS1*)
                                   while DTACK*
                                   end(of while)
                         end(of while)
               end(of while)
               deassert (AS* AND DS0* AND DS1* AND PASS AND AM0-AM5 AND LWORD*
)
               build        ENDSUBEVENT Token
      end(if)
end(if)
```

IX) Actions on SYSRESET

On SysReset two actions are provided:
 -clear the data fifo,the Event Number fifo
 -desable the ROCO (bit ER cleared in the Control/status register).

X) VXI bus addresses of the ROCO

The ROCO is dynamically configured,register based A16 device. See VXI specification

VIII-3)DT32 inteface operations

VIII-3-1) Store the Event number

```
if WST true
        if StartEvent token
                store Event number in event number register
        end(if)
end(if)
```

VIII-3-2) Readout protocol

```
while (GO*/STOP high AND data fifo Empty AND Event number fifo empty)
        if (DTREN AND NOT DTPASS)
                assert DTSTOP
        end(if)
        while DTREN
        end(of while)
        deassert DTSTOP
end(of while)
if (DTREN AND NOT DTPASS)
        while data fifo valid
                get next data fifo
                while DTPAUSE
                end(of while)
                put data on DT32 bus
                assert WST
                deassert WST
        end(of while)
        assert DTPASS
end(if)
while DTREN
end(of while)
deassert DTPASS
```

VIII-1-2) Read Event Number Fifo

```
while NOT FIFO EMPTY
        while NOT VXI readout section hold
                pull event number
                pass to VXI readout section
        end(of while)
end(of while)
```

VIII-2) Data fifo operations

VIII-2-1) Write the data fifo

```
if ROCO master on VME bus
        while NOT data fifo Full
                if VXI readout data valid
                        push the data in data fifo
                        update word-count
                end(if)
                if Endsubevent token ready
                        push Endsubevent token in data fifo
                        update word-count
                end(if)
        end(of while)
else
        if TEST bit set
                while NOT data fifo full
                        if test data register written
                                push the test data register in data fifo
                        end(if)
                end(of while)
        end(if)
end(if)
```

VIII-2-2) Read the data fifo

```
        if DTREN
                while NOT Endsubevent token
                        pull data from data fifo
                        send data to DT32 interface
                end(of while)
                pull Endsubevent token
                if Event number from Endsubevent token ≠ Event number from START TOKEN
                        Event number fault
                end(if)
                send Endsubevent token to DT32 interface
        end(if)
```

VII-10) Register map for ROCO

REGISTER	OFFSET
Manufacturer ID	0
Model Code	2
VXI Status /Control	4
[Offset]	6
Serial Number	8
Modification Level	10
EndSubEvent Token	12
Data Fifo Test	16
Event Number Test	20
ROCO Status/control	22
Time Out 1	24
Time Out 2	26
Interruption/Bus request	28

VIII) Operations:

VIII-1) Master trigger Interface operations

VIII-1-1) Write Event Number Fifo

```
while ER
    while Not STOP
        if TEST bit set
            if Test event number register written
                push register in event number fifo
            end(if)
            while event number fifo full
                assert INHIBIT REQUEST
            end(of while)
        else
            while VALIDATION1
                push EVENT NUMBER on leading edge of
VALIDATION
                while event number fifo full
                    assert INHIBIT REQUEST
                end (of while)
            end(of while)
        end(if)
    end(of while)
end(of while)
```

VII-7) Interruption registers

This register (8 bits,write only) is used to select the interruption level and the bus request level.

-Interruption level bits select the level from 0 to 7.
-Bus request level bits select the level of bus request from 0 to 3.
These bits are located like this:

D7	D6	X	X	X	D2	D1	D0
BR1	BR0				IRQ2	IRQ1	IRQ0

the lower level for the bus request is done for BR0 and BR1 =0
the higher level for the bus request is done for BR0 and BR1=1
the lower level for an Interruption request is done for IRQ0 , IRQ1 and IRQ2 =0 (The IT request is masked)
The higher level for an Interruption request is done for IRQ0 ,IRQ1 and IRQ2 =1

VII-8) VXI standard registers

Three registers will be configured as register-based device: the ID register and the Device Type register.

-The ID register (16 bits) holds the device class (Register based),the address space (A16) and the manufacturer ID (offset 0) on read.On write,this register holds the logical address of the ROCO.

-The device type register (16bits) holds the Model Code (offset 2).For the Roco,the model code is 256.

-The Status and Control VXI register.

Control register:
Only the bit 0 is significant,It is the RESET bit.
Reset is set by writing to 1 and is cleared by writing 0,or by SYSRESET*.

Status register:
bit 0 : reflect of Reset bit in control register.
bit 2 :passed =1
bit3 :ready =1
bit14 : modid*

The others bits are not implemented.

VII-9) VXI user specified registers

Two registers:
-The serial number register (offset 8) is a 16 bits register containing the serial number
of the ROCO.
-The modification level (offset 10) is a 16 bits register which contains the modification level.This wil be particular to each ROCO.

readout cycle is terminated.A local Time out implemented on the ROCO is also able to assert TOR in case this was not provided by the Resource Manager.

-ENF: When enabled (1) in control register,this bit,with the TEST bit set is used to test the fault mode.In normal Mode (TEST bit clear) the ENF bit in status register is true if the event number of StartEvent Token is not the same than the Event number of the EndSUbEvent Token out of the data fifo.

Reading the status register from the Resource Manager clear the TOR and ENF bits in test mode and in normal mode.

VII-3) Word count

16 bits register.This is the count of the number of words in a subevent.The word count includes the EndSubevent word.The 12 LS bits of the word count are included in the last word put on the DT32 bus (End of Sub event token).See figure 3 ,data structure.This register is not accessible via the VME bus.

VII-4) Test registers

Two registers are implemented:

-a 32 bits write only register.Writting in this register causes the data to be pushed in the data fifo if the TEST bit of control register is enable

-a 4 bits register (write only) where the event number written is pushed in the Event number fifo if the TEST bit of control register is enable.

They are enabled when the TEST bit of the Control/Status register is set .

The data fifo of the first ROCO in the daisy chain is written with a STARTEVENT token and some data.The others ROCO's data fifos are written with data and a ENDSUBEVENT token.The first ROCO's data fifo is the last written to begin the DT32 transfer.

Writting an event number in the 4 bits register simulates the receipt of a validation pulse,and its event number from the Master Trigger.Then the software can load data into the data fifos on the GE and BGO cards (if these are in test mode).The ROCO can read them out,using a REN-Readout cycle ,by writting to this 4 bits ROCO register.Then the ROCO transmits this data on the DT32 bus,as normal.

VII-5) Event number register

This register (4 bits) store the event number from the Start event token when the DT32 bus is in activity.This register is not accessible via the VME bus.

VII-6) Time Out registers

Two registers (16 bits,write only) are implemented:

-Time Out 1 register to select the local time out for TOR. (see control/status register)

-Time Out 2 register to select the maximun wait for BLTACK* (see figure 4)

VII-2) Control /status register

16 bits registers,the control register is write only,the status register is read only.Reading the status register returns the control register contents,except the RESET bit.

bit	Name	Control register	status register
d0	ER	Enable ROCO	- - - - - - -
d1	RESET	Reset	0
d2	TEST	Test	- - - - - - -
d3	IRF	Inhibit Request on ENF	- - - - - - -
d4	IENF	Interrupt on ENF Enable	- - - - - - -
d5	ITOR	Interrupt on Time-out enable	- - - - - - -
d8	FNE	- - - - - - -	Fifos not Empty
d9	EFF	- - - - - - -	Event number fifo full
d10	DFF	- - - - - - -	Data fifo full
d11	DTP	DTREN transmit to DTPASS	- - - - - - -
d14	TOR	Time out on vxi readout	Time out on vxi readout
d15	ENF	Event Number Fault	Event number Fault

-ER: When disabled (0) the ROCO will not store events,performs a vxi readout,transfers on DT32 bus.

-RESET: Writing this bit to one start a RESET procedure.The Event Number and Data fifos are cleared.All the ROCO registers are cleared,except the control register.The Reset bit is always clear (0) in the status register.

-TEST: When this bit is set (1),use of the two test registers (data fifo test register and event number test register) is enabled.The ROCO will not accept VALIDATION3 inputs from the Master Trigger.

-IRF: Asserts the output Inhibit Request on ENF.

-IENF: When enabled (1) in control register,an interruption request is asserted by ROCO on Event Number Fault .This interrupt request is passed to the VME bus.

-ITOR: When enabled (1) in the control register,an interruption request is asserted on the VME bus on Time Out during a VXI readout.

-FNE,EFF,DFF: three bits giving the status of the ROCO's fifos.

-DTP:when enabled (1),this bit tell the ROCO to always transmit DTREN to DTPAS without trying to transmit any data and to check the event number.This allow software to test one ROCO-VXI crate without having to move any DT32-bus cable.

-TOR: When enabled (1) in the control register,this bit,with the TEST bit set is used to test the fault mode on time out.In normal mode (TEST bit clear) the TOR bit in status register is true if the BERR* line is asserted by the Resource Manager during a vxi readout.Then,the

VI)-1 DTSTOP

The first ROCO asserts DTSTOP when :

-the VXI backplane GO*/STOP is high (STOP is true)

-The Data fifo and Event number fifo are empty (the last event is put out of cards,the master trigger must not do a new VALIDATION when the GO*/STOP line is high on the VXI backplane).

-the DTREN input is true,that is the EVENT BUILDER try to read a new event,thus the last event has been read.

-the DTPASS,that is the DTREN of the next ROCO is false.

The DTSTOP handshakes with the DTREN input.See figure 6.
If there is an error during the last event,another ROCO may asserts DTSTOP instead DTPASS.
The event builder must check the integrity of the event to ensure that every ROCO has send its EndSUbEvent token.

VI-2) DTPAUSE

Pause is asserted by the HSM interface,to tell that the HSM has not accepted the last data word (i.e no ackn).This line in an input on all the ROCOs modules.Pause prohibits a new write strobe (WST) on DT32 bus when it is asserted.
The ROCO which writes data on DT32 bus may sense the pause request later,so a fifo on HSM interface must be used.

VII) Roco registers

some registers are required, they are:

- device dependant registers:
  - ENDSUBEVENT REGISTER
  - CONTROL/STATUS REGISTERS
  - WORD COUNT
  - DATA FIFO TEST REGISTER
  - EVENT NUMBER TEST REGISTER
  - EVENT NUMBER REGISTER
  - TIME OUT REGISTERS
  - INTERRUPTION/BUS REQUEST REGISTER
- vxi standart registers:
  - REGISTER BASED DEVICE/MANUFACTURER ID/LOGICAL ADDRESS
  - DEVICE TYPE REGISTER/MODEL CODE
  - STATUS/CONTROL REGISTER
- vxi user specified registers:
  - SERIAL NUMBER
  - MODIFICATION LEVEL

VII-1) ENDSUBEVENT register

32 bits register where:

d31-d30	=	error field	= 00 on initialisation
d29-d24	=	Roco Number	= RN $0 \leq RN \leq \$2F$
d23-d16	=	End of sub event flag	= $FF
d15-d04	=	Word count	
d03-d00	=	Event number	

the bits D00-D15 are genered by the ROCO
the bits D16-D31 are written from VME,but the bit d31 is also set by a ROCO if ENF is true

IV) VXI readout interface

The ROCO uses the VME bus ROR algorithm.After its initialisation,if the Enable Bit of the control register is set and the Test bit is clear,ROCO is the master on the VMEbus(See VII Roco Registers).If the resource manager takes the bus master ship,the ROCO requests again the bus when there is one event number at least in the Event number Fifo.The ROCO is master on VME until the resource manager requests the bus master.When the resource manager requests the bus master, ROCO gives the bus after the VME data transfer is done.
The VXI readout sequences are:

1) Normal readout
2) No data
3) Error on readout

IV-1) Normal Readout

When an event number is pulled out of the Event Number fifo,the BLTACK* line is asserted by the cards which have data to be readout.(See figure 4)
The readout is according to the specification of the VXI Read Out mechanism (Alexander,version 0.92)

IV-2) No Data

If BLTACK* is not asserted within 200 ns,ROCO terminates the readout cycle (figure 5).

IV-3) Error

If the DS* line is asserted during more than 102µs,the resource manager may asserts BERR*,then the readout cycle is terminate with an error during readout.Else a local time out is implemented on ROCO in case the BERR* is not provided by the resource manager.

V) Data fifo

The data fifo,used to store sub events from data acquisition in the VXI crate can hold at least 16 sub events.That is the size is 4k x 32 bits (see figure 3).
If there is not enough space to store a new subevent in the data fifo,a "Half Full" signal from the data fifo is used to prohibit the read out cycle (figure 2).The block data transfer on VME bus is not allowed,to prevent a locking during the readout.

VI) DT-32 interface

The first ROCO (master trigger crate) reads the STARTEVENT TOKEN from the TRIGGER unit where the event number is stored.This is the first word of an event.This word is passed on the DT-32 bus.
All ROCOs store the 4 bits event number of StartEvent Token from DT32.
All the data are pulled from the data fifo and put on the DT-32 bus(with the DTREN-DTPASS handshake for the daisy chain) until the EndSubevent token is reached.
A comparison is made with the event numbers from StartEvent token and EndsubEvent token. If there is a difference the ROCO asserts "Event Number Fault".An error bit is set in the ROCO-status register and a flag is set in the ENDSUBEVENT TOKEN.
The data transfer works without handshake,that is HSM write strobe is used without acknowledge
Two lines on the DT-32 bus are included: DTSTOP and DTPAUSE.

EUROGAM PROJECT

Read-Out COntroller ROCO VXI unit Specification

J.L. Pedroza March 1991

Edition 2.4

This is a document to present the Read Out controller VXI board or ROCO unit to transfer data from the VXI instrumentation towards the EVENT BUILDER and HISTOGRAMMER.This is the result of a meeting at CENBG between M.M. ALEONARD,J. ALEXANDER,J.C. GOUILLAUD,C.RING and the author.The major notes used to define the ROCO are : Specification of the VXI readout mechanism (Eurogam project J.R. Alexander) DT32-bus specification (Eurogam project J.R.Alexander)

I) Introduction

The ROCO is a VXI board sitting at the right of the RESOURCE MANAGER board.It insures the fast reading of data through the VXI backplane and transfers these data to a HSM interface in the Event Builder crate.
There is one ROCO board per VXI crate.Several ROCO units may be daisy chained to transfer data from several VXI crates to the Event Builder crate.In this daisy chain,some specific ROCO (eg ROCO FERA) may be included to read data from a CAMAC crate with LECROY 4300 ADCs.
The first ROCO to transfer data to the Event Builder is located in the VXI crate holding the MASTER TRIGGER unit.

II) The ROCO's functions

To complete the VXI readout,the data transfer on DT-32,the Master Trigger connection,the VME-VXI functions the ROCO unit contains five blocks.

- -the Master Trigger interface
- -the VXI readout interface
- -the data fifo to store subevents
- -the DT32 interface
- -the registers to control and check the ROCO.

III) Master Trigger interface

During a data acquisition on VXI crate,some validations may appear (figure 1).A fifo is used to store event numbers latched by VALIDATION3(TTLTRG6) during the data acquisition procedure.This fifo is the EVENT NUMBER FIFO.If this fifo is full,an INHIBIT-REQUEST is asserted and is send to the MASTER TRIGGER module via the RESOURCE MANAGER(ECLTRG2).
The data of each event are stored on the acquisition cards,until the ROCO read them.