Eurogam VXI line usage

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1 Introduction

This document describes my understanding of the conclusions of a meeting between engineers involved in Eurogam from UK, France and Germany held at Daresbury on 16th July 1990. The paper under discussion which contains much more detail was produced by Alphonse Richard (dated 13/7/90) after a meeting held between French engineers in Paris on 8th June who tried to cover the needs of *all* French VXI instrumentation for nuclear structure physics, not solely Eurogam.

Where I refer to changes, they relate to the proposal mentioned above, *'Utilisation des Lignes VXI'* by Alphonse Richard dated 13/7/90.

2 VXI lines

2.1 Local Bus

- LBUS0 Supplementary analogue sumbus 1 *agreed, unchanged*
- LBUS1 Supplementary analogue sumbus 2 *agreed, unchanged*
- LBUS2 Analogue inspection line 1 *agreed, unchanged*
- LBUS3 Analogue inspection line 2 *agreed, unchanged*
- LBUSA4 RENin LBUSC4 RENout (Readout ENable daisy chain) *agreed, unchanged*
- LBUS5 Voltage inspection line *NOT AGREED, see note 1* †
- LBUS6 Contrôle des fenêtres *NOT AGREED, see note 2* †
- LBUS7 not allocated †
- LBUS8 Event Number *agreed, but see note 3* †
- LBUS9 Event Number *agreed, but see note 3* †
- LBUS10 Event Number *agreed, but see note 3* †
- LBUS11 Event Number *agreed, but see note 3* †
- LBUS12 Reserved (Anti-Compton veto in Eurogam) †
- LBUS13 Reserved (Anti-Compton veto in Eurogam) †
- LBUS14 Reserved (Anti-Compton veto in Eurogam) †
- LBUS15 Reserved (Anti-Compton veto in Eurogam) †
- LBUS16 Reserved (Anti-Compton veto in Eurogam) †
- LBUS17 Reserved (Anti-Compton veto in Eurogam) †
- LBUS18-35 not allocated. †

2.2 ECLTRG 0-5

- ECLTRG0 Validation 1 *agreed, unchanged*
- ECLTRG1 Synchronisation of triggers for test mode *agreed, unchanged*
- ECLTRG2 Inhibit (D size) *agreed, unchanged*
- ECLTRG3 Logic inspection line 1 *agreed, unchanged*
- ECLTRG4 Logic inspection line 2 *agreed, unchanged*
- ECLTRG5 Validation 2 *agreed, unchanged*

2.3 TTLTRG 0-7

- TTLTRG0 End of coding *agreed, unchanged*
- TTLTRG1 End of readout *agreed, unchanged*
- TTLTRG2 Transfer all scalers to shadow registers. *agreed, unchanged*
- TTLTRG3 Clear *agreed, unchanged*
- TTLTRG4 Go/Stop *agreed, unchanged*
- TTLTRG5 Event reject *agreed, unchanged*
- TTLTRG6 Validation 3 *agreed, unchanged*
- TTLTRG7 Inhibit (C size) *agreed, unchanged*

2.4 STAR lines

- STARX Fast trigger *agreed, but see note 4*
- STARY Fast trigger *agreed, but see note 4*

2.5 Sumbus

- SUMBUS *agreed, unchanged but see note 5*

2.6 VME lines

VME lines are used for setup, executing normal VME cycles, and for readout in a slightly non-standard method defined in a separate document.

2.7 Other Lines

All lines in this section are as defined in the VXI specification

- CLK10
- CLK100
- SYNC100
- MODID(00-12)

3 Notes

These notes describe changes made and reasons for the changes.

3.1 Note 1

It was not agreed that a third analogue inspection line must be defined for measuring voltages. It was suggested that 2 are enough, and that if any more than 2 analogue signals need to be measured simultaneously then on card ADCs with VME readout should be used. It was agreed that the Eurogam slot 0 card will have a strap to connect its slow ADC to either an analogue inspection line or to LBUS5 (voltage inspection line) in case LBUS5 is reallocated.

3.2 Note 2

It was not agreed to allocate a VXI local bus line to window adjustment since the adjustment can be made using the logic inspection lines. It was agreed that we will explain the two methods to the physicists, and only if there is a strong preference for the analogue method would the line could be allocated. (The UK physicists expressed no strong preference for either method when asked.)

3.3 Note 3

These lines were changed from TTL to single ended ECL since they are sent with the validation signals, 2 of which are ECL. ECL will also introduce less backplane noise than TTL during analogue processing. It is not agreed whether we use these lines in 2 pairs as proposed or use all 4 of them with validation to identify the event and then use VME address lines to select which of the 16 possible events will be read. (VME address lines can also be used during local bus readout if a VME cycle precedes/accompanies local bus readout.

3.4 Note 4

STARX and STARY were changed such that both are usable in either direction. Thus the 'Dècision logique' usage and the 'Trigger Rapide' usage is possible on one line or on two lines. In Eurogam it is possible (with coaxial detectors) to make each Ge card handle one pentagon, so the STARX/Y line could represent a hit in a certain pentagon. Alternatively, with two mixed detector types in the same crate, we might want to introduce slightly different fast trigger signals or a very fast validation.

3.5 Note 5

Note that the proposal limits the VXI SUMBUS to –1.6 Volts whereas the VXI specification allows ±3 Volts

3.6 Other comments

It was suggested that we could introduce classes of conformance so that all signals in class 1 *must* be used as specified or left alone; those in class 2 should be used as specified if possible, but may be re-allocated for a good reason, for example to gain lines for local bus readout. All the signals mentioned in this document would be class 1 signals except for Voltage inspection (LBUS5), Contrôle des fenêtres (LBUS6), Event number (LBUS8-11) and Anti-Compton vetos (LBUS12-17) allowing LBUS5-LBUS35 to be used for local bus readout in a future system. These class 2 signals are denoted in the list by the †symbol.

I believe that these lines should remain in class 2 at least until we have a working VME readout scheme with a satisfactory data throughput. At this point we can judge whether it is worth continuing to regard these lines as class 2 to facilitate an easy upgrade to Euroball which will use local bus readout anyway or whether we can say that Eurogam will never require readout faster than the measured VME rate and thus that these lines may be exclusively defined as proposed.