9 Memory Map of the G.I.R. for the Ge Card

9.1 VXI Configuration Registers: (Inside the G.I.R.)

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11).

VXI Base Address *(slot 1)*	***Description***	***DATA Format***
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8a	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

9.2 Channel Area Addresses

Channel 1 (0x1000 --0x10FE)	**Bus Width**	**Read/ Write**	**Function**
0x1000	16	w	Dac Adjustment no.1 (see Dac Memory Map below)
0x1010	16	r/w	Channel Control Register 4 bits (bit0= enable/disable*, bit1= Test Gen. enable/disable*,bit2 & 3 free)
Channel 2 (0x1100 --0x11FE)	**16**	**r/w**	**Function**
0x1100	16	w	Dac Adjustment no.2(see Dac Memory Map below
0x1110	16	r/w	Channel Control Register 4 bits
Channel 8 (0x1700 --0x17FE)	**16**	**(r/w)**	**Function**
0x1700	16	w	Dac Adjustment no.8(see Dac Memory Map below
0x1710	16	r/w	Channel Control Register 4 bits

9.2.1 DAC Memory Map:

This applies to all channel DAC setup for Address 0x1000 to 0x100e , and 1100 to 110e (channel 1&2) up to (channel 7& 8), because every two channels share two DACs A&B.

Channel 1 (0x1000 --0x10FE)	**DAC A/B**	**G.I.R. DAC parameter Value**	**DAC Parameter Name**
0x1000	A	0	CFD Threshold channel 1
0x1002	A	4	CFD Output DELAY Channel 1
0x1004	A	2	PZ Threshold Channel 1
0x1006	A	6	FT Sample Threshold Channel 1
0x1008	B	0	Val Threshold Channel 1
0x100a	B	4	Pileup Threshold Channel 1
0x100c	B	2	WatchDog Threshold Channel 1
0x100e	B	6	Bipolar Cross over Channel 1
0x1100	A	1	CFD Threshold channel 2
0x1102	A	5	CFD Output DELAY Channel 2
0x1104	A	3	PZ Threshold Channel 2
0x1106	A	7	FT Sample Threshold Channel 2
0x1108	B	1	Val Threshold Channel 2
0x110a	B	5	Pileup Threshold Channel 2
0x110c	B	3	WatchDog Threshold Channel 2
0x110e	B	6	Bipolar Cross over Channel 1

9.2.2 DAC Memory Map:

This Table shows the hardware parameter's list of the DACs parameters w.r.t. their effective position.

Channel 1 (0x1000 --0x10FE)	**DAC A/B**	**G.I.R. DAC parameter Value**	**DAC Parameter Name**
0x1000	A	0	CFD Threshold channel 1
0x1100	A	1	CFD Threshold channel 2
0x1004	A	2	PZ Threshold Channel 1
0x1104	A	3	PZ Threshold Channel 2
0x1002	A	4	CFD Output DELAY Channel 1
0x1102	A	5	CFD Output DELAY Channel 2

0x1006	A	6	FT Sample Threshold Channel 1
0x1106	A	7	FT Sample Threshold Channel 2
0x1008	B	0	Val Threshold Channel 1
0x1108	B	1	Val Threshold Channel 2
0x100c	B	2	WatchDog Threshold Channel 1
0x110c	B	3	WatchDog Threshold Channel 2
0x100a	B	4	Pileup Threshold Channel 1
0x110a	B	5	Pileup Threshold Channel 2
0x100e	B	6	Bipolar Cross over Channel 1
0x110e	B	7	Bipolar Cross over Channel 2

9.3 Common Area Addresses

9.3.1 Common DACs:

VME Address	Bus Width	R/W	Function
0x0000	16	w	CFD Width Adjustment
0x0002	16	w	Test Generator amplitude Adjustment

9.3.2 Common Registers:

Global Addresses	Bus Width	Read/ Write	Function
0x10	16	r/w	Module Control Register (MCR)
0x20	16	r/w	Digital Inspection 1 channel select
0x22	16	r/w	Digital Inspection 1 parameter Select
0x24	16	r/w	Digital Inspection 2 channel select
0x26	16	r/w	Digital Inspection 2 parameter Select
0x28	16	r/w	Analog Inspection 1 channel select
0x2A	16	r/w	Analog Inspection 1 parameter Select
0x2C	16	r/w	Analog Inspection 2 channel select
0x2E	16	r/w	Analog Inspection 2 parameter Select
0x30	16	r/w	Voltage Inspection channel select
0x32	16	r/w	Voltage Inspection parameter Select
0x40--0x5E	32	r/w	Test acces to data FIFO
0x60--0x70	16	r only	Read Default DAC Buffer values from XCProm
0x60--0x70	16	w only	Set Default DAC Buffer Values in XCPROM for non volatile mode
0x80--0x90	16	w only	Change Default DAC Buffer Setup in Volatile mode
0xA0--0xBE	16/32	r/w	Readout Setup
0x100--0x17C	32	r/w	Saroc 1 Setup
0x180-0x1FC	32	r/w	Saroc 2 Setup

9.3.2.1 Module Control Register: VME base Address : 0x10 **a vérifier avec Nab**

Bit Number	Meaning when = 0	Meaning when = 1
0	Mark Pileup & Veto Events	Reject Pileup & Veto Events
1	TFA Gain setting X 1	TFA Gain setting X 3
2	Sliding Scale Counter Off	Sliding Scale Counter On
3	If SS off, force SS DAC to 0V	If SS on, force SS DAC to 9V
4	Not Allocated	Not Allocated
5	Pipeline Off (dead until data in STR8080)	Pipeline On (dead until data in GIR FIFO)
6	Event Number Readout On	Event Number Readout Off
7	Common Deadtime Readout	Parallel Readout
8	Reset FIFO Disable	Reset FIFO
9	Reset G.I.R. Disable	G.I.R. Reset
10	Not Last Card	Last Card (use terminators)
11	Not Allocated	Not Allocated
12	Not Allocated	Not Allocated
13	Not Allocated	Not Allocated
14	Event Number Q set by 0x12	Use real Event Number Q
15	Status: FIFO empty	Status: FIFO not empty

9.3.2.2 Digital inspection lines:

Digital Inspection line 1 : VME base Address : 0x20 (channel Select), and 0x22 (parameter Select)
To Disable the Digital inspection Line 1 write 0x00 at address 0x22. LI1_OEx-x+1[3..0]
Digital Inspection line 2 : VME base Address : 0x24 (channel Select), and 0x26(parameter Select).
To Disable the Digital inspection Line 2 write 0x00 at address 0x26. LI2_OEx-x+1[3..0]

parameters Line1 = LI1_OEx-x+1[3..0] Line2 = LI2_OEx-x+1[3..0]	GIR Control Lines to Analogue Card SRCELI [3..0]	GIR Control Lines to Analogue Card LI1-OEx-x+1[3..0] LI2-OEx-x+1[3..0]	GIR Control Lines MUX_CH_SEL	Data Value for channel Address	Data Value for Parameter Address
Disable	0x0	0x0	1	0x00	xx
End of FlatTop(Shap.Amp.)1	0x1	0x1	0	0x01	0x01
LT Reset output 1	0x2	0x1	0	0x01	0x02
FT sample 1	0x3	0x1	0	0x01	0x03
Val sample 1	0x4	0x1	0	0x01	0x04
4MeV serial D out of ADC 1	0x5	0x1	0	0x01	0x05
Tac Reset (Start TAC) 1	0x6	0x1	0	0x01	0x06
Valack 1	0x7	0x1	0	0x01	0x07
Pre-pulse Pileup Indicator 1	0x8	0x1	0	0x01	0x08
Convert input to ADC 1	0x9	0x1	0	0x01	0x09
ADC Clock 1	0xA	0x1	0	0x01	0x0A
CFD Delayed 1	0xB	0x1	0	0x01	0x0B
CFD Direct 1	0xC	0x1	0	0x01	0x0C
End of FlatTop(Shap.Amp.)2	0x1	0x1	1	0x02	0x01
LT Reset output 2	0x2	0x1	1	0x02	0x02
FT sample 2	0x3	0x1	1	0x02	0x03
Val sample 2	0x4	0x1	1	0x02	0x04
4MeV serial D out of ADC 2	0x5	0x1	1	0x02	0x05
Tac Reset (Start TAC) 2	0x6	0x1	1	0x02	0x06
Valack 2	0x7	0x1	1	0x02	0x07
Pre-pulse Pileup Indicator 2	0x8	0x1	1	0x02	0x08
Convert input to ADC 2	0x9	0x1	1	0x02	0x09
ADC Clock 2	0xA	0x1	1	0x02	0x0A
CFD Delayed 2	0xB	0x1	1	0x02	0x0B
CFD Direct 2	0xC	0x1	1	0x02	0x0C
Channel 3 & 4 same values	see above	0x2	see above	0x03 to 0x04	see above
Channel 5 & 6 same values	see above	0x4	see above	0x05 to 0x06	see above
Channel 7 & 8 same values	see above	0x8	see above	0x07 to 0x08	see above
Not Used all Chan(Disable)	0x0	0x0	x	0x01 to 0x08	0x0D to 0x1F

G.I.R. Global Parameters	GIR Control Lines			Data Value for channel Address	Data Value for parameter Address
Disable				*0x20*	*0x000*
Fast_Trigger	0x001			0x20	0x001
Inhibit_buf (M.T.)	0x002			0x20	0x002
Validation	0x003			0x20	0x003
Veto	0x004			0x20	0x004
OrValack	0x005			0x20	0x005
Conversion DTime (coding)	0x006			0x20	0x006
StartReadoutSAROC	0x007			0x20	0x007
Renin (SAROC)	0x008			0x20	0x008
SAROCDTready0	0x009			0x20	0x009
SAROCDTready1	0x00A			0x20	0x00A
OR8CFD-Delay	0x00B			0x20	0x00B
Inhibit Card	0x00C			0x20	0x00C
SAROCDTack_buf	0x00D			0x20	0x00D
SAROCEmpty0	0x00E			0x20	0x00E
SAROCEmpty1	0x00F			0x20	0x00F
Readout Event Fault	0x010			0x20	0x010
Readout Event Match	0x011			0x20	0x011
SAROCLPASS	0x012			0x20	0x012
CSA *(FifoChipSelect_A)	0x013			0x20	0x013
CLKA(FifoClock_A)	0x014			0x20	0x014
ENA(Fifo Enable Port_A)	0x015			0x20	0x015
AS* (VME)	0x016			0x20	0x016
DS (DS0* and DS1*) (VME)	0x017			0x20	0x017
R/W* (VME)	0x018			0x20	0x018
ModRoco	0x019			0x20	0x019
CardRenin *(From ROCO)	0x01A			0x20	0x01A
BLTACK (Card)	0x01B			0x20	0x01B
BLTACK (Bus)	0x01C			0x20	0x01C
OE_Ident*	0x01D			0x20	0x01D
CSB* (FifoChipSelect_B)	0x01E			0x20	0x01E
CLKB (FifoClock_B)	0x01F			0x20	0x01F
ENB (Fifo Enable Port_B)	0x020			0x20	0x020
OR_fifo (EmptyFlag)	0x021			0x20	0x021
FDTACK	0x022			0x20	0x022

DTACK* (VME)	0x023			0x20	0x023
CardRenout(Bus Renout)	0x024			0x20	0x024
SysClk	0x025			0x20	0x025
LT_Reset*	0x026			0x20	0x026
Oe_Global	0x027			0x20	0x027
Reset_Fifo*	0x028			0x20	0x028
DecodeSel(CardChipSelect)	0x029			0x20	0x029
Strobe_Dec2	0x02A			0x20	0x02A
Dclk	0x02B			0x20	0x02B
DCS*	0x02C			0x20	0x02C
DDin	0x02D			0x20	0x02D
Coding_Bus	0x02E			0x20	0x02E
ExternalReset_ LT	0x02F			0x20	0x02F
Readout Event Fault more than 1	0x030			0x20	0x030
Spare2	0x031			0x20	0x031
Vme Address 1	0x032			0x20	0x032
Vme Address 2	0x033			0x20	0x033
Vme Address 3	0x034			0x20	0x034
Vme Address 4	0x035			0x20	0x035
Vme Address 5	0x036			0x20	0x036
Not Used (DI Disable)	Disable			valus not = 0x20	xxxx

9.3.2.3 Analog inspection lines:

Analog Inspection line 1 : VME base Address: 0x28 (channel Select), & 0x2A (parameter Select).
To Disable the Analog inspection Line 1 write 0x00 at address 0x28. AID[3..0], AI1-OEx_x+1[3..0]
Analog Inspection line 2 : VME base Address : 0x2C (channel Select), and 0x2E (parameter Select).
To Disable the Analog inspection Line 2 write 0x00 at address 0x2C. AID[7..4], AI2-OEx-x+1[3..0]

Parameters for channel 1 & 2	GIR Control Lines to Analogue Card AID [3..0] AID [7..4]	GIR Control Lines to Analogue Card AI1-OEx-x+1 [3..0] AI2-OEx-x+1 [3..0]	Data Value for channel Address	Data Value for Parameter Address
4 MeV energy 1	1111	0001	0x01	00
20 MeV energy 1	1110	0001	0x01	01
Bip. Sig for Peak tim. 1	1101	0001	0x01	02
TFA output 1	1100	0001	0x01	03
TAC output 1	1011	0001	0x01	04
FT ramp 1	1010	0001	0x01	05
VAL ramp 1	1001	0001	0x01	06
Pre-amp Sig (1st Buf) 1	1000	0001	0x01	07
4 MeV energy 2	0111	0001	0x02	00
20 MeV energy 2	0110	0001	0x02	01
Bip. Sig for Peak tim. 2	0101	0001	0x02	02
TFA output 2	0100	0001	0x02	03
TAC output 2	0011	0001	0x02	04
FT ramp 2	0010	0001	0x02	05
VAL ramp 2	0001	0001	0x02	06
Pre-amp Sig (1st Buf) 2	0000	0001	0x02	07
Not used(Disable) 1 & 2	0111	0000	xxxx	08 to FF

For the others channels, the AI1-OE [3..0] lines are changed :

AI1-OE [3..0], AI2-OE [3..0] = 0x0010 for the channels 3 - 4
AI1-OE [3..0], AI2-OE [3..0] = 0x0100 for the channels 5 - 6
AI1-OE [3..0], AI2-OE [3..0] = 0x1000 for the channels 7 - 8

9.3.2.4 Voltage inspection line:

VME base Address : 0x30 (channel select), and 0x32 (parameter select).
To Disable the Voltage Inspection line : write 0x00 at address 0x30.

parameters	GIR Control Lines to Analogue Card AMD [3..0]	GIR Control Lines to Analogue Card MTOEx-x+1 [3..0]	Data Value for Channel Address	Data Value for Parameter Address
CFD Threshold 1	0000	0001	0x01	00
CFD Threshold 2	0001	0001	0x02	00
CFD out delay Thres. 1	0010	0001	0x01	01
CFD out delay Thres. 2	0011	0001	0x02	01
PZ Adjustment 1	0100	0001	0x01	02
PZ Adjustment 2	0101	0001	0x02	02
FT SampleThreshold 1	0110	0001	0X01	03

FT SampleThreshold 2	0111	0001	0x02	03
Val Sample Threshold 1	1000	0001	0x01	04
Val Sample Threshold 2	1001	0001	0x02	04
Watchdog Timer Thres. 1	1010	0001	0x01	05
Watchdog Timer Thres. 2	1011	0001	0x02	05
Pileup Threshold 1	1100	0001	0x01	06
Pileup Threshold 2	1101	0001	0x02	06
Bip. Crossover Thres. 1	1110	0001	0x01	07
Bip. Crossover Thres. 2	1111	0001	0X02	07
Not used (Disable) 1	xxxx	0000	0x01	08 to 0F
Not used (Disable) 2	xxxx	0000	0x02	08 to 0F
Same Values **Same Values** **Same Values**	See upper See upper See upper	0010 0100 1000	0x03 to 0x04 0x05 to 0x06 0x07 to 0x08	See upper See upper See upper
Global parameters	**GIR Control Lines to Analogue Card AMD [3..0]**	**GIR Control Lines to Analogue Card MTOE 1**	**Data Value for Channel Address**	**Data Value for Parameter Address**
Vee 24	0000	1	0x09	0x10
Vee 18	0001	1	0x09	0x11
Vee 12	0010	1	0x09	0x12
Vee 5.2	0011	1	0x09	0x13
Vee 5 Analogue	0100	1	0x09	0x14
Vee 2	0101	1	0x09	0x15
0 v	0110	1	0x09	0x16
Vcc 5 Analogue	0111	1	0x09	0x17
Vcc 5	1000	1	0x09	0x18
Vcc 12	1001	1	0x09	0x19
Vcc 18	1010	1	0x09	0x1A
Vcc 20	1011	1	0x09	0x1B
Vcc24	1100	1	0x09	0x1C
Test Generator Level	1101	1	0x09	0x1D
CFD Width	1110	1	0x09	0x1E
0 v	1111	1	0x09	0x1F
Not used (Disable)	xxxx	0	0x09	0x20 to 0xFFFF

9.3.2.5 Ge Configuration Registers (Analogue part):

VXI Base Address	***Description***	***DATA Format***
0x40	In Read Mode this is the Man. ID	D7..D0 from XCPROM
0x42		
0x44		
0x46		
0x48	Read Only: Serial no.	Read 8 bits only from XCPROM d7 to d0
0x4a	Read Only: Modification Level	Read 8 bits only from XCPROM d7 to d0

9.3.2.6 Ge DAC Buffer Control Memory Map (non volatile):

Base Addresses	**Bus Width**	**Read/ Write**	**Function**
0x60	16	r/w	Default DAC Buffer **1** values from XCProm
0x62	16	r/w	Default DAC Buffer **2** values from XCProm
0x64	16	r/w	Default DAC Buffer **3** values from XCProm
0x66	16	r/w	Default DAC Buffer **4** values from XCProm
0x68	16	r/w	Default DAC Buffer **5** values from XCProm
0x6A	16	r/w	Default DAC Buffer **6** values from XCProm
0x6C	16	r/w	Default DAC Buffer **7** values from XCProm
0x6E	16	r/w	Default DAC Buffer **8** values from XCProm
0x70	16	r/w	Default DAC Buffer **Common parameters** from XCProm

9.3.2.7 Ge DAC Buffer Setup Memory Map (volatile):

Base Addresses	**Bus Width**	**Read/ Write**	**Function**
0x80	16	write only	Change Default DAC Buffer **1** mode in XCProm
0x82	16	write only	Change Default DAC Buffer **2** mode in XCProm
0x84	16	write only	Change Default DAC Buffer **3** mode in XCProm
0x86	16	write only	Change Default DAC Buffer **4** mode in XCProm
0x88	16	write only	Change Default DAC Buffer **5** mode in XCProm
0x8A	16	write only	Change Default DAC Buffer **6** mode in XCProm
0x8C	16	write only	Change Default DAC Buffer **7** mode in XCProm
0x8E	16	write only	Change Default DAC Buffer **8** mode in XCProm

0x90	16	write only	Change Default DAC Buffer **Common parameters** mode in XCProm

9.3.2.8 G.I.R. Readout Memory Map : VME base Address : 0xA0 to 0xBE.

Base Addresses	Bus Width	Read/ Write	Function
0xA0	16	r/w	Event Counter Register
0xA2	16	r/w	Item + Group no. Register
0xA0	32	read only	Item + Group no. + Event Counter
0xA4	32	r/w	Fifo Test Enable
0xA8	16	r/w	G.I.R. Readout Control Register
0xAA	N.A.	r only w only	Start Readout Saroc in test mode End Readout Saroc in test mode
0xAC	16	r only	Readout, Temperature Status Register
0xAE	16	r/w	Valack Timeout Register (multiple of 62.5 ns) (100 <t< 4 sec.) (active when bit2 of RCR is 1) e.g. to have 100 us timeout write the value 0x640 (1600).
0xB0	32	r only	Qstat1,Qstat0 counter (16 bit each). The Qstat1 counter is to count the number of event faults difference more than one. Qstat0 counter for the number of event faults. Qstat1 value in 16 MSB, Qstat0 value is in 16 LSB
0xB4to 0xBE	N.A.	r/w	Not yet Implemented

8.3.2.8.1 G.I.R. Readout Control Register (RCR) (*not fixed*):

VME base Address : 0xA8 to be upgraded

Bit Number	Meaning when = 0	Meaning when = 1
0	Run mode for SAROC readout	Test mode for SAROC readout
1	Run mode for External readout	Test mode for External readout
2	Disable Valack Timeout Reset	Enable Valack Timeout Reset
3	Enable Readout from G.I.R.	Disable Readout from G.I.R. (card is bypass)
4	Not yet defined	Not yet defined
5	no pipelining at all (dead until VXI Readout ends)	Pipeline Readout stage (dead until data are in FIFO) (N.A.Y.)
6	Event Number Readout off	Event Number Readout on
7	Common Deadtime Readout mode (Eurogam I & II)	Euroball Readout mode
8	DSP set to Slave Mode (N.A.Y.)	DSP set to Master Mode(N.A.Y.)
9	DSP Slave is not last Slave Card(N.A.Y.)	DSP Slave is the last Slave Card(N.A.Y.)
10	Contrôle des fenêtres off(N.A.Y.)	Contrôle des fenêtres on(N.A.Y.)
11	Use Event Number Q = 00 given by 0xa2 register	Use Event Number Q (qstat1,qstat0) (see table below)
12	Not yet defined	Not yet defined
13	Not yet defined	Not yet defined
14	Not yet defined	Not yet defined
15	Not yet defined	Not yet defined

(N.A.Y.) (Not Available Yet)

8.3.2.8.1.1 G.I.R. Qstatus Table:

Qstat1:Qstat0	Meaning When Set
00	Trigger Broad cast nibble is equal to G.I.R. event counter Least Significant Nibble
01	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **more than one**
10	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **one**

9.3.2.8.2 G.I.R. Readout Status Register (*not fixed*): VME base Address : 0xAC

Bit Number	Meaning when = 0	Meaning when = 1
0	G.I.R. Temperature indicator is above the upper threshold	G.I.R. Temperature indicator is below the upper threshold
1	G.I.R. Temperature indicator is below the lower threshold	G.I.R. Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Valack Timeout deasserted	Valack Timeout asserted
8	Empty Flag of Fifo1 asserted	Empty Flag for Fifo1 deasserted
9	Full Flag of Fifo1 asserted	Full Flag for Fifo1 deasserted
10	Empty Flag of Fifo2 asserted	Empty Flag for Fifo2 deasserted
11	Full Flag of Fifo2 asserted	Full Flag for Fifo2 deasserted
12	Global Saroc_Empty asserted	Global Saroc_Empty deasserted
13	Status: No fault	Status: Event fault 0

14	Status: No fault	Status: Event fault 1
15	Status: No fault	Status: Event fault 2

Event Fault 0 = local event number fails to match broadcast event number.
Event Fault 1 = Resynchronised by exactly 1 count (latched).
Event Fault 2 = Resynchronised by more than 1 count (latched).