The EXOGAM Trigger System

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1.0 Introduction

The function of the trigger system is to identify that an interesting physics event exists and has been detected by the EXOGAM electronics. When this happens the trigger system will send control signals to the detector electronics to indicate that this event is to be coded and to the readout electronics to indicate that this event is to be stored in buffers in the VXI crates.

The EXOGAM trigger system will use a simple "common dead time" method of operation which means that once EXOGAM starts to process an event (coding and VXI crate readout), the system is dead and no further events will be accepted until the first event is either aborted or stored in the VXI crate readout buffer. The only effect that another event may have during the dead time is to cause pileup indicators to be set in the detector electronics cards.

EXOGAM electronics will be built in VXI D-sized format, in common with most modern large arrays of detectors, and so can use the same infrastructure as existing arrays (Eurogam, Euroball, INDRA, ICARE, DEMON...) which includes a standard mapping of system control lines (including trigger signals) onto the lines designated as "user defined" in the VXI specification. Because of the similarity to existing arrays it is not necessary to design a new trigger card for EXOGAM. The Euroball master trigger card will be used and a summary of its specification is included in section 6.0 of this document.

The user may trigger his experiment using either a conventional multiplicity sumbus method or externally generate a single logic pulse to be used as a trigger. It is possible to combine the two methods, requiring a certain fold and the existence of an external logic input before starting to process an event. For more complex triggering, multiple conditions may be set in either OR or AND, for example:

Trig= (FOLD•1 AND External Logic Input 1) OR (FOLD•4) OR (External Logic Input 2)

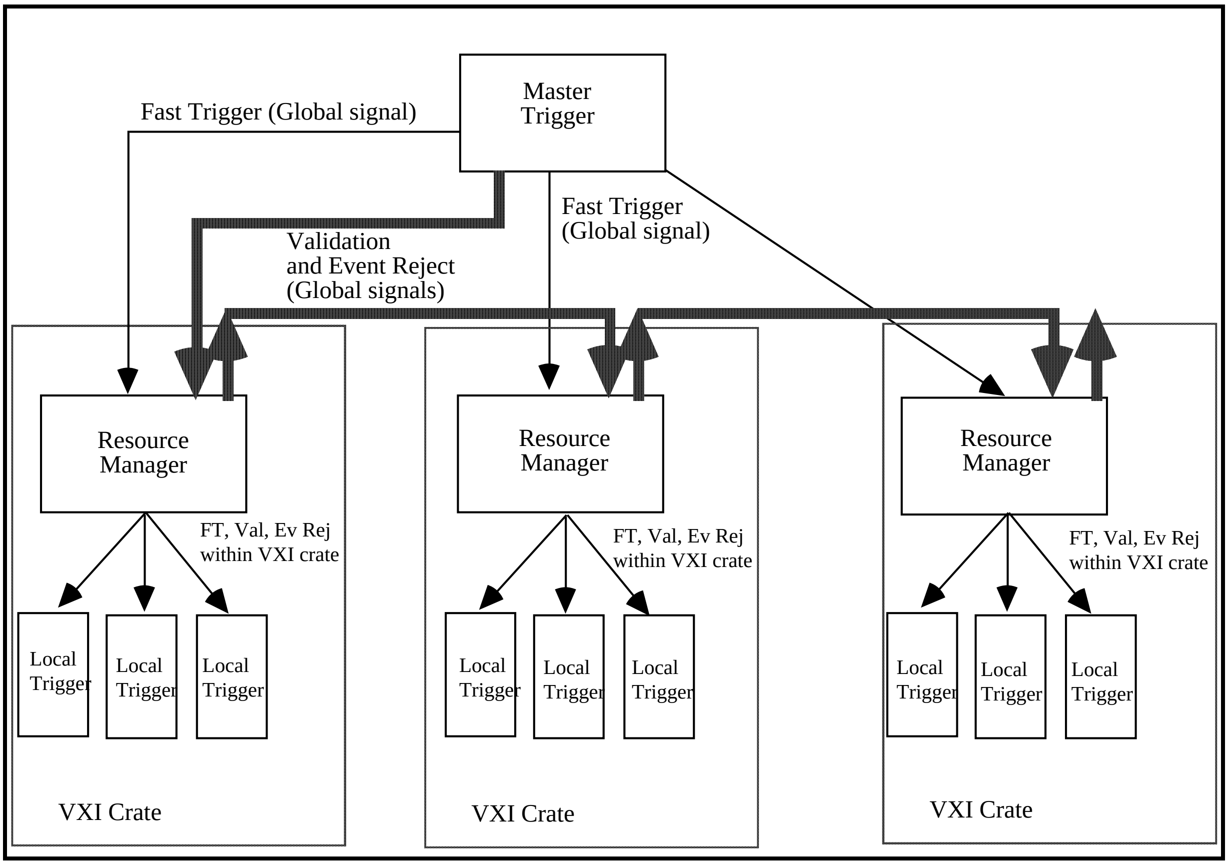
A multiplicity sumbus output is provided on the front panels of all detector electronics cards, and up to 4 such sumbuses may be used simultaneously.

The trigger system is a 2 level system, the first level being used to provide good timing for stopping TACs and a quick trigger decision, and the second level being used to either confirm that the event is good and so must be read out or else that it is bad and so to reject the event. The global trigger signals issued by the master trigger card are Fast Trigger (1st level trigger) and Validation (2nd level trigger). If there is a Fast Trigger, but no Validation (bad event) the Event Reject signal is generated instead of Validation.

2.0 General Architecture

The trigger system comprises one central master trigger card which issues global trigger signals. These signals are received and acted upon by a small piece of logic in the detector electronics which is called the “local trigger “. The job of the local trigger is to check whether the firing of a discriminator in its own detector is in coincidence with the global trigger signals and if so, to initiate coding and set a flag to say that this detector’s electronics will participate in crate readout. The local trigger also contains reset logic and a timeout to tidy up its associated electronics after each event whether it reads out successfully or not.

As shown below, the master trigger card broadcasts the Fast Trigger, Validation and Event Reject signals to each VXI crate via the Resource Managers using a Star topology for the Fast Trigger and a multi-drop ribbon cable for Validation and Event Reject. The Resource Managers in turn transmit these 3 signal to each slot in their crates. The Fast Trigger signal needs low skew and jitter because it is also used to stop TACs, so it is distributed using the matched point to point VXI STARX lines. The Validation and Event Reject signals use VXI TTLTrig lines which are bussed within a VXI crate.



2.1 The Local Trigger (LT)

The function of the local trigger (LT) is to control its own channel(s) of electronics by generating timing signals to control ADC conversion and whether or not the channel(s) participate in readout. The LT must check whether its channel has been triggered by random (background) radiation or as part of an event. It does this by sampling the Fast Trigger pulse a certain time (programmable) after its channel's discriminator fired. Later it samples the Validation pulse in the same way before transmitting its ADC data to the card readout buffer where they wait for the crate readout cycles. The LT is reset by one of the following:

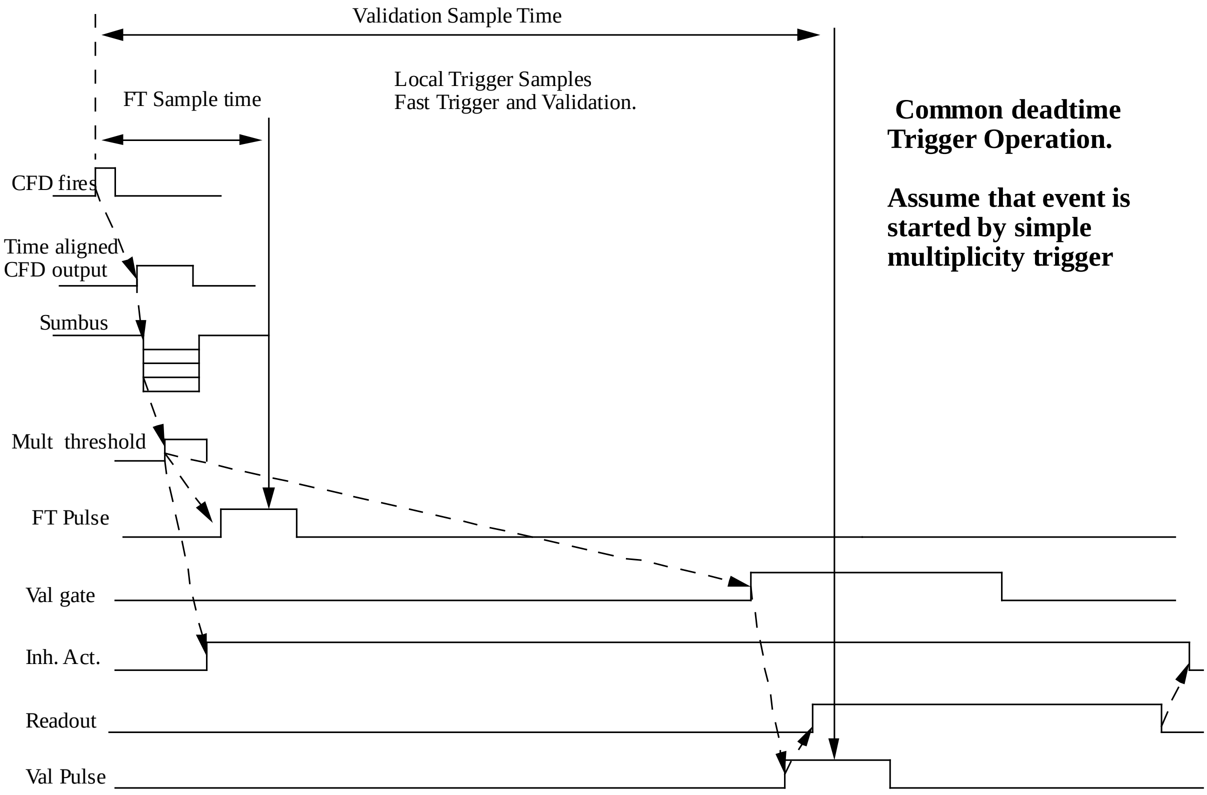
- a sample point finding no Fast Trigger/Validation,
- the Event Reject line being set, while the local trigger is active,
- by a successful data readout cycle over the VXI bus
- by a watchdog timeout (if an error occurs).

2.2 A typical event

The following diagram shows a typical event with a trigger condition set for simple multiplicity-only triggering.

The CFD in a channel fires and starts its Local Trigger timers. At the same time it enables its driver for the current sumbus. In this example several other CFDs for other detectors are in coincidence, so the threshold programmed into the master trigger card is exceeded and the event is accepted. To indicate acceptance the master trigger issues a Fast Trigger and generates an internal Validation Gate during which it checks any other (optional) user defined trigger conditions to be satisfied before issuing a Validation. The Validation indicates that the event must be read when the readout system is free to issue a readout cycle.

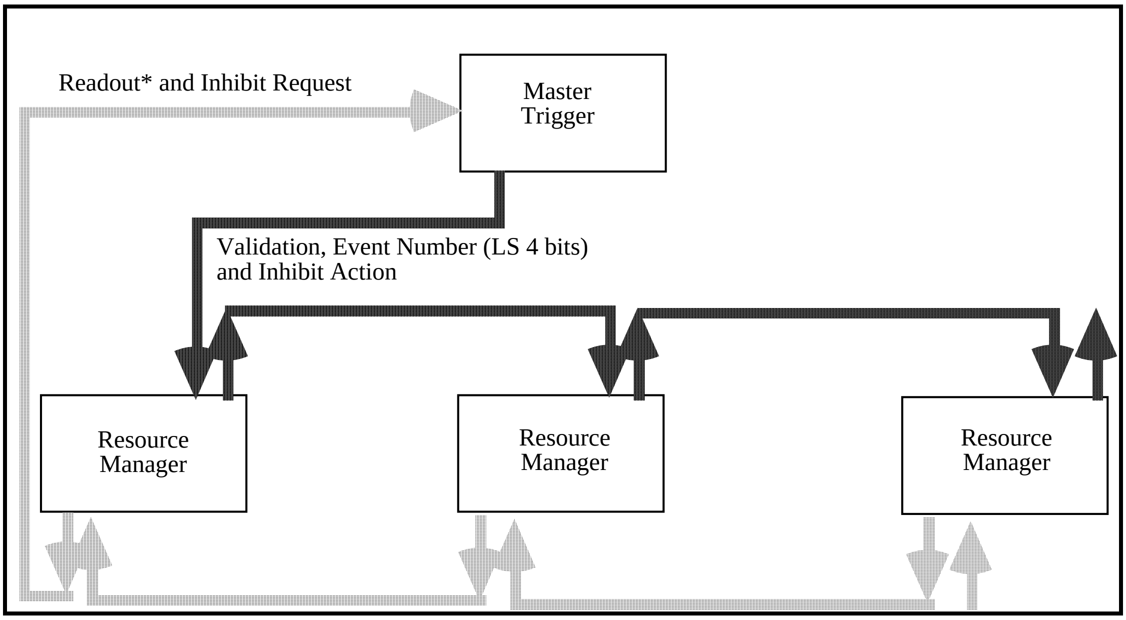
The Inhibit Action (or busy/dead time signal) is true from the start of Fast Trigger until the end of the readout cycle, and prevents the master trigger from accepting any new events while it is true. The Local Trigger sample times for both Fast Trigger and Validation are shown too.



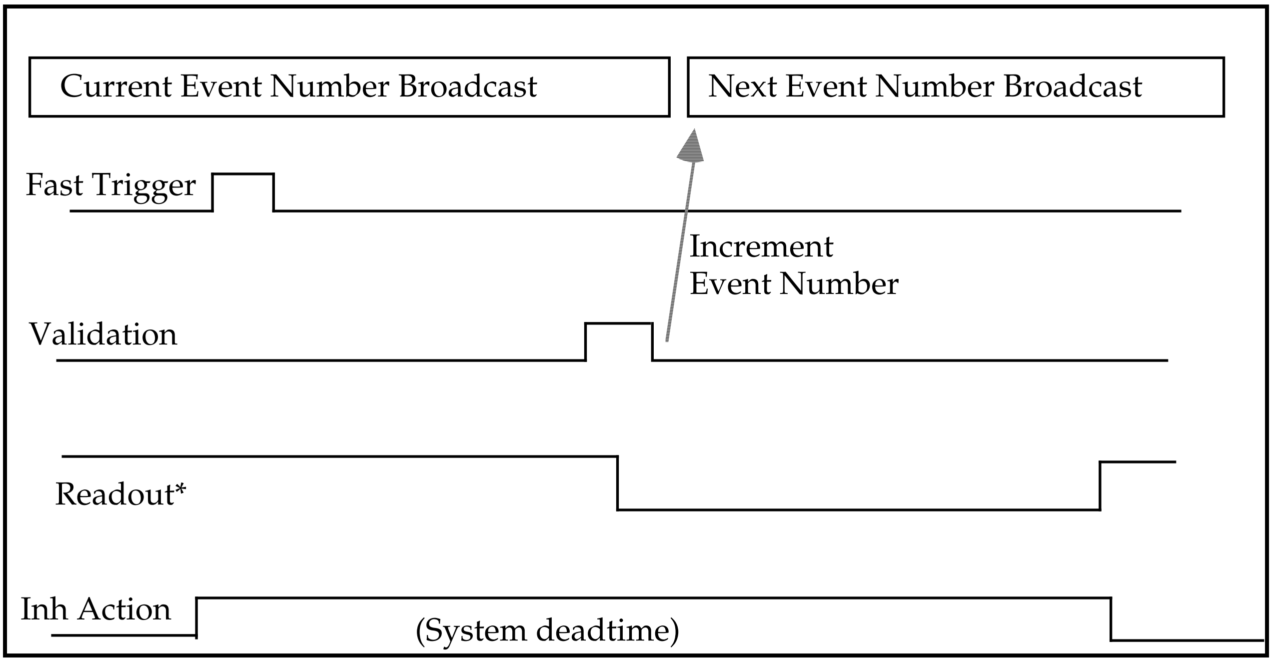
All the pulse widths and delays in this diagram are programmable, so the user can configure the system to match their own requirements. The event coincidence window is defined by the width of the fast trigger, although the width and the alignment of the CFD outputs driving the sumbus must be correctly adjusted to overlap for long enough to cross the fold threshold to generate a Fast Trigger. So, the CFD widths must be wide enough to be coincident for the worst detector timing jitter.

3.0 Interaction with the readout system.

Every time the master trigger issues a Validation (2nd level trigger pulse) the crate readout cards (STR8080/VRE) initiate a crate readout cycle. From the time that an active local trigger receives Validation until it has successfully transferred all its data into the crate readout card's buffer, a detector electronics card containing data will drive the open collector (wired OR) Readout* line on its own VXI backplane. So Readout* indicates that readout is (or will be) taking place. The Readout* signals from all VXI crates are sent back to the master trigger card by the Resource Manager cards. The master trigger card waits for all Readout* lines to be released before allowing another event.



The master trigger card generates an event number (32 bits) which is incremented at the end of every Validation (NOT by the 1st level Fast Trigger). The bottom (least significant) 4 bits of this event number are broadcast to all cards in the VXI system along with the other global trigger signals so that every card in the system can resynchronise its own local copy of the event number if necessary.



4.0 System control signals

The signals which start, stop and pause the electronics and data acquisition must be generated and controlled from only 1 place for consistent and safe system operation. This place is the trigger system.

The following signals are sent from the master trigger card to each VXI crate in addition to the validation, event reject and fast trigger signals described in earlier sections:

Stop/Go — Starts and stops data acquisition. Used in detector electronics cards to gate discriminator enable signals, so if set to stop, no discriminators can fire.

Inhibit Action — Indicates that the system is dead or paused (see Inhibit Request).

Synch Pulsers — Allows all test pulsers in detector electronics cards to be triggered at once.

Transfer Scalers — Transfers the current scaler values into a shadow register ready for readout.

The following signal is received by the master trigger card from each VXI crate in addition to the readout* signal described in earlier sections:

Inhibit Request: — Indicates that the system should be paused at the conclusion of the current event for the duration of the inhibit request signal. Used for flow control in the readout system when readout buffers are full, for pausing acquisition during detector filling and for synchronising slow ancillary detectors. Available to users for similar purposes.

5.0 Triggers for ancillary detectors.

EXOGAM has been designed to operate with ancillary detectors and so the EXOGAM trigger system provides the following inputs and outputs for ancillary detector trigger electronics:

<u>EXOGAM outputs:</u>
- Fast Trigger
- Validation
- Event Reject (for failed validations)
- Sumbus fold discriminator logic output (1)
- Sumbus analogue buffered outputs (4)

<u>EXOGAM inputs:</u>
- Current sumbus (total 4 including EXOGAM)
- Logic inputs (8, of which 4 may be stretched and delayed, programmable threshold)
- Inhibit Request (to extend dead time for slow ancillary detectors)

Ancillary detector triggers may be configured to make the ancillary device the master and EXOGAM the slave, or EXOGAM the master and the ancillary device the slave. In the first case EXOGAM generates triggers whenever the ancillary device sends it a trigger input, regardless of whether the EXOGAM detectors have fired or not, and any available data is collected. In the second case the ancillary device is triggered and its ADCs gated for readout whenever it receives a trigger signal from EXOGAM, regardless of whether there is data in the ancillary detector ADCs or not and any available data is collected. However, a hybrid of these two methods would normally be used, for example requiring both a logic signal from the ancillary detector and an EXOGAM fold of greater than or equal to one Clover before triggering either EXOGAM or the ancillary detector.

6.0 Brief Description of EXOGAM (Euroball) Master Trigger card.

The Trigger card is a D sized VXI card that examines a programmable set of its input signals using a Xilinx LCA FPGA and controls nuclear physics experiments based on those inputs.

Inputs:
4 analogue sumbus inputs connected to 4,3,2 and 1 leading edge discriminators for • fold decisions using up to 4 different folds for each sumbus. LCA sees inputs both direct from discriminators, and also after programmable time alignment circuits (delay 0-2µs, width 0-2µs).
Total 20 inputs to trigger decision FPGA.

8 Front panel logic inputs with a common programmable threshold (fast NIM, ecl, TTL, slow NIM). 4 of these inputs are also connected to time alignment circuits (delay 0-10µs, width 0-10µs) making a total of 12 inputs to the trigger decision FPGA.

1 Front panel Time Reference signal (fast NIM) (used for very accurate Fast Trigger timing).

System input signals are connected via a14 way differential ecl cable. These are Readout, Inhibit Request and Coding. Inhibit Request may also be driven via a fast NIM input.

Stop and Start inputs for the trigger's TAC are provided.

Outputs:
Fast Trigger: (12 Fast NIM Lemo 00 outputs)

System output signals are connected via a 40 way differential ecl cable. These are: Validation, Synch for Test Pulsers, Event Number (bits 0-3), VXI GO, Clear, Event Reject, Inhibit Action and Transfer Scalers to shadow registers.

Fold discriminator logic output (1) for use by ancillary detectors.

Scalers:
The Trigger card contains 8 scalers (32 bit) to count Fast Triggers, Validations, Readout cycles, Trigger Requests and a user selected signal from the trigger decision FPGA.

TAC:
A 0-2µs TAC is provided with Stop and Start software selectable to come from either the front panel or from one of the sumbus fold discriminators.

Readout and VME Interface
The VXI backplane interface for readout and control uses the Euroball standard GIR.
Data words are defined by the configurable FPGAs. For Euroball they will be some or all of the trigger type, the event number the TAC and the sumbus fold levels coded in ADCs.
For EXOGAM a 48 bit timer counterwill be added in the fpga's (rate 1MHz).

System Control
The system event number is generated in the trigger card and distributed from it during readout. The LS 4 bits are also broadcast to maintain system synchronisation.

The Fast Trigger, validation, event rejection and flow control are all generated by the trigger card and the register where the VXI GO/STOP bit is generated is also located in the trigger card.