True Singles Specification

1. REQUIREMENT:

Create True Singles histograms for each of the Clover centre contacts. True Singles is defined as all inputs for a channel to be histogrammed, regardless of any involvement in a multi-parameter event. Histogram 6MeV (ADC Range) energy spectra with a programmable number of time frames per channel.

Energy data will have 13 bit resolution with sliding scale correction for DNL. This is all that is required from the energy channel ADC which is likely to provide 15 bit resolution.

Time frames will be based on either the channel TAC or an external Time Frame Generator.

> The TAC measuring CFD -> Beam Pulse, or CFD -> Fast Trigger. The TAC output to be divided into 16 equal time frames over the range 0 to 100nS. For some decay experiments the TAC output to be divided into 16 equal time frames across the full TAC output range of 0 to 2000nS.
>
> Time Frame Generator (section 3) will control a counter in the Clover VXI card. Counter range is 1 to 64. Resolution reduction of the energy to use more than 16 frames is acceptable starting with 16 frames and 8k energy. (next 32 frames and 4k energy etc.) The range of frames is one clock of 10uS to 65000 clocks of 100mS

The Singles data can be collected whether multi-parameter is in use or not. It will be possible to disable Singles data in the VXI card.

Data will be histogrammed externally to the VXI card using a different data path to the multi-parameter data.

Max. histogram update rate: 10Khz./channel in 8 channels/VXI card. => 80 K updates/sec.

Note: Source for the above information is the ExoGam Singles meeting held at the University of Surrey on 2nd of May 1997.

2. SPECIFICATION

2.1 Overview.

The Clover VXI card (Inner contact card :HRGe8X) creates singles data for each of its eight channels, and transfers it to a VME module using a single 40Mhz. 4 bit serial data link. The VME module contains memory and links for either four or eight Clover VXI cards.

The Clover VXI card operates in different modes depending on the experimental requirements. These modes, and how they affect the True Singles operation, are detailed in the document "Constant Fraction Control Logic" by N.Karkour, and A.Richard. Available from ftp://csn-cds3.in2p3.fr/pub/elec/exogam/ccl_v01.htm

The VME module is a CES RIO 8062 PowerPC card running LynxOS. The Clover VXI card serial links connect to a mezzanine board, mounted on the VME module, containing a DSP (Digital Signal Processor), four link connections, memory, and a high speed bus (PCI) connection to the PowerPC, and VME.

The DSP is the Analog Devices ADSP21062, which includes six 40Mhz. 4 bit serial links in each chip. Input data from the links is stored in memory on the mezzanine board, translated by the DSP to histogram addresses, and transferred via the PCI bus to the PowerPC as 16k buffers. The transfer rate over the PCI bus for block transfers of this sort is 100Mbytes/sec.

To accommodate slow rate experiments all the input, and internal buffers will be flushed when no transfer to the PowerPC has occurred for 1 second. The buffers can be flushed by specific request from the experimental control software. Typically when the experiment is stopped, and started.

Memory required per channel: 8K data, 16 time frames = 512Kbytes.

2.2 Data Format

The format of the 48 bit word is split into three fields. Two are those used for multi-parameter data.

47....................32	31.......................16	15..........................0
Time frame count or all TAC ADC data	Group/Item number	6MeV Data

This format allows a trade between time frame , and analog data to be made at the DSP. The Qualifier flags that indicate a BGO veto, and pile-up may be used to select clean data only, ignored, or used to select between histograms. The number of bits allocated per channel is 17, this is made up by summing the bits allocated from the 6MeV data, time frame, and qualifier fields. The size of the available memory is the limit, currently 512Kbytes per channel.

The DSP uses the Group/Item number field to identify the channel. The user may define how many bits of data from the energy, timing, and qualifier fields to use to create the histogram. The user will make this selection using a MIDAS GUI. The selection will be implemented by the DSP.

Example:

Energy: 13 bits, starting from bit 2; Timing 4 bits, starting from bit 5. If this is the TAC data then it defines 16 frames at 8nS intervals. Assumes: TAC range is 0 to 2000nS in 8192 channels.

2.3 Spectrum Server

The Spectrum Server program running in another PowerPC in the VME crate interfaces the User to the Singles PowerPC. The histogram management operates across this interface. The Singles PowerPC is responsible for zeroing histograms, and flushing the DSP buffers.

The Spectrum Server allocates memory in the Singles PowerPC for histograms, and communicates with the Singles PowerPC using a table entry. The Spectrum Server accesses the Singles PowerPC memory directly via the VME bus.

The interface table is defined in appendix A

3. C1030 VME TIME FRAME GENERATOR.

The TFG unit contains a timer/counter module, a VME interface and an interrupt controller. The timer/counter module will divide the overall timing *period* up into *frames* as defined by the user. Up to 64 *frames* can be timed sequentially. Each *frame* can contain a maximum of 65535 counts at the *clock rate*. The *clock rate* can have a period of between 10uS to 100mS in steps of 10.

TFG controls:

Clock: 10us, 100us, 1ms, 10ms, 100ms

Number of clocks per frame: 1 to 65,535. A different number of clocks can be selected for each frame.

Number of frames per period: 1 to 64 frames

The following table of connections is extracted from the C1030 VME Time Frame Generator preliminary document from J.Thornhill Liverpool University.

Inputs	Function
Clear Edge	Rising edge at input generates a 1uS Ge CLEAR output. Resets internal counters to zero.
Clear Level	Places the same logic level as input onto the Ge CLEAR output. Resets all internal counters to zero.
Period Start	Rising edge on input starts counters (t0).
Ge Count TERM	Input used to terminate the Ge COUNT output at the end of the cable.
Ge Clear TERM	Input used to terminate the Ge COUNT output at the end of the cable.

Outputs	Function
Ge Clear	Either level (Clear Level) or pulse (Clear Edge) or by output by VME command to Clover Ge card. Sets frame to zero.
Ge Count	Pulse 1uS wide to increment (or increment enable) the frame counter on the Clover Ge card. No pulse output at end of last frame.
Veto	Generated at the end of the last time frame to indicate that the PERIOD has ended. Will remain until one of the Clear inputs is received by the module.
Period End	Generated at the end of the last time frame to indicate that the PERIOD has ended. Pulse 1uS wide.

All signals are -ve fast NIM.

4. CONNECTION DETAILS.

The cabling from the VXI card will be a 16-way ribbon cable ending in latched IDC connectors. The connection will use differential ECL drivers and receivers. The connector pin numbers are in the table below. The pin numbers are for a 16 pin IDC connector with bump polarisation.

Pin	Signal name -ve	Pin	Signal name +ve
1	Clock	2	Clock
3	Ground	4	Ground
5	Data 0	6	Data 0
7	Data 1	8	Data 1
9	Data 2	10	Data 2
11	Data 3	12	Data 3
13	Ground	14	Ground
15	Acknowledge	16	Acknowledge

The DSP module requires TTL signal levels, so a 19” rack mounted adapter will be manufactured. This will interface the Clover VXI 16-way ribbon cable to the DSP modules requirements. The adapter will provide for eight links.

Block diagram of ExoGam Singles