The EXOGAM Ge Segment Card

Contents:

1.0 Introduction

The EXOGAM segmented clover detectors comprise 4 crystals, each segmented 4 ways. The 16 outer (segmentation) contacts will each have their own preamp unlike prototypes where signals were grouped and connected to only 9 preamps. Each segmented Clover will have 4 centre contact signals which will be connected to the EGeV8 cards with full energy, time and pulse shape measurement. The 16 outer contacts will be connected to a simple VXI card measuring energy only and relying on the EGeV8 card for timing. True singles will not be provided on the outer contacts.

The Ge segment cards will work in common deadtime across all 16 channels, or across 4 groups of 4 channels (associated with each quadrant of a Clover) or in 2 groups of 6 for use with 2 Ortec PT6 detectors

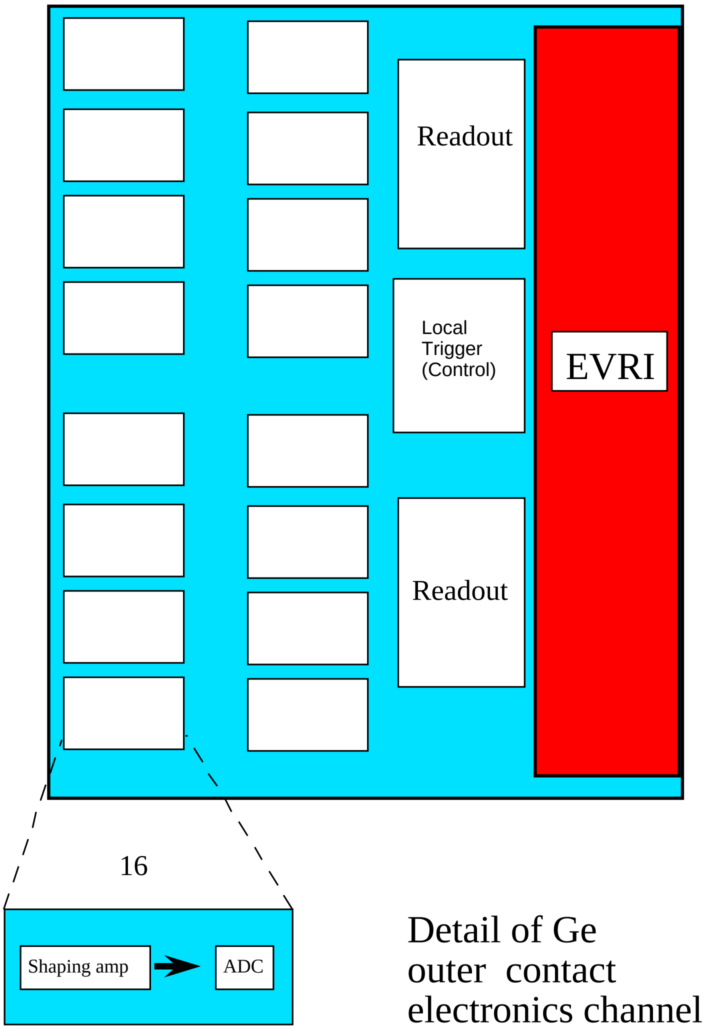
Vetos from the ESS card will be accepted and regenerative buffers will drive the Vetos from the Ge segment card to EGeV8 card. Vetos may be connected directly from the ESS card to the EGeV8 card if the Ge Outer contact card is not used or is used unsuppressed.

The Ge segment card will have no timing or positional determination electronics because the timing and position will be determined on the centre contacts. Obviously the same gamma ray detected in the same detector will have the same timing and positional information.

Random background gamma rays may interact within a clover crystal whilst it is detecting an event from the target nucleus cascade. In this case the early or late arrival of the background gamma can be marked using "early pulse" and "late pulse" qualifier flags.

2.0 General Architecture

Diagram showing possible layout of 16 channel Ge segment card and detail of a channel.



Exogam Outer contact Ge Card

3.0 Details of signal processing and adjustable parameters.

Energy Part:

The shaping amplifier will have a single 0-8 MeV range. It will be implemented by using a simplified version of the dual range amplifier designed at IPN Orsay for the EGeV8 (centre contact) Ge card. This will be either quasi-triangular or rounded top shaping with a baseline width of approximately 13 to 15us. After the shaping amplifier there will be a peak detector and stretcher.

A simple leading edge discriminator will detect when each input crosses a programmable threshold and will be used by the local trigger to detect channels which fired before (early pulse) or after (late pulse) the CFDs and are therefore not in coincidence with the real event.

Adjustment:
- PZ adjustment (10 bits)
- PDS gate
- Early/late pulse threshold adjustment (common to all inputs)

ADC

The ADC part will use either the ISN Euroball 13 bit ADC or a new 14bit ADC (based on AD976A) with sliding scale correction. One sliding scale counter could be used for the whole card since the Exogam system will work in common deadtime although if possible the new 14 bit ADC modules will have individual DACs, counters and subtractors. The ISN ADC requires an external DAC, counter and subtractor.

Energy: 0 - 8 MeV in 8k or 16k channels (1keV or 0.5keV/channel)

Adjustment:
• The sliding scale correction can be turned on and off on each channel for testing.
• The readout of each parameter has its own enable/disable.

Control

Since the system is Common Dead Time, we will use one Local Trigger (LT) for all 16 channels. The local trigger controls the mapping of the 4 CFD inputs to the control of the channels in either 1 group of 16 (where any CFD starts all channels) or 4 groups of 4 (where each CFD starts the 4 channels associated with its own quadrant) or 2 groups of 6 for Ortec PT6 detectors.

The local trigger (LT) will contain the trigger interface for sampling the validation pulse, timing circuits to control ADC conversion and the channel's participation in readout. The LT will also contain the peak detector gate for the Energy channel. The LT needs only a sample point for Validation to check for readout (this is a common deadtime system and there is no TAC on the segment signal, so there is no reason for FT sample).

The local trigger will be started by the CFD outputs from the EGeV8 card driven when any of the 4 associated CFDs fires. 4 escape suppression Veto inputs may be associated with these CFDs and may either reject or mark the data (if marking is used, then the early/late pulse marks are OR'ed together.)

The LT will detect late pulses by marking the data when the LE discriminator fires during the peak detection gate. Early pulses will be detected by looking for amplifiers which were already busy when their associated CFD input was asserted.

Zero/threshold data suppression (with one common threshold) will be used to remove the data words from ADCs which are not part of the event.

Adjustment:
- Local Trigger mode (1x16, 4x4, 2x6)
- Enable and disable for local trigger groups 1 - 4
- Enable and disable rejection based on suppression shield Vetos.
- Mark using Veto or using separate early and late pulse indications.
- Validation sample point 0-10µs in 40ns steps (common to all groups)
- Watchdog timeout 0-100µs in 400ns steps (common to all groups)

Inspection Lines:

Logic and analogue inspection lines will be connected to all important internal signals and may be switched to the VXI bus inspection lines under software control.

4.0 Inputs and Outputs

Front panel:

Inputs:

• 16 Charge preamp inputs. Each channel will have its own input from the Ge outer contacts.
Connector type: SMA
Signal Type: Analogue (200mV/MeV, 1k input impedance, Decay time constant: 50µs ±5%)

• 4 CFD inputs from EGeV8 card
Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL

• 4 Veto inputs from ESS card
Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL

Outputs:

• 4 Veto outputs to EGeV8 card
Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL

• 4 CFD outputs to ESS card
Connector type: IDC header (twisted pair ribbon cable)
Signal Type: ECL

Back panel:

The back of the card will connect to the VXI bus P1, P2 and P3 using the GIRv5 board which will handle all VME bus cycles for set-up and readout. There will be no other back panel connections.

5.0 Timescale and responsibility

The electronics design is expected to follow this schedule:

Build or modify sub-modules and mount 1 channel in NIM card for tests end 1998.
Prototype VXI card to be tested autumn 1999.
First Production cards available autumn 2000

The Ge Outer Contact card is the responsibility of the UK. Work on the card will be carried out at Daresbury Laboratory and at the University of Liverpool using GIRv5 cards supplied by CSNSM Orsay, shaping amplifiers provided by IPN Orsay and ADCs designed either at ISN(13 bits) or a new design from UK if the ISN ADCs are not available.