The EXOGAM Electronics System Architecture

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1.0 Introduction

The EXOGAM array comprises a number of multi-element segmented Ge detectors. The current plans are for up to 16 segmented Clover detectors, each equipped with an escape suppression shield. There are many similarities between EXOGAM electronics and that used for large gamma ray arrays like Eurogam and Euroball. The EXOGAM electronics will capitalise on our experience from these systems and will continue to use miniaturised sub-modules housed in cards built in VXI D-sized format.

The Euroball readout and triggering systems are both suitable for EXOGAM, so these can be used without further development. The Euroball infrastructure (crates, resource managers and crate readout cards) can be used in EXOGAM. Although it is not planned to re-use Euroball equipment (which will be in use elsewhere), it is beneficial to use equipment well known to the engineers designing and maintaining the electronics for EXOGAM. Logic and analogue inspection lines will again be provided from all modules (accessible via the resource manager front panels) for visualisation of internal signals from the modules. Some component designs from Eurogam and Euroball can be re-used with small enhancements or modifications in the new VXI modules.

There are some important differences between Euroball and EXOGAM electronics: the detectors are different, there will be a high level of background radioactivity to be removed from the spectra, and with an array comprising entirely multi-element detectors, the use of add back becomes more important and therefore low energy resolution is highly significant.

The VXI modules in the EXOGAM system will be:

- Segmented Clover Ge Inner Contact electronics (2 clovers per card)
- Segmented Clover Ge Outer Contact electronics (1 clover per card)
- Segmented Clover escape suppression shield electronics (6 shields per card)
- Master Trigger card (1 card)
- Resource Managers, type STR8032 (1 per crate)
- Crate readout cards, type STR8080 (1 per crate)

The following modules will be added for use with ancillary detectors:

- 2x 64 channel ADC cards (GANIL peak sensing voltage converters)

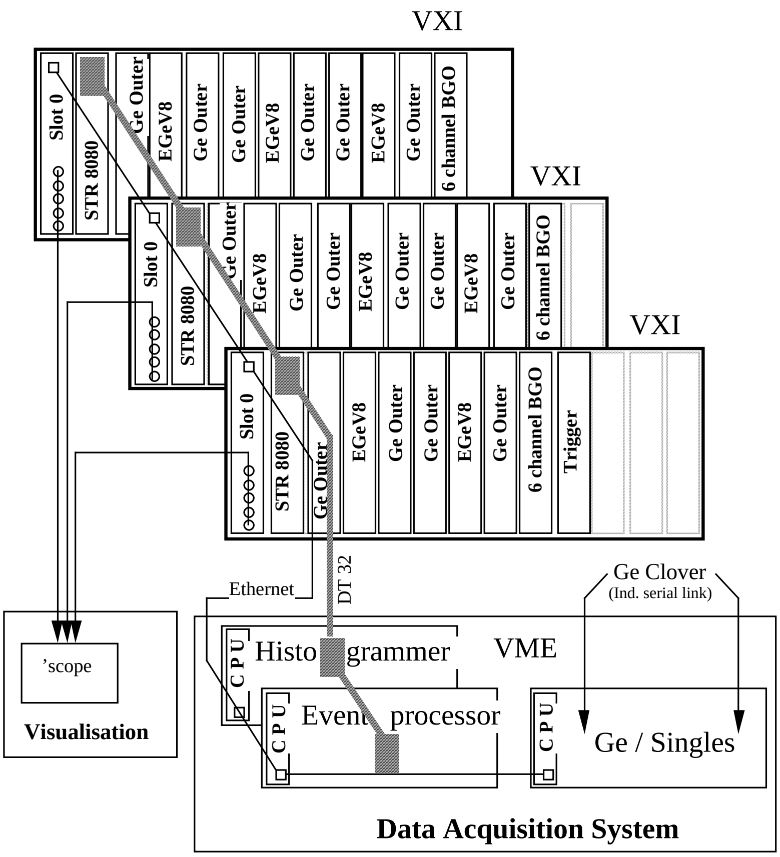
The basic system will comprise 8 Clover Inner contact Ge cards, 16 Clover Outer contact Ge cards, 3 Clover shield cards, 1 Master Trigger card and so will fit in 3 VXI crates and still leave space for ancillary detector cards to be added. The 3 crates will require a total of 3 Resource managers, and 3 Crate readout cards.

Singles histograms which record every Clover Ge ADC conversion without any trigger dead time losses are required for some EXOGAM experiments. A method of histogramming such “true singles” will be provided. The true singles system will generate 2-d spectra with energy (13 bits) and timing (4 bits) where the timing may be connected either to a TAC measuring CFD-beam pulse (for background rejection) or to an external time frame generator (for beta decay experiments).

2.0 General Architecture

The following diagram[1] shows an overview of the architecture of EXOGAM electronics.

Each crate has spare slots for additional electronics for ancillary detectors.



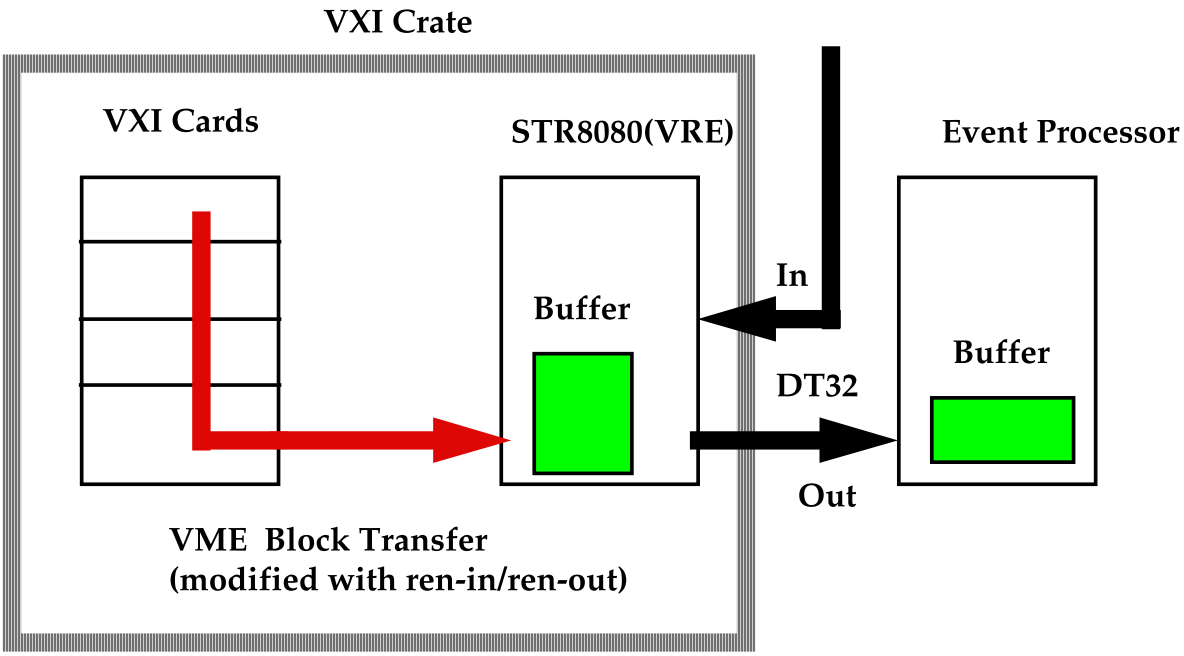
EXOGAM System Diagram

Drawn by Pouthas and Lazarus
Last update 20-3-98

[1] This diagram was originally drawn by Joel Pouthas for the “Livre Blanche” and has been updated since then by Ian Lazarus to include changes as the system has been refined and improved..

3.0 Readout system.

The following diagram shows the schematic flow of EXOGAM readout. The data are transferred over the VXI backplane into a buffer in the STR8080 crate readout controller. At the end of this cycle the crate is ready for a new event, and when all VXI crates have finished their readout cycles for the current event, the system permits a new event. Thus DT32 bus readout from VXI into the VME event collectors is decoupled from the VXI backplane readout by the STR8080's buffer and cannot block VXI readout except by failing to empty the buffer fast enough. In this case a flow control mechanism will prevent the generation of new triggers until there is space in the STR8080 buffer again by driving Inhibit Request.



Every time the master trigger issues a Validation (2nd level trigger pulse) the crate readout cards (STR8080/VRE) initiate a crate readout cycle. The open collector (wired OR) Readout* line on the VXI backplanes indicates that readout is (or will be) taking place and is driven by all VXI data source cards from Validation until they have transferred their data on the bus.

The VXI backplane readout cycle is like a VME block transfer in the DTACK*/DS* handshakes, but has been modified to allow multiple slaves to respond in sequence to the same cycle by means of a FERA-like REN-IN, REN-OUT chain running down all the modules in the crate to pass a readout token from slave to slave. The slave with the token is the one that responds to the DS* and each slave transfers all available data until its FIFO is empty. Then it stops driving the Readout* line, and passes the readout token to the next card by driving its REN-OUT signal into the next cards REN-IN input.

Readout from the STR8080 to the event collector uses the DT32 bus, developed for Eurogam, used in Euroball and now supported as one of the output module options in the Struck STR8080. The DT32 bus is very similar to FERA except that it is 32 bits wide. The data are transferred synchronously using the WST pulses as strobes. The signals are all differential ECL, carried over ribbon cables.

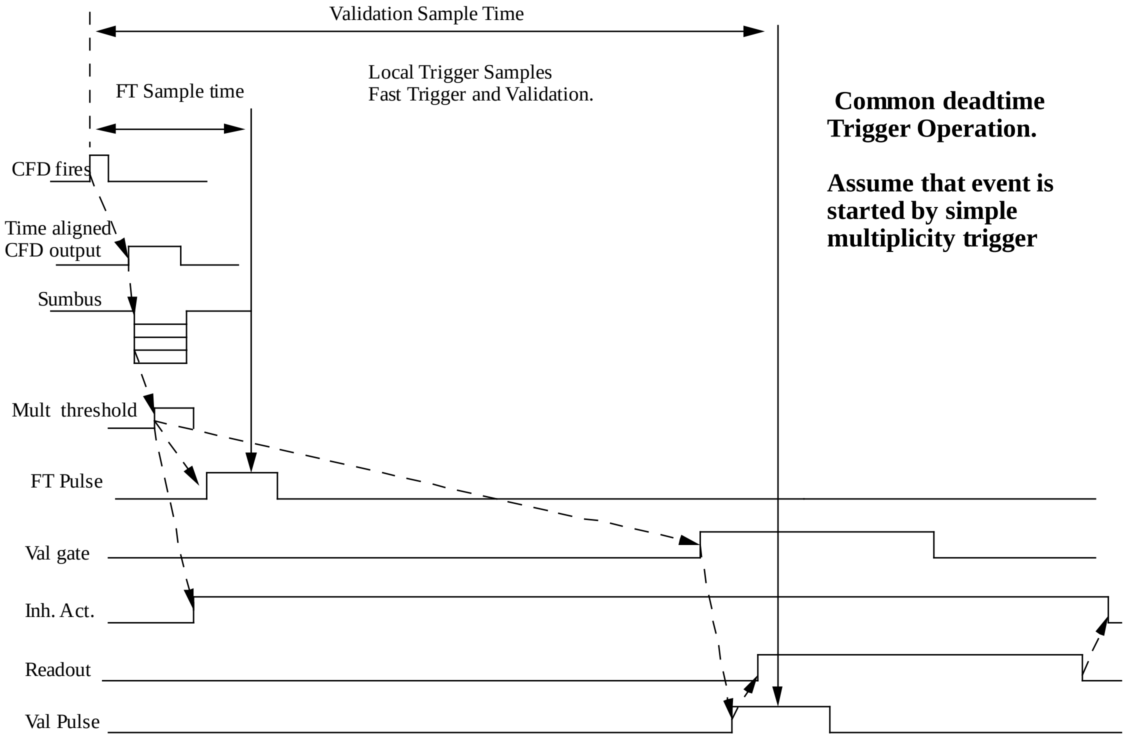
Full details of VXI backplane readout can be found in EDOC076 and full details of DT32 readout are in EDOC075 from the Eurogam document server. Details of hardware event format and tokens will be described elsewhere in the data acquisition documentation.

4.0 Trigger system

The EXOGAM trigger system will use a simple “common dead time” method of operation which means that once EXOGAM starts to process an event the system is dead and no further events will be accepted until the first event is either aborted or stored in the VXI readout buffers. The only effect that another event may have during the dead time is to cause pileup indicators to be set in the detector electronics cards.

The user may trigger his experiment using a conventional multiplicity sumbus or may provide a single logic pulse to be used as a trigger. It is possible to combine the two methods for more complex triggers, requiring a certain fold and the existence of an external logic input before starting to process an event. Multiple (parallel) trigger conditions may be used.

The trigger system is a 2 level system, the first level being used to provide good timing for stopping TACs and a quick trigger decision within 2μs. The second level is used between 2 and 10μs to either confirm that the event is good, and so must be read out, or else that it is bad and so must be rejected. The global trigger signals issued by the master trigger card are Fast Trigger (1st level trigger) and then Validation (2nd level trigger). The global signals are distributed to every module where they are used by Local Triggers to check whether or not its channel is active in coincidence with enough other channels to have caused an event. The Local Trigger controls ADC coding and readout for its channel or module. The Event Reject signal may be asserted by the Master Trigger at any time during the event to abort the current event and resets all Local Triggers.



Common deadtime Trigger Operation.

Assume that event is started by simple multiplicity trigger

In the diagram above, the CFD in a channel fires and starts its Local Trigger timers. At the same time it enables its driver for the current sumbus. Other CFDs from other detectors are in coincidence so the threshold programmed into the master trigger card is exceeded and the event is accepted. To indicate acceptance the master trigger issues a Fast Trigger and generates an internal Validation Gate during which it checks any other (optional) user defined trigger conditions to be satisfied before issuing a Validation. The Validation indicates that the event must be read by the crate readout. Meanwhile, the local trigger must check whether its channel has been triggered by random (background) radiation or as part of an event. It does this by sampling the Fast Trigger and Validation pulses at certain times (programmable) after its channel's discriminator fired. A fuller description of the trigger system is available as a separate EXOGAM specification, edoc415, and a brief specification of the VXI trigger is given in section 9.

5.0 Ancillary Detectors.

EXOGAM has been designed to operate with ancillary detectors. There will be 3 possible methods for connecting ancillary detectors.

The first is that users bring their own custom built EXOGAM-compatible VXI cards and crate with interfacing of readout via DT32 and triggering as described in section 4. This is the most "seamless" route in to the EXOGAM system for those who have the resources to use it.

The second method is for users who don't have (or can't bring) their own ADCs. EXOGAM and GANIL will provide 128 channels of VXI peak sensing voltage ADC cards in 2 VXI cards to which users can connect their ancillary detector signals. Each input has its own independent gate although the duration of the gates is the same for all ADCs. These modules are described more fully in another part of the specification documents. 3 variants (charge, voltage and time) of this VXI card exist: requests for more channels or for charge/time versions should be made via the Ancillary Detector group (convenor John Durell)

The third method is for the users who already have a system with FERA ADCs. A module called an FVI (FERA-VXI Interface) designed by CENBG, Bordeaux could be available to interface FERA chains into the VXI readout if there is sufficient user demand *(send comments to Ancillary Detector group convenor*, John Durell*)*. Each FVI handles 2 FERA chains. Note that GANIL discourages the use of FERA, so users must provide their own FERA support.

To facilitate the connection of ancillary detectors and to help synchronise them, the EXOGAM system makes available certain outputs and accepts certain inputs:

EXOGAM outputs:
- Fast Trigger
- Validation
- Event Reject (for aborted events)
- Sumbus fold discriminator logic output (1)
- Sumbus analogue buffered outputs (4)
- Event number (least significant 4 bits)
- Stop/Go
- Inhibit Action (System busy or paused by Inhibit Request)

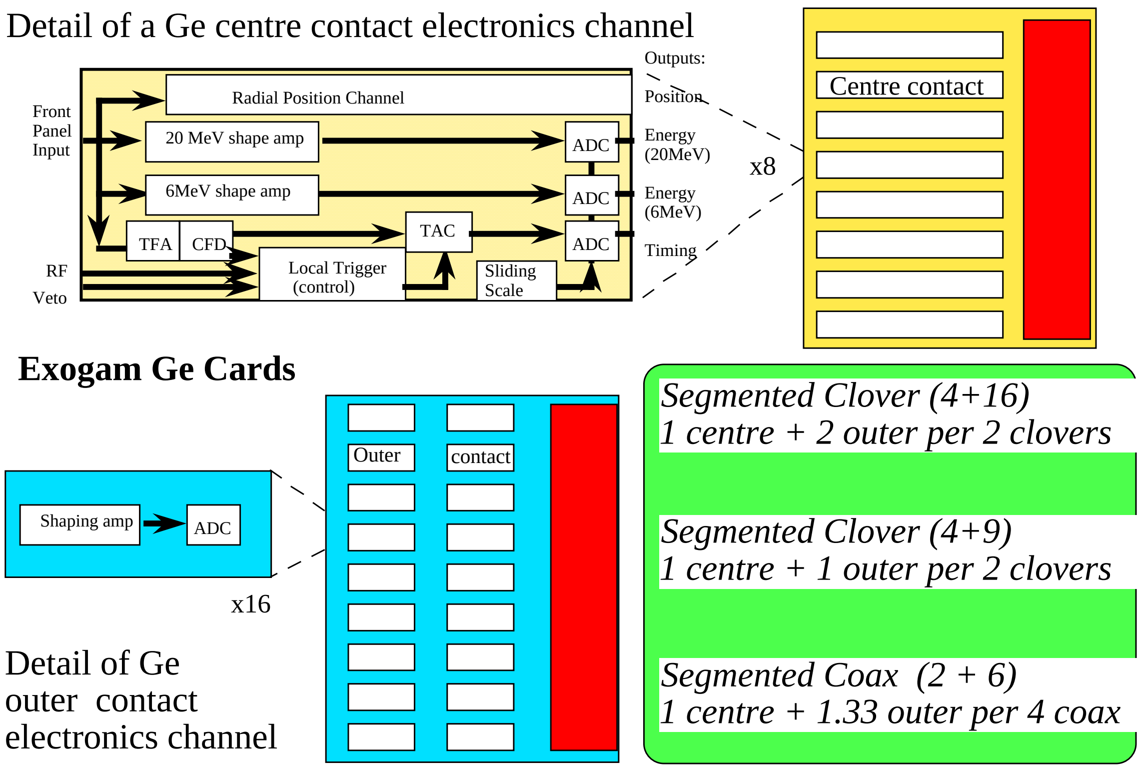
EXOGAM inputs:
- Current sumbus (total 4 including EXOGAM)
- Logic inputs (8, of which 4 may be stretched and delayed, programmable threshold)
- Inhibit Request (to extend dead time for slow ancillary detectors)

6.0 Ge Electronics

EXOGAM Ge cards must instrument both segmented clover and segmented coaxial detectors, and, ideally, be compatible with Miniball's segmented cluster detectors too.

The segmented clover detectors comprise 4 crystals, each segmented 4 ways, so the segmented clovers require electronics for 4 inner (centre) contacts and 16 outer contacts. The segmented coax detectors have 2 centre contacts from the single longitudinally segmented electrode; the outer electrode is segmented 6 ways. So coaxial segmented detectors require electronics for 2 inner contacts and 6 outer contacts. The Miniball segmented cluster detectors have one centre contact and an outer contact segmented 6 ways.

The Exogam Ge electronics will comprise 2 card types: the HRGE8X card will be fully instrumented for 8 centre contacts and the Ge segment (outer contact) card will be instrumented more simply for 16 outer contacts. The Miniball requirement for full instrumentation on the 6 outer contacts as well as the single inner contact can be met by the HRGE8X card.



Each channel in the HRGE8X will have electronics to measure energy, timing and radial hit position. The energy will be measured in 2 ranges from 0-6MeV or from 0-20MeV with 14 bits (16k) ADCs. The 20MeV range could (if requested by users) be switchable to become a 3MeV range. The 6MeV range will not be switchable. Online gain and offset adjustment of ±5% will be provided in the 6MeV energy range only. The timing will measure from the time the CFD fires to either the next beam timing (RF) pulse or to the time of the Fast Trigger (first level trigger, also acting as a global timing reference). Hit localisation information is available by a combination of the radial hit position determination and the intrinsic segmentation of the detector. The radius of the main interaction is determined by analysis of a current pulse obtained by differentiating the charge pulse from the preamps (or a current pulse directly from the preamps). The pulse shape analysis will use digital processing in a DSP to analyse samples from a 65MHz, 12bit flash ADC to find the greatest slope of the current pulse (or other algorithms developed later).

The HRGE8X Ge cards will connect to the VXI bus via an interface module called the EVRI (**E**xogam **V**xi **R**eadout and **I**nterface card) which is a development of the Euroball GIRs.

The Ge segment electronics will comprise 16 channels measuring energy only, and will connect to the VXI bus via an updated GIR (v5) which is simpler electrically and more rigid mechanically than the Euroball GIRs. The Ge segment VXI card will behave as a slave to the HRGE8X, using the CFD signals from the associated HRGE8X card to trigger operation of the local triggers which will provide the control for peak detection and readout. "Late pulse" detection will be provided to mark those channels which have received a new input pulse during the peak detection gate. This is analogous to post pulse pileup except that it is marked regardless of whether the channel was processing a pulse when the late input arrives. Similarly, early pulses (channels that are already busy when the peak detector gate starts) will be marked.

More information about the Ge cards can be found on the IPN WWW site (HRGe8x) and in edoc407 (Ge segment card)

7.0 Escape Suppression shield electronics

The EXOGAM segmented Clover Ge detectors will all use escape suppression shields made of Bismuth Germanate (BGO) at the sides and Caesium Iodide (CsI) as back-catchers. The number of BGO crystals in the shield will vary depending on whether EXOGAM is operating in its close packed mode or its normal mode, but the phototubes will be ganged together to give a total of 4 outputs from the side pieces and another 4 from the back catcher in both cases. All that will change is that extra phototubes will be added to the daisy chain when the extra side pieces of BGO are added.

The HV will be daisy chained between phototubes with a small potentiometer provided on each base for gain matching. It will not be possible to individually switch HV on/off to gain match or test individual phototubes via this VXI card.

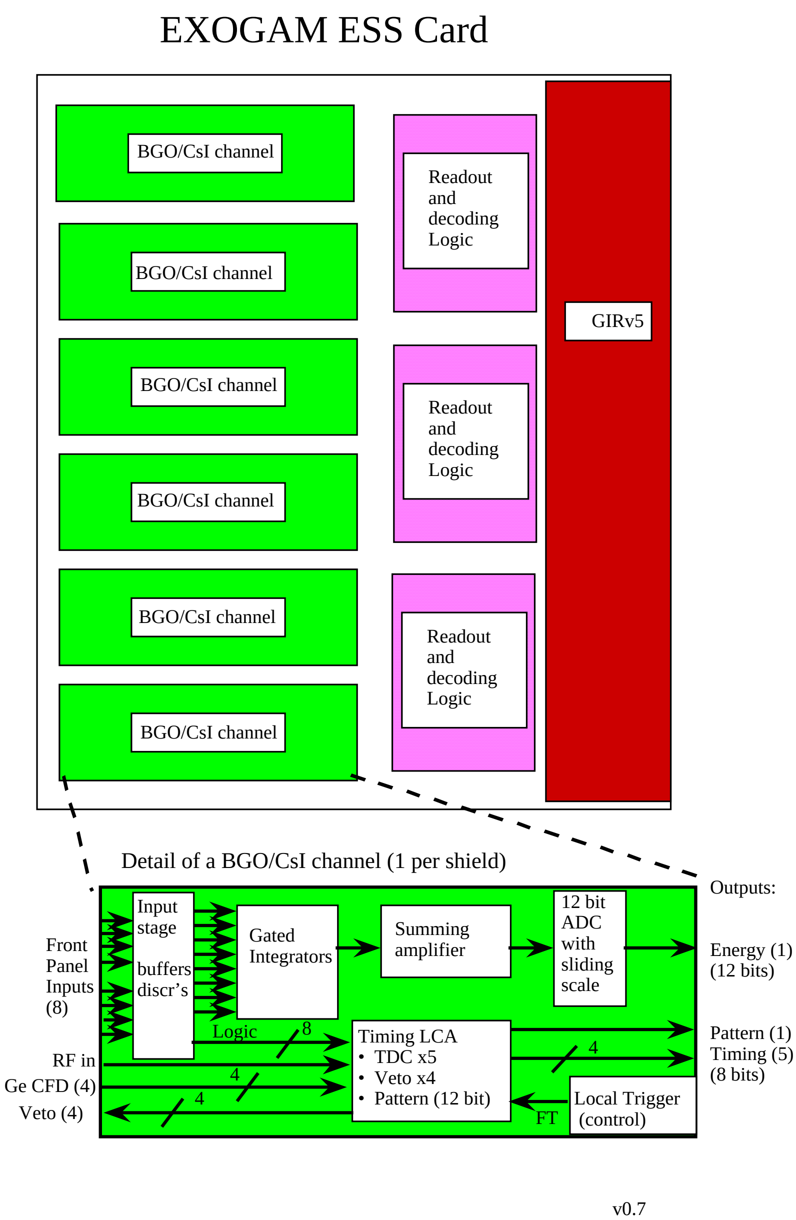
The 8 signals from a shield will be handled by a single channel of electronics which will measure the sum energy of all 8 inputs and the timing of either each quarter of the shield or the whole shield measured against its respective Ge CFD. The user may also select by, computer control, whether the shield timing and Veto are generated from BGO only, CsI only or both BGO and CsI. In addition to energy and timing, a 12 bit hit pattern will be generated from each shield and its associated Clover Ge using a programmable coincidence window (0-1200ns) started by the first of all Ge, BGO and CsI inputs to fire.

Four Vetos will be provided from each shield (one per Ge crystal) for the associated Ge cards. The user may select whether each Veto is generated from all the shield elements (i.e. all 4 are the same) or generated individually from just the quarter nearest its Ge crystal. The user may also select whether the Veto is derived from the side pieces alone, the back catcher alone or from the back catcher and side pieces taken together. The width of each veto will be adjustable for optimum suppression.

The ESS card is designed primarily to enhance the Ge peak-total, hence the name, Escape Suppression Shield (ESS) card, so the card's prime purpose is providing good Veto information. The ESS card will also measure the shield's sum energy in the range 0-20MeV.

The signals from the phototubes to the ESS card will be driven from buffers in the HV distribution box mounted close to the shield. The signals will be amplified and driven by line drivers, in the preamplifiers, along cables to the ESS card. There will be no shaping in the preamplifiers to reduce the signal delays and therefore give the best timing. All signal shaping will take place within the ESS card.

Each ESS card will instrument 6 complete escape suppression. It will connect to the VXI bus via an updated GIR (v5) which is simpler electrically and more rigid mechanically than the Euroball GIRs. A front panel current sumbus will be provided (4mA per shield) to indicate how many shields have fired.



More information about the ESS card can be found in edoc406.

8.0 Singles Histogramming

The singles histogramming system was designed according to the following specification:

Each Clover Ge channel (there are 4 such channels for each Clover) will have its own histogram comprising:

- 13 bits of sliding scale corrected energy
- 4 bit “timeslice” which is software selectable to cover either 0-100ns (CFD-RF) or 0-1000/2000ns (full scale) (CFD-FT)
- Instead of the timeslice, a 64 channel (6 bit) time frame may be used for slow decay experiments. The time frame is externally clocked in range: 1x10µs to 64k x 100ms (> 1 hour). Where 32 or 64 time frames are used, the energy resolution will be reduced by 1 or 2 bits respectively.

So the total memory required for each Clover is 2**(4+13) x 4 longwords = 2 Mbytes

The system will be designed to cope with the following rates:

- Up to 10kHz per crystal (i.e. 40kHz per Clover detector)
- 40kHz x (13+4) bits + control = approx. 1 MHz serial readout per card.

No add-back will be used in singles because the complexity does not justify the improvement in resolution. A switchable BGO veto will be provided to allow optional histogramming of only clean data without scatters into the escape suppression shield.

The system will use a dedicated readout path and the current proposal is that this will use dedicated links from each Clover card's EVRI (via the Ge card's front panel) to a commercial SHARC DSP (Digital Signal Processor) mounted on a module in a VME crate. The SHARC family of DSP devices is also used in the EVRI, so the DSP's own high speed serial link can be used to transfer the data. The SHARC module will be installed on a commercial VME PowerPC card, and will connect to four Clover Ge cards. The PowerPC will share the histogramming memory with the SHARC, and will run the LynxOS operating system. The Spectrum Server will run in the LynxOS environment. The Time Frame Generator will also be located in this VME crate.

More information about the singles system can be found in edoc414.

9.0 VXI Trigger Card Specification

The Trigger card is a D sized VXI card that examines a programmable set of its input signals using a Xilinx LCA FPGA and controls nuclear physics experiments based on those inputs.

Inputs:
4 analogue sumbus inputs connected to 4,3,2 and 1 leading edge discriminators for • fold decisions using up to 4 different folds for each sumbus. LCA sees inputs both direct from discriminators, and also after programmable time alignment circuits (delay 0-2µs, width 0-2µs).
Total 20 inputs to trigger decision FPGA.

8 Front panel logic inputs with a common programmable threshold (fast NIM, ecl, TTL, slow NIM). 4 of these inputs are also connected to time alignment circuits (delay 0-12µs, width 0-12µs) making a total of 12 inputs to the trigger decision FPGA.

1 Front panel Time Reference signal (fast NIM) (used for very accurate Fast Trigger timing).

System input signals are connected via a 14 way differential ecl cable. These are Readout, Inhibit Request and Coding. Inhibit Request may also be driven via a fast NIM input.

Stop and Start inputs for the trigger's TAC are provided.

Outputs:
Fast Trigger: (12 Fast NIM Lemo 00 outputs)

System output signals are connected via a 40 way differential ecl cable. These are: Validation, Synch for Test Pulsers, Event Number (bits 0-3), VXI GO, Clear, Event Reject, Inhibit Action and Transfer Scalers to shadow registers.

Fold discriminator logic output (1) for use by ancillary detectors.

Scalers:
The Trigger card contains 8 scalers (32 bit) to count Fast Triggers, Validations, Readout cycles, Trigger Requests and a user selected signal from the trigger decision FPGA.

TAC:
A 0-2µs TAC is provided with Stop and Start software selectable to come from either the front panel or from one of the sumbus fold discriminators.

Readout and VME Interface
The VXI backplane interface for readout and control uses the Euroball standard GIR.
The following data words are individually enabled for readout: trigger type, the event number (2x16 bit words), the TAC and the four sumbus fold levels coded in ADCs. A new 48 bit timer, counting at 1MHz, has been implemented for EXOGAM and will be optionally readable in event data as 3 words of 16 bits, staticised when the Fast Trigger pulse is produced.

System Control
The system event number is generated in the trigger card and distributed from it during readout. The LS 4 bits are also broadcast to maintain system synchronisation. The Fast Trigger, validation, event rejection and flow control are all generated by the trigger card and the register where the VXI GO/STOP bit is generated is also located in the trigger card.