# Euroball Trigger User Guide

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## 1 Introduction

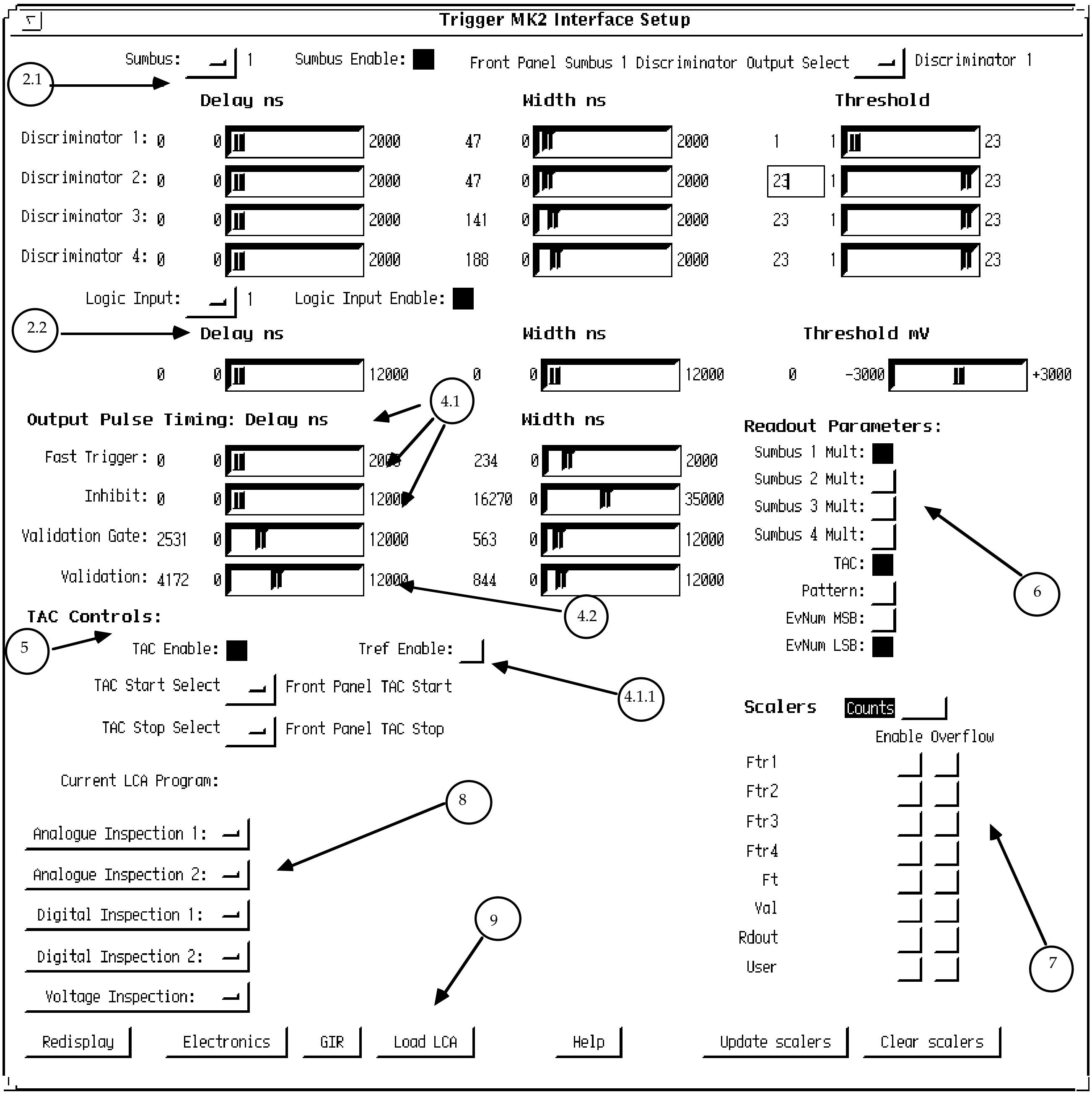
The main function of the trigger card is to generate the 2 global trigger signals known as Fast Trigger (FT) and Validation (Val). The details of the Euroball Trigger system are described in *"An Introduction to the Euroball Electronics"* with which the user is assumed to be familiar.

Associated with the Val pulse is a 32 bit event number which is incremented at the end of every Val pulse. The bottom 4 bits of this event number are used by the rest of the system as a synchronisation reference. The event number may be read from the trigger card in the event by event data.

The decision as to whether or not to generate FT and Val pulses is made by a reconfigurable logic cell array (LCA) implemented in a Xilinx 4013 LCA. This LCA is known as the FTV_LCA. The inputs to the FTV_LCA are a mixture of system signals and physics signals. The system signals indicate whether or not the system is already busy (dead) and whether the system is in the Stop state or the Go state. If the system is not dead and is in the Go state then the physics inputs are compared against the programmed criteria for FT and Val generation. The physics inputs come from 4 sumbuses (for fold selection) and 8 logic inputs (for signals from ancillary detectors or beam state indicators).

The FTV_LCA initially loads a default program from its PROM which will handle most experiments. For unusual experimental trigger conditions the FTV_LCA can be reconfigured by downloading a new configuration file from a library in the Euroball MIDAS control software.

The remainder of this document describes how to control the Euroball Trigger card from the MIDAS control window called "Trigger MK2" which is shown on the following page. Arrows on the diagram show the section number in this document which describes the electronics controlled by the indicated part of the control screen.




## 2 Physics Inputs for FT and Val decisions

The MIDAS control window for the Trigger card controls all the physics inputs from which FT and Val generation is controlled.

### 2.1 Sumbus inputs

The 4 sumbus inputs allow selection based on fold. The 4 sumbus inputs are electrically identical. The inputs should be connected to current sources representing fold and where the total current doesn't exceed 80mA. In Euroball and Eurogam a level of 4mA per hit is generated by Cluster Ge cards and other Ge electronics giving a maximum fold of 20. The MIDAS threshold calibration assumes these input levels when it maps the fold selection to a real DAC output so other levels will require special calibration.

Conventionally sumbus 1 is connected to RawGe multiplicity, sumbus 2 to clean Ge multiplicity leaving sumbus 3 and sumbus 4 available for signals from ancillary detectors (or as spares in case of problems with sumbus 1 and 2). The sumbuses are electrically identical and differ only in the number of simultaneous threshold checks which may be performed.

Each sumbus is connected to a number of leading edge discriminators which are compared against the DAC output level(s) set by the user's fold selection(s). The discriminator outputs are connected directly to the trigger logic FTV_LCA and also to non-retriggerable Gate and Delay modules. The Gate and Delay outputs are also connected to the trigger logic FTV_LCA, permitting the use of delayed or stretched pulses where coincidence with external devices or signals is required as a trigger condition.

The sumbus inputs are controlled from the part of the MIDAS window at the top, under the "sumbus" pull down menu button. Use the pull down menu to select one of the 4 sumbuses and then the 12 sliders below will control the selected sumbus. The MIDAS software shows the user only one sumbus at a time. The user can control the following:

1) Sumbus enable/disable for the current sumbus
2) Fold selection threshold (≥n) by using the threshold slider
3) Delay and Width of Gate and Delay output using the appropriate sliders.

Note that sumbus 1 has four different discriminators allowing up to 4 different fold selections to be used simultaneously with various other inputs when making complex FT selections (see example in 2.3). Each discriminator has an associated Gate and Delay module.

Sumbus 2 has 3 discriminators, sumbus 3 has 2 discriminators and sumbus 4 has only 1 discriminator. Unused sliders for sumbus 2, 3 and 4 are inactive and "greyed out" on the screen although still displayed.

Each sumbus produces a buffered voltage signal at the trigger's front panel proportional to the current on the sumbus.

Sumbus 1 has an additional feature where a fast NIM pulse is available on the front panel connected to the output of one of the four discriminators. This output is always enabled, and a pull down menu at top of the MIDAS control screen selects which of the four discriminators is connected.

**2.2 Logic inputs**

The logic inputs are controlled from the part of the MIDAS window immediately below the "Logic Input" pull down menu button. One enable button is used to enable or disable all 8 logic inputs (ticked = enabled). Use the pull down menu to select one of the 8 logic inputs and then the 3 sliders below will control the selected input.

Each of the 8 front panel logic inputs is connected to its own leading edge discriminator with its own programmable threshold with a range +2volts to -3v. This is adjusted using the slider called "threshold".

Inputs 1 to 4 have a gate and delay generator after the discriminator for time alignment. The delay and width are controlled from the appropriate sliders.

Unused sliders for delay and width of inputs 5-8 are inactive and “greyed out” (although still displayed). Only the threshold may be adjusted for inputs 5-8.

**2.3 Example of a complex Fast Trigger Condition**
In most experiments the simple default program described in 4.0 will be sufficient, but to demonstrate the power of the trigger system here is a more complex example.

In this example we look for 8 trigger conditions simultaneously, based on the folds detected on sumbus 1, sumbus 2 and sumbus 4 and pulses from 7 different logic inputs. The input from logic input 5 causes a trigger on its own regardless of other inputs. All other 7 possible trigger conditions are accepted only if the additional condition is fulfilled that the fold seen on sumbus 3 is within a specified range (2 to 9).

```
FT  =   (SB3Fold≥2  AND  NOT_SB3Fold≥10)
        AND
        (
                (SB1Fold ≥5)
        OR      (SB1Fold≥3 AND LogicInput 1)
        OR      (SB1Fold ≥2 AND LogicInput 2)
        OR      (SB1Fold≥1 AND LogicInput 3 AND NOT_LogicInput 4)
        OR      (LogicInput 6)
        OR      (SB1Fold≥3  AND  SB2Fold≥2)
        OR      (SB4Fold≥7 AND LogicInput 7)
        )
    OR
        (LogicInput 5)
```

Each of the 8 lines may be allocated a different bit in the Trigger Type field, so that they can be differentiated at the time of the validation for 8 different validation checks.

There is no real limit to the number of OR terms or AND terms which can be specified although practically the set-up and time alignment will be the limiting factor, and only 8 different trigger type bits exist without coding and decoding the 8 bit trigger type field.

The FT that results from these conditions must arrive at the Ge and BGO channels at approximately the same time whichever condition generates it. In this way the FT sample coincides with an FT pulse for a good event. The FT pulse width must be wide enough to cover all possible jitter between conditions.

The input gate and delays must be used to delay the fastest conditions to wait for the slowest input. The gate and delays can also be used to determine which input acts as a gate for which other (for example a wide logic input ANDed with a Fold≥n condition will be timed by the Ge, whereas a wide pulse derived from the Fold≥n ANDed with a narrow pulse from an ancillary detector via a logic input will be timed by the ancillary detector. All inputs are available on inspection lines (see 8.0) to facilitate set-up of complex triggers.

## 3 System Inputs for FT and Val decisions

In addition to the logic conditions placed on the inputs described in section 2, there are two other requirements that must be fulfilled before triggers may be generated. Firstly, the VXI GO bit in the experiment control window must be set to GO (i.e. the system must be running) and secondly the system must not be busy with a current event (in common dead time mode) or very close to a preceding event (parallel mode).

### 3.1 Definition of Busy (Triggers Blocked)

The Inhibit Action signal is set for a period controlled by the "Inhibit" slider at the start of every event recognised by the trigger card. In Common dead time operation it must be adjusted to cover at least the time from Fast Trigger to the start of readout. The Trigger is also blocked while the Readout* signal is true on the 14 way system input cable (daisy chained from all the VXI resource managers), indicating that at least one VXI crate is still reading data into its STR8080 buffer. During this time the trigger is busy. The Inhibit pulse may be programmed to a longer period (up to 35µs) for diagnostic purposes if there is a possible fault in the propagation of the Readout* signal.

In parallel mode the Inhibit Action signal (set for a period controlled by the "Inhibit" slider) is the only information used to determine whether the trigger is busy. The minimum pulse width is determined by the sum of the delay and width of the validation pulse. If the delay is 0 then the minimum period for Inhibit Action must be sufficient to create 2 distinct Validation pulses to start readout for the 2 successive events, i.e. Validation pulse width plus about 500ns.

#### 3.1.1 Inhibit Request

An Inhibit Request is generated by the logical OR of the front panel fast NIM (Lemo) InhReq input and the Inhibit Request in the 14 way system cable daisy chained from all the resource managers. In both parallel and common dead time, the Inhibit Request prevents the generation of any further Fast Triggers and Validations. However if Inhibit Request is asserted after FT and before Val, it does not prevent the validation for the event during which it is asserted, so 1 readout request (Validation) maybe be generated after Inhibit Request is asserted. Ancillary detector electronics may use the Inhibit Request signal to extend an event in common dead time mode by asserting Inhibit Request after the Fast Trigger and maintaining it until the ancillary detector is ready for another event.

Readout devices such as the STR8080 are designed to either issue an Inhibit Request before the completion of readout for the event which makes them become full, i.e. before the following Fast Trigger (common dead time mode only) or else to allow room in their buffers for at least one more event after issuing the Inhibit request (common dead time and parallel).

## 4 Output pulses

Using the inputs described in section 2, triggers are generated subject to the additional system requirements described in section 3 (VXI Go is true and the system is not busy).

The default LCA program will generate a Fast Trigger when:

(Sumbus 1 threshold 1 exceeded)
OR
(Sumbus 2 threshold 1 exceeded)
OR
(Sumbus 1 threshold 2 exceeded AND FP logic input 1 is true)
OR
(Sumbus 3 threshold 1 exceeded)
OR
(Sumbus 4 threshold 1 exceeded)

(All these inputs are taken from their attached gate and delay by the default program, so the trigger condition is SB1GD1 + SB2GD1 + (SB1GD2 & FPL1GD) + SB3GD1 +SB4GD1.)

**4.1 Fast Trigger**
The internal Fast Trigger signal from the FTV_LCA is generated when the FT condition described above (or a user generated equivalent) is satisfied.

The output of the FTV_LCA which triggers the FT gate and delay will also trigger the gate and delays called "Inhibit" (defining system dead time in parallel mode) and "Validation Gate" (defining the delay and width of the Validation Gate signal). There are sliders to control these delay and width settings.

There are 12 identical fast NIM FT outputs at the bottom of the front panel.

**4.1.1 Timing Reference Input (Tref)**
The timing of Fast Triggers generated from the sumbuses will vary slightly due to the use of a leading edge discriminator and the finite rise time of the sumbus pulse (the same threshold is reached at different times for different sumbus pulse sizes). In order to overcome this time walk when very accurate timing is required the FT output of the FTV_LCA can be gated with a Time reference, Tref. Typically Tref will be connected to RF from beam pulses or to a fast scintillator.

When the Tref Enable button is ticked, the Tref input is AND'ed with the FT output of the FTV_LCA and the result of the AND is used to trigger the gate and delay which generates the FT output pulse. NB there will be no FT output pulse if the Tref pulse is not supplied by the user and Tref is enabled. The Tref input is located in the middle of the front panel and requires a fast NIM pulse (or level).

To help the user set up the AND so that Tref is the later signal, three signals are available on the logic inspection lines: the FT_GD_TRIG_INSP and TREF_INSP inspection lines are the inputs for the AND condition, and Fast_Trigger is the output of the gate and delay triggered by the AND.

### 4.2 Validation
During the Validation Gate signal the Validation logic condition is checked.

The default setting is to validate every event, but the user may download a new trigger LCA setting from the library to introduce a validation logic condition, for example using a logic input from an ancillary detector. Different validation conditions may be applied for different trigger types (see section 2.3 for description of how to define trigger types) depending on what caused the FT. E.g. for high fold FT condition you might validate always, but for lower fold you might require that a logic input is present during Validation Gate.

The Validation output is generated when the Validation trigger condition (default - Validation Gate) is true and triggers the gate and delay generator controlled by the “Validation” sliders. The Validation is distributed to the rest of the system via the 40 way system cable daisy chained for the trigger to all VXI resource managers. One fast NIM (Lemo) output is provided on the front panel for ancillary detectors or diagnostics

Users should consider carefully the efficiency of their validating device if they introduce a validation condition. An example is given in Appendix B.

## 5 TAC

The Trigger card contains a TAC for use during experiments. It can be started by one of 4 signals (Front panel TAC Start, Sumbus 1 discriminator 1, Sumbus 2 discriminator 1, or Logic input 1). It can be stopped by one of 4 signals (Front panel TAC Stop, Sumbus 1 discriminator 1, Sumbus 2 discriminator 1, or Logic input 1). The start and stop signals are selected from pull down menus in the area of the window called “TAC Controls”. The TAC must be enabled by clicking the TAC enable. Front panel TAC start and stop signals require fast NIM levels and are located in the middle of the front panel.

Note that the ADC requires 2.7μs after TAC stop to convert its data, so you should delay the start of readout (back edge of Validation) until the ADC is not busy by either delaying or making wider the validation output. ADC busy and Validation are both available on logic inspection lines. If you read too soon then you will read the previous event’s data. The ADC is an 11 bit coder without sliding scale (actually 12 bits, but it operates from 0x800 to 0xFFF, using the 12th bit as a sign bit which is always true). TAC range is 2μs.

## 6 Readout of data

The trigger card provides up to 8 data parameters, each enabled or disabled under user control. The area of the window called “Readout Parameters” contains buttons to enable (when ticked) or disable the readout of the following parameters:

- Event number bottom 16 bits
- Event number top 16 bits
- Pattern/trigger type (from trigger selection LCA)
- TAC output
- Sumbus level from sumbus 1-4

The event number is incremented at the back edge of every validation pulse ready for the next event: the event number that is to be read for the current event is latched at the start of the validation pulse.

The sumbus level is coded by peak sensing ADCs where approximately 13 decimal corresponds to fold=1, 26 decimal to fold=2 etc.. The user should check this calibration in their own experimental apparatus to check for any variations in sumbus driver current or resource manager buffer gain.

## 7 Scalers

Eight scalers are provided and connected to the following signals:

1 = Fast Trigger Request (trigger condition) 1
2 = Fast Trigger Request (trigger condition) 2
3 = Fast Trigger Request (trigger condition) 3
4 = Fast Trigger Request (trigger condition) 4
5 = Fast Trigger out
6 = Validation out
7 = Readout cycles
8 = user defined

The scalers are displayed and controlled in the bottom right corner of the trigger window. There are 2 buttons for each scaler. The left button enables the scaler when ticked and the right button is a status indicator for 32 bit overflow. All scalers will be cleared by the clear button. Pressing the update button displays either the current total counts or the current rate (measured over a 3 second period) depending on the status of the Counts/Rates toggle buttons (yellow = selected, blue = not selected).

Scalers cannot be included in the event by event data stream.

## 8 Inspection Points

Inspection lines are provided for many internal signals and are controlled from the 5 pull down menus near the bottom of the card. There are 2 digital inspection lines and 2 analogue inspection lines and also a voltage inspection line.

Active levels and some typical timings are shown in Appendix C.

## 9 Reloading the LCA

To reload the FTV_LCA which defines for the trigger condition, press the “Load LCAs” button at the bottom of the window in the middle. This will bring up a new frame in which you must select the program you want to load and then click on the load button. The frame will disappear after a successful load. There is a status bar on the main trigger window which is called “Current LCA Program”.

## 10 “The Trigger Doesn’t work” Some common mistakes:

If there are no FT outputs from the trigger then the most likely cause it that you have set it up wrong! Here are some things to check:

1) Is VXI GO set? (look at the system control window)

2) Is Inhibit Request set (look at the Resource Manager window, selecting the resource manager for the VXI crate where the trigger is located)

3) Are the Ge CFDs enabled? (look for pulses on the sumbus using trigger analogue inspection lines)

4) Are the trigger sumbus discriminators enabled? (select the correct sumbus with the pull down menu and check the “Sumbus enable” tick box.)

5) If the sumbus discriminator is enabled and the sumbus input pulse can be seen then look for the discriminator output on the inspection line. If there is no output then check your sumbus threshold setting and adjust it until there is an output.

6) Look at the timing of the signals in your trigger equation: do the signals for any AND conditions overlap when viewed on the inspection lines?

7) Check the Tref button. If you tick Tref then you must provide a fast NIM pulse (or active level) during the internal FT pulse in order to trigger the FT output gate and delay.

If you get extra triggers then check the hidden sumbuses and logic inputs by looking at each part of the pull-down menu in turn. Unused sumbuses should be disabled and unused discriminators should be set to their default full scale value (fold≥23). The initial condition has all inputs disabled and discriminators at full scale. Whatever you set using VXI restore will over-ride the defaults, so be sure that you know what’s in the restore file for the hidden (undisplayed) menu items (usually sumbus 2,3,4 and logic inputs 2-7).

## Appendix A Trigger fold settings

| input voltage | sb1comp1 fires up to DAC=nn | equivalent fold | suggested DAC value (decimal) |
|---|---|---|---|
| -100mV | up to 8 | ≤1 | 6 |
| -200mV | up to 20 | ≤2 | 17 |
| -300mV | up to 31 | ≤3 | 28 |
| -400mV | up to 43 | ≤4 | 40 |
| -500mV | up to 54 | ≤5 | 51 |
| -600mV | up to 67 | ≤6 | 64 |
| -700mV | up to 78 | ≤7 | 75 |
| -800mV | up to 89 | ≤8 | 86 |
| -900mV | up to 102 | ≤9 | 99 |
| -1000mV | up to 113 | ≤10 | 110 |
| -1100mV | up to 125 | ≤11 | 122 |
| -1200mV | up to 136 | ≤12 | 133 |
| -1300mV | up to 148 | ≤13 | 145 |
| -1400mV | up to 159 | ≤14 | 156 |
| -1500mV | up to 170 | ≤15 | 167 |

## Appendix B Validation Efficiency

With a low efficiency device then the system will spend a large percentage of its time waiting for validations that never come. For example consider a trigger condition of gamma-fold≤2 validated by a 10% efficient ion detector which produces a signal 5µs after the gamma rays are detected.

In this case we would require a ValGate delay of 4.5µs and ValGate width of 1µs. So the system would trigger at a rate determined by the gamma-fold≤2 (for example = 50kHz) and receive good validations at a rate of 5kHz.

At a rate of 5kHz the system is dead for about 15µs including readout for a good event. At a rate of 45kHz the system is dead for 5.5µs waiting for validations that never come.

So dead time = 7.5% for good events and 24.75% for failed validations, total 32.25% dead time. Within that total dead time, 75% is due to failed events producing no data.

For 5% efficiency the total dead time becomes 30% and the percentage of total dead time due to failed events with no readout is 87.5%.

## Appendix C Inspection Line signals

To be added.

## Appendix D Specification of Euroball Trigger Card

The Trigger card is a D sized VXI card that examines a programmable set of its input signals using a Xilinx LCA FPGA and controls nuclear physics experiments based on those inputs.

Inputs:
4 analogue sumbus inputs connected to 4,3,2 and 1 leading edge discriminators for ≥ fold decisions using up to 4 different folds for each sumbus. LCA sees inputs both direct from discriminators, and also after programmable time alignment circuits (delay 0-2μs, width 0-2μs).
Total 20 inputs to trigger decision FPGA.

8 Front panel logic inputs with a common programmable threshold (fast NIM, ecl, TTL, slow NIM). 4 of these inputs are also connected to time alignment circuits (delay 0-12μs, width 0-12μs) making a total of 12 inputs to the trigger decision FPGA.

1 Front panel Time Reference signal (fast NIM) (used for very accurate Fast Trigger timing).

System input signals are connected via a14 way differential ecl cable. These are Readout, Inhibit Request and Coding. Inhibit Request may also be driven via a fast NIM input.

Stop and Start inputs for the trigger's TAC are provided.

Outputs:
Fast Trigger: (12 Fast NIM Lemo 00 outputs)

System output signals are connected via a 40 way differential ecl cable. These are: Validation, Synch for Test Pulsers, Event Number (bits 0-3), VXI GO, Clear, Event Reject, Inhibit Action and Transfer Scalers to shadow registers.

Fold discriminator logic output (1) for use by ancillary detectors.

Scalers:
The Trigger card contains 8 scalers (32 bit) to count Fast Triggers, Validations, Readout cycles, Trigger Requests and a user selected signal from the trigger decision FPGA.

TAC:
A 0-2μs TAC is provided with Stop and Start software selectable to come from either the front panel or from one of the sumbus fold discriminators.

Readout and VME Interface
The VXI backplane interface for readout and control uses the Euroball standard GIR.
Data words are defined by the configurable FPGAs. For Euroball they will be some or all of the trigger type, the event number the TAC and the sumbus fold levels coded in ADCs.
For EXOGAM a timer counter could be added in the fpga's if required (max. rate 25MHz).

System Control
The system event number is generated in the trigger card and distributed from it during readout. The LS 4 bits are also broadcast to maintain system synchronisation.

The Fast Trigger, validation, event rejection and flow control are all generated by the trigger card and the register where the VXI GO/STOP bit is generated is also located in the trigger card.