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EUROBALL PROJECT

G.I.R. Technical Document for F.V.I. (Fera to VXI Interface)

by: N. Karkour, D. Linget,

with the collaboration of J.L. Pedroza (C.E.N.B.G.)

1. *FVI* AP Description.

• 1.1) AP1 :

All the signals below are controlled by the *LCA DECODE1*.

- **CS_LUT1 :** Chip Select for the *LookUp Table* for the Fera channel 1.
- **CS_Req1TM :** Chip Select for the *Request time out* register for the Fera channel 1.
- **CS_Ren1Delay :** Chip Select for the *Renin Delay* register for the Fera channel 1.
- **CS_Gate1D :** Chip Select for the *Gate Delay* register for the Fera channel 1.
- **CS_Gate1W :** Chip Select of channel 1 for the *Gate Width* register for the Fera channel 1.
- **CS_FIFO1W:** Chip Select for the *FIFO* for the Fera channel 1.
- **CS1_vsn**m **:** Chip Select for the *VSN select* register; *m* is the *VSN* number (1 to 4).
- **CS_LUT2 :** Chip Select for the *LookUp Table* for the Fera channel 2.
- **CS_Req2TM :** Chip Select for the *Request time out* register for the Fera channel 2.
- **CS_Ren2Delay :** Chip Select for the *Renin Delay* register for the Fera channel 2.
- **CS_Gate2D :** Chip Select for the *Gate Delay* register for the Fera channel 2.
- **CS_Gate2W :** Chip Select for the *Gate Width* register for the Fera channel 2.
- **CS_FIFO2W:** Chip Select for the *FIFO* for the Fera channel 2.
- **CS2_vsn**m **:** Chip Select of channel 2 for the *VSN* register; *m* is the *VSN* number (1 to 4).
- **Strobe_*FVI* :** Strobe signal used to latch the datas inside the *FVI* card during a complete *VME* cycle.
- **ft_tmout :** Chip Select for the *time out* register of the *FT (Fast Trigger)* pulse signal.
- **ft_delay :** Chip Select for the *delay* register of the *FT* pulse signal.
- **ft_width :** Chip Select for the *width* register of the *FT* pulse signal.
- **ft_counter :** Chip Select for the load operation of the *FT* counter.
- **val_tmout :** Chip Select for the *time out* register of the *VAL (Validation)* pulse signal.
- **val_delay :** Chip Select for the *delay* register of the *VAL* pulse signal.
- **val_width :** Chip Select for the *width* register of the *VAL* pulse signal.
- **val_counter :** Chip Select for the load operation of the *VAL* counter.
- **trig_counter :** Chip Select for the load operation of the *trigger* counter.
- **Go*/Stop :** This signal is the *EUROBALL III* GO*/STOP.
- **Card_select :** This signal can be used to enable the data bus buffer on the *Analog* card. It is active, during a complete *VME* cycle, when the *G.I.R.* is selected.
- **SclkProm:** serial *PROM* Clock signal of the *FVI Analog* card.
- **CSProm :** serial *PROM* Chip Select signal of the *FVI Analog* card.
- **DProm_Write:** serial *PROM* Data write to the *FVI Analog* card.
- **DProm_Read:** serial *PROM* Data to be read out of the *FVI Analog* card.

(see E²Prom connection figure).

- **FTPulseTest :** Calibrated *FT* pulse signal used for the test ($\cong$ 200 ns).
- **ValPulseTest :** Calibrated *VAL* pulse signal used for the test ($\cong$ 200 ns).
- **TrigPulseTest :** Calibrated *Trigger* pulse signal used for the test ($\cong$ 200 ns).
- **ClrFTcounter :** Clear signal for the *FT* counter.
- **ClrValcounter :** Clear signal for the *VAL* counter.
- **ClrTrigcounter :** Clear signal for the *Trigger* counter.
- **Reg_Io :** these signals are not used in the *FVI* card, they are controlled by the *LCA DECOD1*. They can be used by the *Analog* card for future applications.

All the signals below fixed signal.

- **ADD[7..1] :** this is the lowest byte of the *VME* Address bus, it is enabled by the *LCA DECOD1*.

- **AFLAG1 :** Free Analog signal from the *Analog* card, controlled by the *DSP* (via an *ADC*).
- **RDFLAG1,2 :** Free Digital signals from the *Analog* card, controlled by the *LCA READOUT*.
- **LED 1:** display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

ALL Chip Select Signals are TTL Active high signals except that of CSPROM signal.

• 1.2) AP2 :

- 16 MHz: buffered *VME* System Clock signal.

- MReg: 8 bits Module Register, each signal enable or disable a common function on the *Analog* card :

0 ==> Test/Run* : mode of operation.
1 ==> ET0 : .
2 ==> ET1 : .
3 ==> Reject : enable/disable* the rejection.
4 ==> WP Prom : DIsable/Enable* E²Prom Write Protect.
5 ==> Req1 : enable the Request for the Fera channel 1 interface.
6 ==> Req2 : enable the Request for the Fera channel 2 interface.
7 ==> CDT : Common Dead Time mode register.

<u>All the signals below fixed signal.</u>

- ADD[23..8] : these are the other 2 bytes of the *VME* Address bus, they are enabled by the *LCA DECOD1*.

- AIn **:** Analogue Inspection Lines, n is the inspection line indicator.

- DIn **:** Digital Inspection Lines, n is the inspection line indicator.

- VI : Voltage Inspection Line.

- DATA[15..0] : these are the lower sixteen bits of the *GIR* Analog Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SAROC* and *FIFO* data bus during Readout mechanism.

- EVT_IN[3..0] : these lines are the current event number, they are given by the *MASTER Trigger* via the *VXI Local* bus to the Analog cards with *Validation* (LBus [11..8]).

<u>All the signals below are controlled by the Readout *LCA*.</u>

- Datatready : data ready given by the *Readout Chip* when a data is ready to be latched in the *FIFO*.

- Dtack : buffered data acknowledge signal for each data word of the *Readout Chip* in a Readout cycle.

- Renin : start Readout cycle for the *FVI* card.

- LPass : Last PASS, this is the renout signal of the *FVI* and it presents the end of the internal Readout cycle.

- GLOBAL RESET : buffered global Reset signal of all the *Analog* card.

- R/W_buf : buffered *VME* read-write signal.

- Valack : *Validation Acknowledge* signal given by the *FVI* card. This signal is active during validation to validate that there are data to be read out.

- StartReadout : ???? This signal latches the *ADC* data in the *SAROC* internal registers, the back edge of this signal starts the internal Readout cycle.

- LT_Reset : buffered Reset signal for the *Local Trigger*.

- Coding : This is the coding dead time signal, which indicates that the *ADC* are coding, and no *VME* Action must take place. This signal goes to the *MASTER Trigger* as an open collector at the Back plane.

- Reg_Io : these signals are not used in the *FVI* card, they are controlled by the *LCA DECODE2*. They can be defined for future applications.

- READ [17, 16, 8, 5..2] : these signals are dedicated for Readout interface and are not used in the *FVI* card, they are controlled by the *LCA READOUT*. They can be defined for future applications.

<u>All the signals below fixed signal.</u>

- AFLAG2 : Free Analog signal from the *Analog* card, controlled by the *DSP* (via an *ADC*).

- RDFLAG3,4 : Free Digital signals from the *Analog* card, controlled by the *LCA READOUT*.

- LED2 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

• 1.3) AP3 :

<u>All the signals below fixed signal.</u>

- DATA[31..16] : these are the sixteen higher bits of the *GIR* Analog Data bus. This bus has 2 functions : it is the *VME* data bus during read-write operation of the *SAROC* and *FIFO* data bus during Readout.

- EVT_out[3..0] : these lines are the event number that are sent with the data during acquisition mode, and are written in the *FIFO*.

- READ [22..18] : these signals are dedicated for Readout interface and are not used in the *FVI* card, they are controlled by the *LCA READOUT*. They can be defined for future applications.

- FT_ttl_buf : buffered *Fast Trigger* signal (positive TTL) from the *MASTER Trigger* (*starx* on the *VXI* back plane).

- Inhibit_buf : buffered *Inhibit* signal from the *MASTER Trigger* (on the *VXI* back plane).

- VAL_buf : buffered *Validation* signal from the *MASTER Trigger* (on the *VXI* back plane).

- FT_ECL -, FT_ECL+ : *Not used signals by the FVI card.*

- DSPFLAG1, 2, 3 : these signals are not used for the moment in *Euroball*. They can be used later as a connection between the *DSP*, and the *FVI* card. They are controlled by the *DSP*.

- LED3 : display signal of a *LED* indicator driven by an open collector from *G.I.R.* to the front panel.

<u>All the signals below are controlled by the *LCA DECODE2*.</u>

- EF1, EF2 : Empty flag signals of *FVI* Fifo Channel 1, and 2 respectively.

- HF1, HF2 : Half Full flag signals of *FVI* Fifo Channel 1, and 2 respectively.

- FF1, FF2 : Full flag signals of *FVI* Fifo Channel 1, and 2 respectively.

- Inhibit_FVI : Inhibit signal of the *Diamant Trigger*.

- Reject_FVI : Reject signal of the *Diamant Trigger*.

- DigSelAn **:** select signal of the digital multiplexers for the digital inspection line 1, *n* is the multiplexer select bit (n = 0 to 3).

- DigSelBn **:** select signal of the digital multiplexers for the digital inspection line 2, *n* is the multiplexer select bit (n = 0 to 3).

- DigOE1 & **2:** output enable signal of the multiplexers for the Digital Inspection lines 1 & 2.

- VSel[3..0] : select bus of the voltage multiplexers. These signals must be common to all voltage multiplexers.

- Venable : enable signal of the voltage multiplexer.

- Reg_Io : these signals are not used in the *Euroball* BGO cards, they can be defined for future applications.

- Vstrobe: load signal of all the voltage multiplexers.

- LBUSA[31:30]: VXI Local bus signals from the Backplane.

- LBUSC[31:30]: VXI Local bus signals from the Backplane.

Pinouts of the *FVI* AP Connector:

	AP1 Connector			AP2 Connector			AP3 Connector			
PIN NO.	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	ROW A	ROW B	ROW C	PIN NO.
1	+5 V	VPTAT	+5 V	+5 V	AFLAG2	+5 V	+5v	DSPFLAG1	+5v	1
2	+5 V	+5v	+5 V	+5 V	+5 V	+5 V	+5v	+5v	+5v	2
3	CS_Lut1	OVER 1	CSReq1Tm	Reg_Io	RDFLAG3	Reg_Io	DATA 16	DSPFLAG2	DATA 17	3
4	CSRen1Delay	UNDER1	CSGate1D	Reg_Io	RDFLAG4	Reg_Io	DATA 18	DSPFLAG3	DATA 19	4
5	CSGate1W	LED	CSCTRL1	Reg_Io	LED	Reg_Io	DATA 20	LED	DATA 21	5
6	CS_FIFO1	GND	CS1_vsn1	16 Mhz	GND	Reg_Io	DATA 22	GND	DATA 23	6
7	CS1_vsn2	GND	CS1_vsn3	GND	GND	Test/Run*	GND	GND	GND	7
8	CS1_vsn4	GND	CS_Lut2	ADD 8	GND	ADD 9	DATA 24	GND	DATA 25	8
9	CSReq2Tm	GND	CSRen2Delay	ADD 10	GND	ADD 11	DATA 26	GND	DATA 27	9
10	CSGate2D	GND	CSGate2W	ADD 12	GND	ADD 13	DATA 28	GND	DATA 29	10
11	CSCTRL2	GND	CS_FIFO2	ADD 14	GND	ADD 15	DATA 30	GND	DATA 31	11
12	CS2_vsn1	GND	CS2_vsn2	ADD 16	GND	ADD 17	GND	GND	GND	12
13	CS2_vsn3	GND	CS2_vsn4	ADD 18	GND	ADD 19	EVT_out0	GND	EVT_out1	13
14	Strobe_*FVI*	GND	ft_tmout	ADD 20	GND	ADD 21	EVT_out2	GND	EVT_out3	14
15	ft_delay	GND	ft_counter	ADD 22	GND	ADD 23	READ 18	GND	READ 19	15
16	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	16
17	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	17
18	ft_width	GND	val_tmout	ET0	GND	ET1	READ 20	GND	READ 21	18
19	val_delay	GND	val_width	Reject	GND	WP Prom	FT_ECL +	GND	READ 22	19
20	val_counter	GND	trig_counter	AI 1	GND	GND	GND	GND	FT_ECL -	20
21	SclkProm	GND	DProm_write	GND	GND	GND	FT_ttl_buf	GND	Inhibit_buf	21
22	CSProm	GND	Dprom read	AI 2	GND	GND	VAL_buf	GND	Stat_test	22
23	FTPulseTest	GND	ValPulseTest	GND	GND	DI 1	EF1	GND	EF2	23
24	TrigPulseTest	GND	ClrFTCounter	DI 2	GND	GND	HF1	GND	HF2	24
25	ClrValCounter	GND	ClrTrigCounter	Req1	GND	VI	FF1	GND	FF2	25
26	Go*/Stop	GND	Card_Select	Req2	GND	CDT	Inhibit_FVI	GND	Reject_FVI	26
27	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	-5.2 V	GND	-5.2 V	27
28	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	-5.2 V	28
29	Reg_Io	GND	Reg_Io	DATA 0	GND	DATA 1	DigSelA0	GND	DigSelA1	29
30	Reg_Io	GND	Reg_Io	DATA 2	GND	DATA 3	DigSelA2	GND	DigSelA3	30
31	Reg_Io	GND	Reg_Io	DATA 4	GND	DATA 5	DigSelB0	GND	DigSelB1	31
32	Reg_Io	GND	Reg_Io	DATA 6	GND	DATA 7	DigSelB2	GND	DigSelB3	32
33	Reg_Io	GND	Reg_Io	GND	GND	GND	DigOE1	GND	DigOE2	33
34	Reg_Io	GND	Reg_Io	DATA 8	GND	DATA 9	Reg_Io	GND	Reg_Io	34
35	Reg_Io	GND	Reg_Io	DATA 10	GND	DATA 11	Reg_Io	GND	Reg_Io	35
36	Reg_Io	GND	Reg_Io	DATA 12	GND	DATA 13	Reg_Io	GND	Reg_Io	36
37	Reg_Io	GND	Reg_Io	DATA 14	GND	DATA 15	Reg_Io	GND	VSel0	37
38	Reg_Io	GND	Reg_Io	EVT_IN0	GND	EVT_IN1	VSel1	GND	VSel2	38
39	Reg_Io	GND	Reg_Io	EVT_IN2	GND	EVT_IN3	VSel3	GND	VEnable	39
40	Reg_Io	GND	Reg_Io	DataReady	GND	Dtack	Reg_Io	GND	Reg_Io	40
41	Reg_Io	GND	Reg_Io	READ 2	GND	READ 3	Reg_Io	GND	Reg_Io	41
42	Reg_Io	GND	Reg_Io	READ 4	GND	READ 5	Reg_Io	GND	Reg_Io	42
43	Reg_Io	GND	Reg_Io	Read 6_buf	GND	Renin	Reg_Io	GND	Reg_Io	43
44	Reg_Io	GND	Reg_Io	READ 8	GND	LPass	Reg_Io	GND	Reg_Io	44
45	Reg_Io	GND	ADD1	GlobalReset	GND	R/W_buf	Reg_Io	GND	VStrobe	45
46	ADD2	GND	ADD3	Valack	GND	StartReadout	Reg_Io	GND	Reg_Io	46
47	ADD4	GND	ADD5	LTReset	GND	Coding	LBUSA31	GND	LBUSC31	47
48	ADD6	GND	ADD7	READ 16	GND	READ 17	LBUSA30	GND	LBUSC30	48
49	+5 V	GND	+5 V	+5 V	GND	+5 V	+5 V	GND	+5 V	49
50	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V	50
51	-2 V	GND	-2 V	+12 V	GND	+12 V	+24 V	GND	+24 V	51
52	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	52
53	-2 V	-2 V	-2 V	+12 V	+12 V	+12 V	+24 V	+24 V	+24 V	53
54	-2 V	GND	-2 V	-12 V	GND	-12 V	-24 V	GND	-24 V	54
55	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	55
56	-2 V	-2 V	-2 V	-12 V	-12 V	-12 V	-24 V	-24 V	-24 V	56

2 Memory Map of the G.I.R. for the *FVI* Card

2.1 VXI Configuration Registers: (Inside the G.I.R.)

The *VXI* base address is calculated as follow : 0xFFFFFF80 - (n * 0x40) where n is the number of cards between the *Resource Manager* and the Target card (n = 0 to 11).

***VXI Base Address** first card*	***Description***	***DATA Format***
0xFFFFFF80	In Read Mode this is the Man. ID. Device Class and Address Space	d15, d14 = 0x3, d13, d12=01(A16/A32) or 00 (A16/A24), d11, d8 =1111for IN2P3 d7,d0=Pr (0x5A) for IN2P3 from PROM
0xFFFFFF80	In Write mode the R.M. Writes the Logic Address of the VXI card in A13,A6	D7 to D0 is the logical Address
0xFFFFFF82	Read Only Register for the Device type and the model code	d15,d12 = 0x 7 (A24) or 0xf (A32) d11,d8=model code d7 to d0 from PROM
0xFFFFFF84	In Read mode: Status Register	d15 to d0
0xFFFFFF84	Write mode: Control Register	d15 to d0
0xFFFFFF86	Read/Write Offset Register	d15,d8 for A24, d15,d0 for A32
0xFFFFFF88	Read Only: Serial no.	Read 8 bits only from PROM d7 to d0
0xFFFFFF8a	Read Only: Modification Level	Read 8 bits only from PROM d7 to d0

2.2 Channel Area Addresses

Channel 1 (0x10000 --0x1FFFE)	**Bus Width**	**Read/ Write**	**Function**
0x10000 to 0x17FFE	16	r/w	LookUp Table for Channel 1 (32 Kwords)
0x18000	16	r/w	Request 1 Timeout Register
0x18002	16	r/w	Ren1 Delay Register
0x18004	16	r/w	Gate 1 Delay register
0x18006	16	r/w	Gate 1 Width register
0x18008	16	r/w	Fera Channel 1 Control Register
0x1800C	32	r/w	Fera Channel 1 Fifo Test Acess
Channel 2 (0x20000 --0x2FFFE)	**Bus Width**	**Read/ Write**	**Function**
0x20000 to 0x27FFE	16	r/w	LookUp Table for Channel 2 (32 Kwords)
0x28000	16	r/w	Request 2 Timeout Register
0x28002	16	r/w	Ren 2 Delay Register
0x28004	16	r/w	Gate 2 Delay register
0x28006	16	r/w	Gate 2 Width register
0x28008	16	r/w	Fera Channel 2 Control Register
0x2800C	32	r/w	Fera Channel 2 Fifo Test Acess

2.3 Common Area Addresses

2.3.2 Common Registers:

Global Addresses	Bus Width	Read/ Write	Function
0x0	xx	w only	Simulate 250 ns FT Pulse
0x2	xx	w only	Simulate 250 ns Validation Pulse
0x4	xx	w only	Simulate 250 ns Trig Pulse
0x6	xx	w only	Generate 250 ns Clear FT Counter
0x8	xx	w only	Generate 250 ns Clear Validation Counter
0xA	xx	w only	Generate 250 ns Clear Trig Counter
0x10	16	r/w	Module Control Register (MCR)
0x12	16	Read Only	Status Register (*FVI* STAT)
0x20	16	r/w	Digital Inspection 1 channel select
0x22	16	r/w	Digital Inspection 1 parameter Select
0x24	16	r/w	Digital Inspection 2 channel select
0x26	16	r/w	Digital Inspection 2 parameter Select
0x30	16	r/w	Voltage Inspection channel select
0x32	16	r/w	Voltage Inspection parameter Select
0x40--0x5E	16	r/w	*FVI* Card Configuration Registers (XCProm)
0x60	16	r/w	FT Timeout Register
0x62	16	r/w	FT Delay Register
0x64	32	r/w	FT Counter Register
0x68	16	r/w	FT Width Register
0x6A	16	r/w	Validation Timeout Register
0x6C	16	r/w	Validation Delay Register
0x6E	16	r/w	Validation Width Register
0x70	32	r/w	Validation Counter Register
0x74	32	r/w	Ancillary Trigger Counter Register
0x78	16	r/w	VSN Select 1 Register
0x7A	16	r/w	VSN Select 2 Register
0x7C	16	r/w	VSN Select 3 Register
0x7E	16	r/w	VSN Select 4 Register
0xA0--0xBE	16/32	r/w	G.I.R. Readout Memory Map

2.3.2.1 Module Control Register: VME base Address : 0x10 (read/ write)

Bit Number	Meaning when = 0	Meaning when = 1
0	Test Register Inactif	Test Register Actif
1	ET 0 Register Disabled	ET 0 Register Enabled
2	ET 1 Register Disabled	ET 1 Register Enabled
3	Reject Register Disabled	Reject Register Enabled
4	*FVI* Card PROM Write Disable	*FVI* Card PROM Write Enable
5	REQ1 Register Disabled	REQ1 Register Enabled
6	REQ2 Register Disabled	REQ2 Register Enabled
7	CDT Register Disabled	CDT Register Enabled
8	Reset FIFO Disable	FIFO Reset
9	Reset G.I.R. FIFO Disable	G.I.R. FIFO Reset
10	Reset G.I.R. Disable	G.I.R. Reset
11	Not Last Card	Last Card (use terminators)
12	not yet defined	not yet defined
13	not yet defined	not yet defined
14	not yet defined	not yet defined
15	not yet defined	not yet defined

2.3.2.2 *FVI* Status Register: VME base Address : 0x12 (read only)

Bit Number	Meaning when = 0	Meaning when = 1
0	Test Register Inactif	Test Register Actif
1	Empty Flag FIFO1 Disabled	Empty Flag FIFO1 Enabled
2	Empty Flag FIFO2 Disabled	Empty Flag FIFO2 Enabled
3	Half Full Flag FIFO1 Disabled	Half Full Flag FIFO1 Enabled
4	Half Full Flag FIFO2 Disabled	Half Full Flag FIFO2 Enabled
5	Full Flag FIFO1 Disabled	Full Flag FIFO1 Enabled
6	Full Flag FIFO2 Disabled	Full Flag FIFO2 Enabled

7	Inhibit FVI Register Enabled (resetted when read)	Inhibit FVI Register Disabled
8	Reject Register Enabled(resetted when read)	Reject Register Disabled
9 to 15	Not Used	Not Used

2.3.2.3 Digital inspection lines:

Digital Inspection line 1 : VME base Address : 0x20 (channel Select), and 0x22 (parameter Select)
To Disable the Digital inspection Line 1 write 0x00 at address 0x22. DigselA[3..0]
Digital Inspection line 2 : VME base Address : 0x24 (channel Select), and 0x26 (parameter Select).
To Disable the Digital inspection Line 2 write 0x00 at address 0x26. DigselB[3..0]

parameters Line1 = DigselA[3..0] Line2 = DigselB[3..0]	GIR Control Lines to Analogue Card DigselA[3..0] DigselB[3..0]	Data Value for channel Address	Data Value for Parameter Address
DISABLED	0000	0x0	xxxx
WST 1	0000	0x 1	0x 0
REN 1	0001	0x 1	0x 1
GATE 2	0010	0x 1	0x 2
WST 2	0011	0x 1	0x 3
REN 2	0100	0x 1	0x 4
GATE 1	0101	0x 1	0x 5
RESET	0110	0x 1	0x 6
Inhibit	0111	0x 1	0x 7
Reject	1000	0x 1	0x 8
Trigger	1001	0x 1	0x9
REQ1	1010	0x 1	0xA
REQ2	1011	0x 1	0xB
WST 1	1100	0x 1	0xC
READFIFO1	1101	0x1	0xD
READFIFO2	1110	0x1	0xE
G.I.R. Parameters	**GIR Control Lines**	**Data Value for channel Address**	**Data Value for Parameter Address**
Fast_Trigger	0x001	0x 20	0x001
Inhibit	0x002	0x 20	0x002
Validation	0x003	0x 20	0x003
Veto	0x004	0x 20	0x004
***FVI* Valack**	0x005	0x 20	0x005
En_Int_Readout_TEST	0x006	0x 20	0x006
StartReadout	0x007	0x 20	0x007
Renin (SAROC)	0x008	0x 20	0x008
SAROCDTready0	0x009	0x 20	0x009
	0x00A	0x 20	0x00A
	0x00B	0x 20	0x00B
	0x00C	0x 20	0x00C
SAROCDTack_buf	0x00D	0x 20	0x00D
	0x00E	0x 20	0x00E
	0x00F	0x 20	0x00F
	0x010	0x 20	0x010
	0x011	0x 20	0x011
End Readout	0x012	0x 20	0x012
CSA *(FifoChipSelect_A)	0x013	0x 20	0x013
CLKA(FifoClock_A)	0x014	0x 20	0x014
ENA(Fifo Enable Port_A)	0x015	0x 20	0x015
AS* (VME)	0x016	0x 20	0x016
DS (DS0* and DS1*) (VME)	0x017	0x 20	0x017
R/W* (VME)	0x018	0x 20	0x018
ModRoco	0x019	0x 20	0x019
CardRenin *(From ROCO)	0x01A	0x 20	0x01A
BLTACK (Card)	0x01B	0x 20	0x01B
BLTACK (Bus)	0x01C	0x 20	0x01C
OE_Ident*	0x01D	0x 20	0x01D
CSB* (FifoChipSelect_B)	0x01E	0x 20	0x01E
CLKB (FifoClock_B)	0x01F	0x 20	0x01F
ENB (Fifo Enable Port_B)	0x020	0x 20	0x020

OR_fifo (EmptyFlag)	0x021	0x 20	0x021
FDTACK	0x022	0x 20	0x022
DTACK* (VME)	0x023	0x 20	0x023
CardRenout(Bus Renout)	0x024	0x 20	0x024
SysClk	0x025	0x 20	0x025
LT_Reset*	0x026	0x 20	0x026
Readout_Event_Match	0x027	0x 20	0x027
Reset_Fifo*	0x028	0x 20	0x028
Decode_Sel(CardChipSelect)	0x029	0x 20	0x029
Strobe_Dec2	0x02A	0x 20	0x02A
Dclk	0x02B	0x 20	0x02B
DCS*	0x02C	0x 20	0x02C
DDin	0x02D	0x20	0x02D
Coding_Bus	0x02E	0x20	0x02E
Coding_GIR	0x02F	0x20	0x02F
Event Fault more than one	0x030	0x20	0x030
Readout Event Fault	0x031	0x20	0x031
Vme Address 1	0x032	0x20	0x032
Vme Address 2	0x033	0x20	0x033
Vme Address 3	0x034	0x20	0x034
Vme Address 4	0x035	0x20	0x035
Vme Address 5	0x036	0x20	0x036
Not Used (DI Disable)	Disable	value not = 0x20	xxxx

2.3.2.4 Voltage inspection line:

VME base Address : 0x30 (channel select), and 0x32 (parameter select).

To Disable the Voltage Inspection line : write 0x00 at address 0x32

parameters	GIR Control Lines to Analogue Card Vsel[3..0]	GIR Control Lines to Analogue Card Venable	Data Value for channel Address	Data Value for Parameter Address
VCC +5 Volts	0000	01	*0x1*	0x0
Gnd	0001	01	*0x1*	0x 1
VEE -5.2Volts	0010	01	*0x1*	0x 2
VBB -2 Volts	0011	01	*0x1*	0x 3
		01	*0x1*	0x 4
		01	*0x1*	0x 5
		01	*0x1*	0x 6
		01	*0x1*	0x 7
		01	*0x1*	0x 8

2.3.2.5 *FVI* Configuration Registers (XC PROM): 8 bits(read only)

VXI Base Address	*Description*
0x40	In Read Mode this is the Man. ID
0x42	CARD TYPE
0x44	Serial no.
0x46	Revision Level
0x48 to 5E	SPARE

2.3.2.6 G.I.R. Readout Memory Map : VME base Address : 0xA0 to 0xBE.

Base Addresses	Bus Width	Read/ Write	Function
0xA0	16	r/w	Event Counter Register
0xA2	16	r/w	Item + Group no. Register
0xA0	32	read only	Item + Group no. Register + Event Counter
0xA4	32	r/w	Fifo Test Enable
0xA8	16	r/w	G.I.R. Readout Control Register (RCR)
0xAA	N.A.	r only w only	Start Readout out in test mode End Readout in test mode
0xAC	16	r only	Readout, Temperature Status Register
0xAE	16	r/w	Valack Timeout Register (multiple of 62.5 ns) (100 <t< 4 sec.) (active when bit2 of RCR is 1) e.g. to have 100 us timeout write the value 0x640 (1600).
0xB0	32	r only	Qstat1,Qstat0 counter (16 bit each). The Qstat1 counter is to count the number of event faults difference more than one. Qstat0 counter for the number of event faults
0xB4 to 0xBE	N.A.	r/w	Not yet Implemented

2.3.2.6.1 G.I.R. Readout Control Register (RCR) (*not fixed*):

VME base Address : 0xA8 to be upgraded

Bit Number	Meaning when = 0	Meaning when = 1
0	Run mode for SAROC readout	Test mode for SAROC readout
1	Run mode for External readout	Test mode for External readout
2	Disable Valack Timeout Reset	Enable Valack Timeout Reset
3	Enable Readout from G.I.R.	Disable Readout from G.I.R. (card is bypass)
4	Not yet defined	Not yet defined
5	no pipelining at all (dead until VXI Readout ends)	Pipeline Readout stage (dead until data are in FIFO) (N.A.Y.)
6	Event Number Readout off	Event Number Readout on
7	Common Deadtime Readout mode (Eurogam I & II)	Euroball Readout mode
8	DSP set to Slave Mode(N.A.Y.)	DSP set to Master Mode(N.A.Y.)
9	DSP Slave is not last Slave Card(N.A.Y.)	DSP Slave is the last Slave Card(N.A.Y.)
10	Contrôle des fenêtres off(N.A.Y.)	Contrôle des fenêtres on(N.A.Y.)
11	Use Event Number Q = 00 given by 0xa2 register	Use Event Number Q from G.I.R. (qstat1,qstat0) (see table below)
12	Not yet defined	Not yet defined
13	Not yet defined	Not yet defined
14	Not yet defined	Not yet defined
15	Not yet defined	Not yet defined

(N.A.Y.) (Not Available Yet)

2.3.2.6.1.1 G.I.R. Qstatus Table:

Qstat1:Qstat0	Meaning When Set
00	Trigger Broad cast nibble is equal to G.I.R. event counter Least Significant Nibble
01	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **more than one**
10	The difference betwseen Trigger Broad cast nibble and the G.I.R. event counter is **one**

2.3.2.6.2 G.I.R. Readout Status Register (*not fixed*): VME base Address : 0xAC

Bit Number	Meaning when = 0	Meaning when = 1
0	G.I.R. Temperature indicator is above the upper threshold	G.I.R. Temperature indicator is below the upper threshold
1	G.I.R. Temperature indicator is below the lower threshold	G.I.R. Temperature indicator is above the lower threshold
2	Temperature indicator 1 is above the upper threshold	Temperature indicator 1 is below the upper threshold
3	Temperature indicator 1 is below the lower threshold	Temperature indicator 1 is above the lower threshold
4	Temperature indicator 2 is above the upper threshold	Temperature indicator 2 is below the upper threshold
5	Temperature indicator 2 is below the lower threshold	Temperature indicator 2 is above the lower threshold
6	Valack Timeout deasserted	Valack Timeout asserted
8	G.I.R. Empty Flag of Fifo1 asserted	G.I.R. Empty Flag for Fifo1 deasserted
9	G.I.R. Full Flag of Fifo1 asserted	G.I.R. Full Flag for Fifo1 deasserted
10	G.I.R. Empty Flag of Fifo2 asserted	G.I.R. Empty Flag for Fifo2 deasserted

11	G.I.R. Full Flag of Fifo2 asserted	G.I.R. Full Flag for Fifo2 deasserted
12	Global Saroc_Empty asserted	Global Saroc_Empty deasserted
13	Status: No fault	Status: fault 0
14	Status: No fault	Status: fault 1
15	Status: No fault	Status: fault 2

10.3. <u>Dac connection figure Serial E²Prom, & Temperature Sensor Connection figure :</u>