EUROBALL III Cluster Card Specification

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Status:
This document describes the electronics discussed and agreed by the electronics engineers and an ECC representative in Heidelberg during March 1994. It has been updated to include changes requested by the detector group and changes to the readout part which were decided on 4th July in the EEDA meeting at Daresbury (v2.0). November update to v2.1 following GIR meeting in Orsay on 17-18/11/94 and Euroball User Meeting in Sept 1994.

The Euroball Cluster detector comprises 7 Germanium (Ge) elements surrounded by Bismuth Germanate (BGO). At the sides there is a shield made from 12 crystals of BGO and at the back a BGO back-catcher made from a further 6 BGO crystals. The Cluster detector electronics will comprise 3 VXI cards per Cluster detector, the first containing analogue electronics for 7 Ge crystals (plus one spare channel), the second containing electronics for 18 BGO crystals with one spare channel plus one composite (sum energy and pattern) BGO channel. The third card will enhance the Ge signal processing by adding 8 PPADC channels.

The Ge channels will produce 3 parameters: 2 energy ranges and 1 timing range. The BGO composite channel will also produce 3 parameters: the sum energy, the earliest crystal's timing and a hit pattern of all the crystals. The other BGO channels will produce timing and energy for each crystal. The PPADC card will be triggered through the analogue Ge card. The PPADC card will perform high resolution energy coding in a more flexible way and to a better resolution for a given processing time than the analogue Ge channel. It introduces the possibility of such things as neutron damage correction, adaptive pulse shaping to reduce pileup losses, and also pulse shape analysis if sufficiently fast flash ADCs are available.

The Ge analogue cards will initially be "monolithic" (one piece motherboard) similar to the Eurogam Clover cards in that the readout and VXI/VME interface will be on the main PCB itself. This has the advantages of making best use of the available space, is mechanically rigid, and allows early prototype delivery, but leaves no scope for upgrades in the future. To allow upgradeablity the production Ge cards will be developed using a General Interface and Readout (GIR) card for VXI/VME interface and readout. All the BGO cards will use the GIR including prototypes because the "learning curve" involved in putting a VXI interface and readout on a prototype card would be longer than using a GIR.

The Cluster electronics will operate in local common dead-time mode, that is to say when an event is detected in the Cluster detector, all channels associated with that detector will be prevented from processing subsequent events until the first is finished. This implements the parallel readout scheme requested by the ECC. In addition, a software selectable simple pipeline will be incorporated. This will give the option of defining that the event processing is finished when the data are in a FIFO ready for VXI readout rather than at the completion of VXI backplane readout, therefore pipelining the readout stage. The monolithic cards will use parallel Eurogam readout only. Later GIR cards will support both the modified VME D64 SSBLT cycles used by Christoph Ender's Crystal Ball VXI electronics and parallel Eurogam readout. NB parallel Eurogam readout requires the use of event numbers to identify the event being read over the VXI backplane since during parallel operation there can be 2 or more events ready for readout when a readout cycle starts. While the Eurogam readout specification supports this event selection at readout time, the Eurogam phase 1 and 2 cards do not all implement this part of the specification. Therefore, care must be taken when operating Euroball cluster VXI cards together with Eurogam VXI cards which cannot distinguish multiple parallel events.

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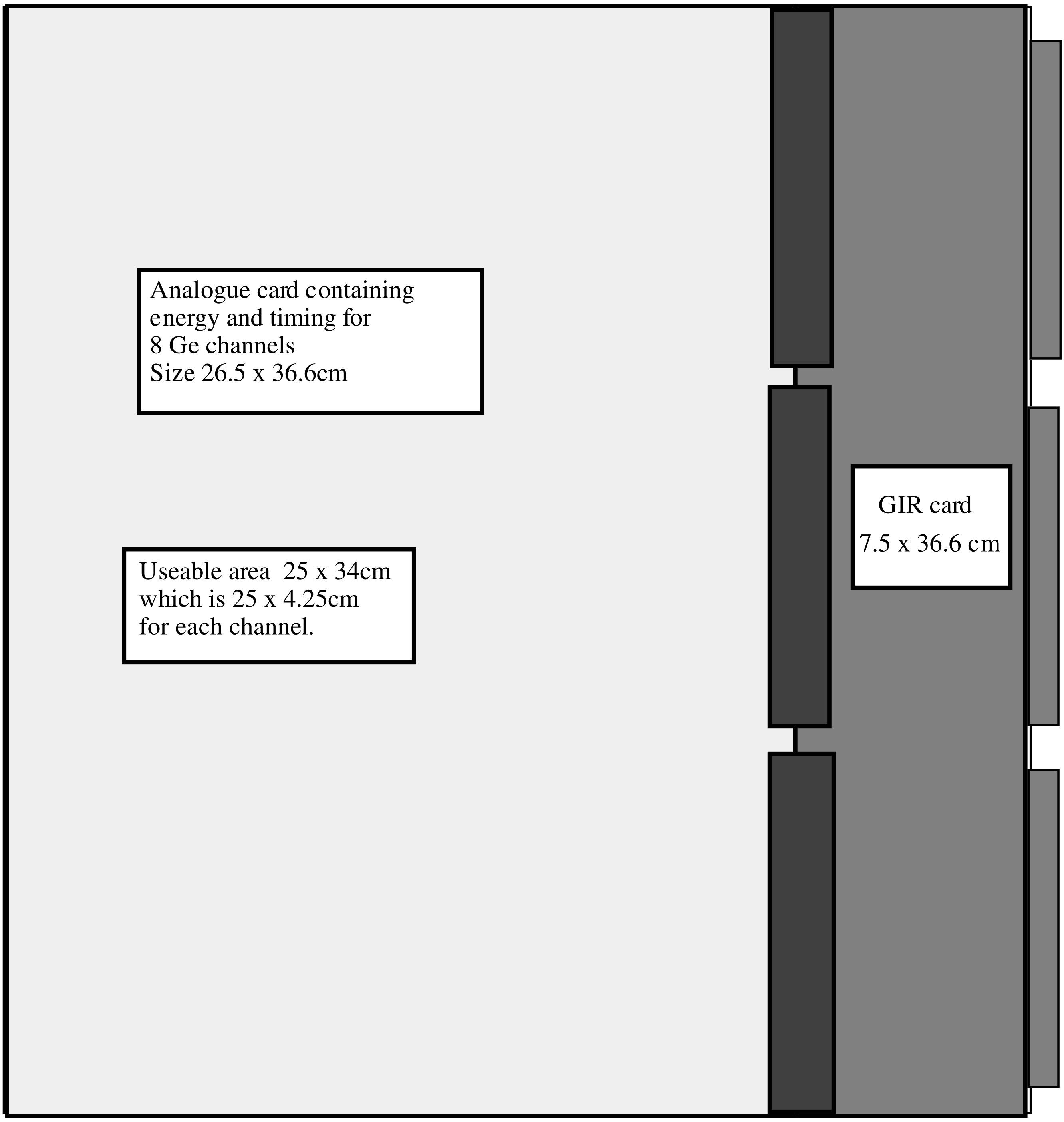

Fig 1. Layout of Euroball III Analogue Ge Cluster VXI card First version monolithic, later cards use GIR as shown

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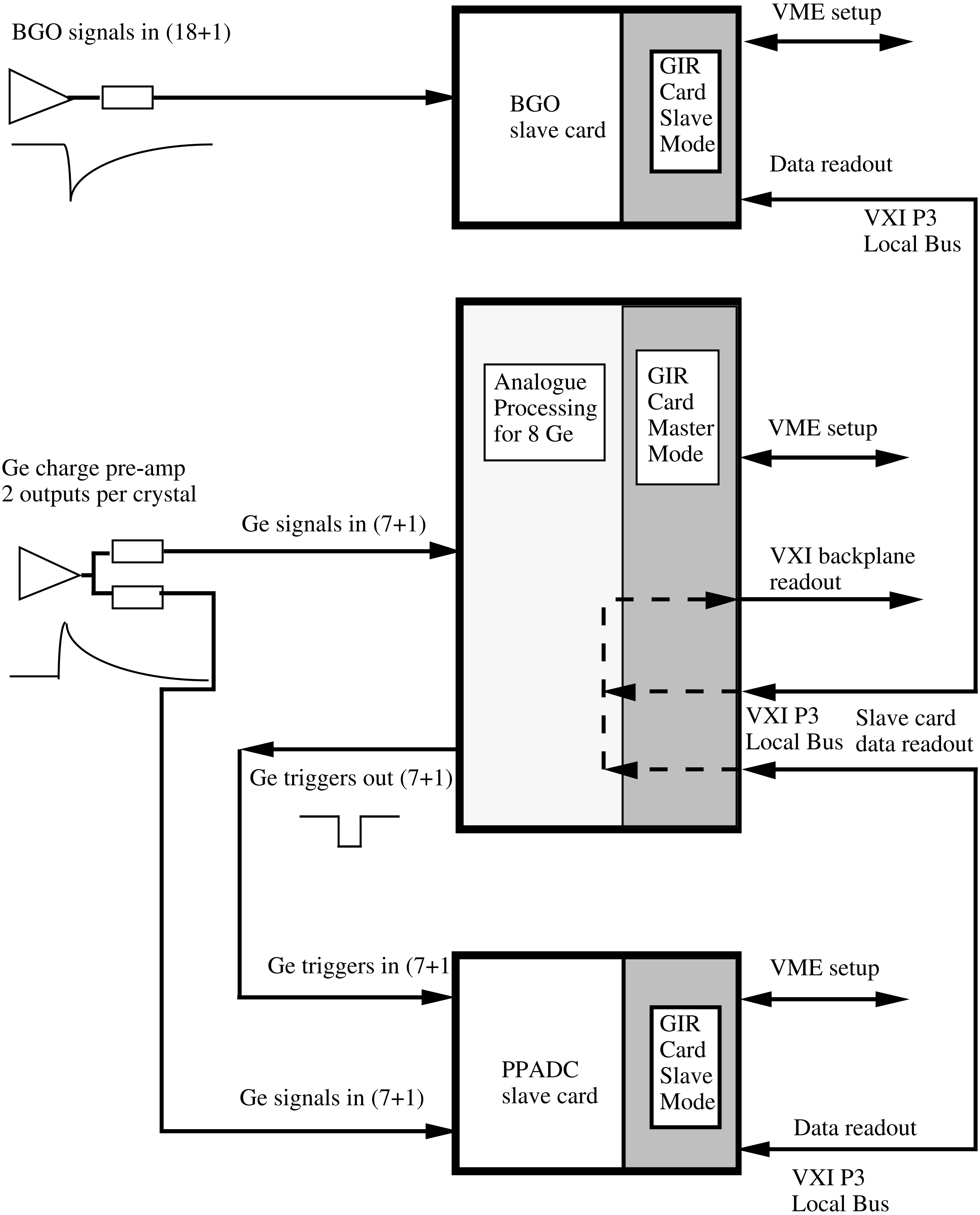

Fig 2. Schematic signal and data flow between VXI cards Shows the GIR cards in Master or Slave mode. (GIR cards can also be set to be all Masters so that each of the 3 cards is independent for readout.)

Ge Signal Processing

Input:

+100mV/MeV (±10%) pre-amp signal with 50Ω pre-amp output impedance.
50μs fall time constant (+/- 5%, limited by PZ adjustment range)
1K input impedance (approx.)
Pre-amp must supply 2 charge outputs; 1 for analogue card and 1 for PPADC
(NB change to pre-amp gain and polarity requested by detector group.)

Analogue Signal Shaping:

Unipolar output from 8th order quasi-trapezoidal filter.
Peaking time of 3μs .
Top is flat to within 0.xx% over a range of 1μs.
Pulse width at 0.1% is 10μs.
Output amplifier stage generates 4MeV and 20MeV ranges.
Incorporates TFA (see Timing section for details)

PPADC Signal Shaping:

Programmable.
Moving window deconvolution yields an exact trapezoidal shape.

Timing:

CFD: min threshold 10 keV, max. threshold 700keV
pulse pair resolution 500(?) ns
fraction 0.3, delay 50ns
TFA with 20ns integration and 180ns differentiation.
Gain switchable from software x3 or x1
TAC 0-2μs. (250ps resolution)

Outputs for coding:

4 MeV energy signal
20 MeV energy signal
TAC measuring from this crystal's CFD to Fast Trigger global reference pulse.
The user can turn on or off readout of each parameter independently under software control.

ADC:

13 bits resolution (8k channels)
Sliding scale (10 bits)
Conversion time 4.5μs
DNL <1%
INL < 250ppm

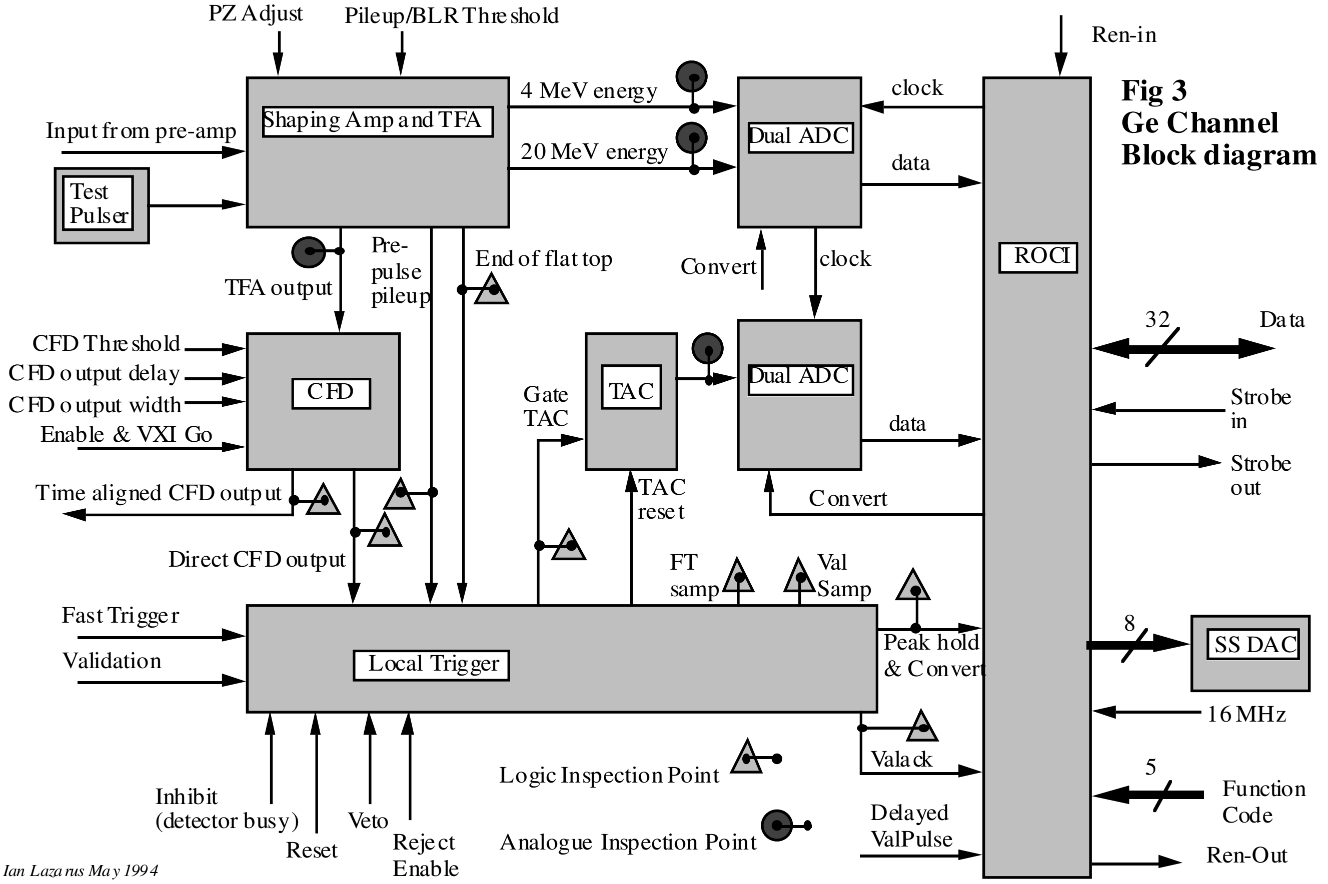

Fig 3
Ge Channel
Block diagram

<u>Analogue Inspection Lines:</u>
4 MeV energy
20 MeV energy
Bipolar signal for peak timing
TFA output
TAC output
LT fast ramp (FT)
LT slow ramp (Validation)
Pre-amp signal (after 1st buffer)

<u>Logic Inspection Line signals</u>

CFD delayed	(x8)
CFD direct	(x8)
End of flat top	(x8)
LT reset Output	(x8)
FT sample	(x8)
Val sample	(x8)
Convert	(x8)
TAC reset (start)	(x8)
Valack	(x8)
Pre-pulse pileup mono	(x8)
ADC Clock	(x8)
UP4 data stream	(x8)
FT pulse	(x1)
Val pulse	(x1)
SAROC out ready	(x2)
SAROC out ack.	(x1)
SAROC 1st Ren-in	(x1)
SAROC 2nd Ren-out	(x1)
Start readout (TFR)	(x1)
OR of 8 CFDs	(x1)
Card busy (local inhibit)	(x1)
Veto	(x1)
LT reset Input	(x1)
Conversion dead time	(x1)
Ren-in (inside buffer)	(x1)
Pass (inside buffer)	(x1)
BLTACK (inside buffer)	(x1)
DTACK (inside buffer)	(x1)
FIFO DTACK	(x1)
FIFO Empty (AND of both)	(x1)
FIFO ReadEnable	(x1)
FIFO Write Enable	(x1)
Readout Event No. Match	(x1)
Event Counter Fault	(x1)
No readout match in last 16	(x1)
Readout complete (reset)	(x1)

<u>Voltage Inspection Lines</u>
All DACs in channel (*CFD threshold, CFD delay, FT sample, Val sample, PZ, Pileup/BLR threshold, LT watchdog, crossover/Peak detect DAC*) Global DACs (*CFD width, test pulser*), DAC reference(s), DC Voltages

BGO Signal Processing:

Input:

From BGO pre-amp. Negative signal with no shaping (T_r=50ns T_f=330ns)
Signal level - 250mV/MeV

Signal Shaping:

Gated integrator.
Peaking time 1 µs
Top is flat to within 0.xx % over a range of xx µs.
Pulse width at 0.1% is xx µs.
Output 20MeV full scale

Timing:

First photoelectron with validation on 2nd electron
TAC range 2µs, resolution 5ns.

Outputs for coding:

20 MeV Energy signal
TAC measuring channel firing time before reference pulse (disc. to FT)
Also the hit pattern from BGO
A sum energy (20MeV full scale) from all inputs
A TAC measuring from first BGO input to a reference pulse (Fast Trigger)

ADC:

13 bits resolution (8k channels)
Sliding scale (8 bits)
Conversion time 4.5µs
DNL <1%
INL < 250ppm

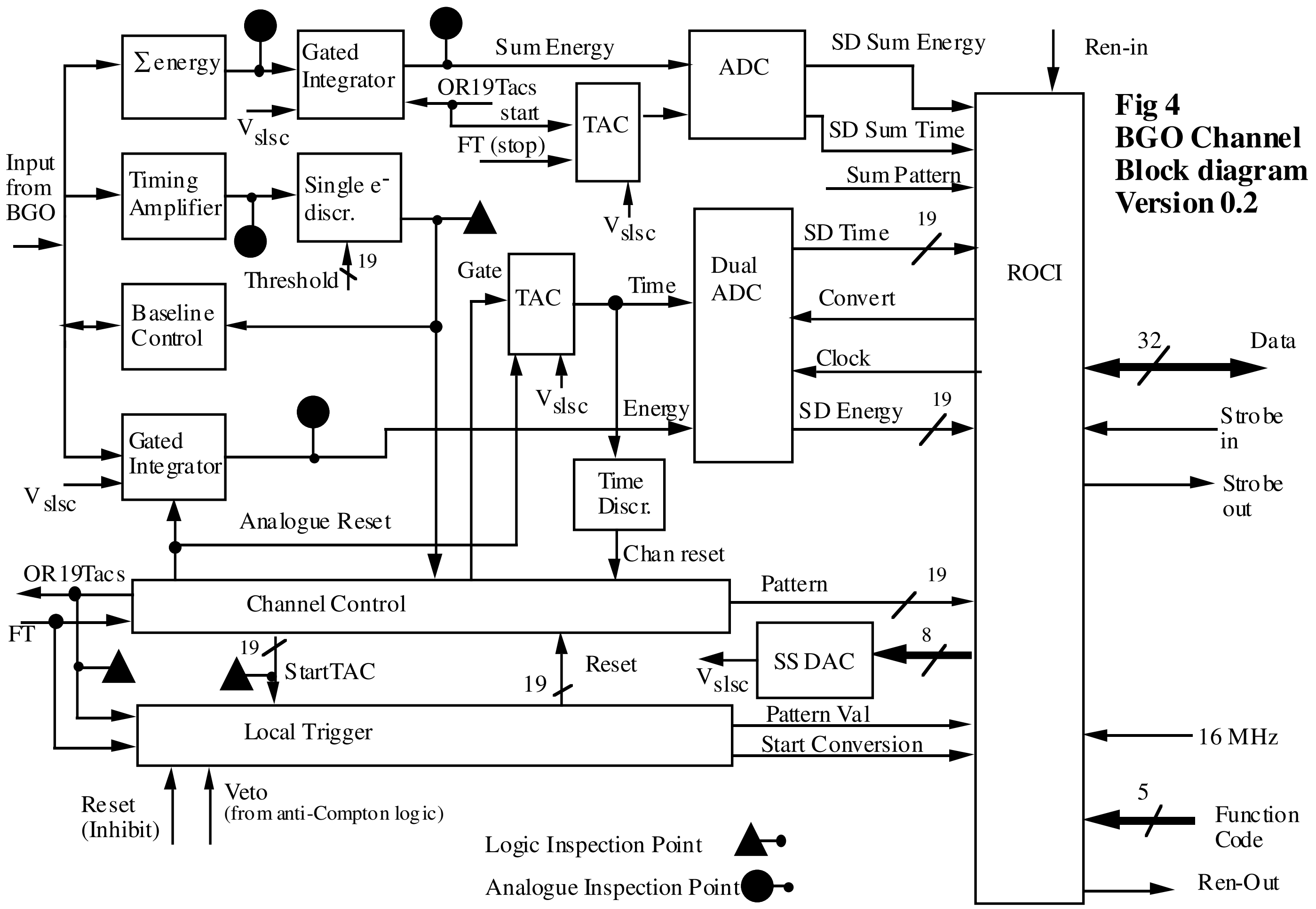

Fig 4
BGO Channel Block diagram
Version 0.2

Analogue Inspection Lines:

Timing Amplifier Output	(x19)
Gated Integrator Output	(x19)
Sum energy before Gated Int.	(x1)
Sum energy Gated Int. Output	(x1)

Logic Inspection Line signals

Single e- Discriminator	(x19)
OR19Tacs (First BGO)	(x1)
Fast Trigger	(x1)
Validation	(x1)
SAROC Ren-in	(x1)
SAROC ren-out	(x1)
Start Conversion	(x1)
Start TAC	(x19)
Fast Trigger	(x1)
ADC dead time monostable	(x1)
Local Trigger reset/inhibit	(x1)
Clock pattern into SAROC	(x1)

Logic Inspection Line signals(contd.)

Valack	(x1)
FT Sample	(x1)
Val Sample	(x1)

Voltage Inspection Lines

+2.5V ref	(x1)
Single e- Discr. Threshold	(x19)
Sliding Scale Voltage	(x3)

Cluster Detector Card Interconnections

* Front panel sumbusses will be introduced instead of the noise prone VXI sumbusses used in Euroball I and II. 3 sumbusses will be provided (Raw Ge, Clean Ge and BGO) each using 2 Lemo 00 connectors, 6 in total.

* 2 identical Ge signals (charge outputs) will be taken from each pre-amp. One will come in to a BNC socket on the analogue card and the other to a BNC socket on the PPADC card.

* 8 Trigger signals will be sent from the Ge local triggers (or CFDs?) to the PPADC card, via 8 Lemo 00 outputs from the analogue Ge card front panel.

* BGO signals will enter the BGO card via Lemo 00 inputs.

* Rate monitoring outputs (for Ge) to VME scalers will be provided from the front panel for compatibility with the other VXI detector electronics carried over from Euroball I and II.

* A veto signal for anti-Compton logic will pass from the analogue BGO to the analogue Ge card via the front panel using a Lemo 00 connector and a fast NIM logic signal This signal will be the logical OR of all the BGO discriminators, stretched into a 1µs wide pulse.

* VXI line usage will be fully compatible with Euroball I and II and Heidelberg/GSI Crystal Ball.

* The GIR cards will be capable of reading out some (or all) data from Slave mode cards to Master mode cards via the spare P3 LBUS lines. (Allows all data to go to one point for DSP manipulation.) Slave cards will also be able to do VXI backplane readout.

* The GIR cards will be capable of reading out independently as Master mode cards.

This large number of connections makes front panel design very difficult. Several options were tried, initially including the original method of taking a single Ge pre-amp signal to the analogue Ge card and then buffering this to the PPADC card. This was discarded on the grounds that it causes un-necessary congestion on the front panel of the Ge analogue card making front panel layout difficult and precluding the small adjustments of front panel layout necessary at the PCB placement/routing stage to obtain a PCB design which is not noise prone. The second pre-amp output is normally cabled to the instrumentation area anyway, so it makes sense to connect it to the PPADC card.

Fig 5 shows the front panel layout proposed for the analogue Ge cards. A similar layout (without the sumbusses and the rate monitoring) could be used on the PPADC card.

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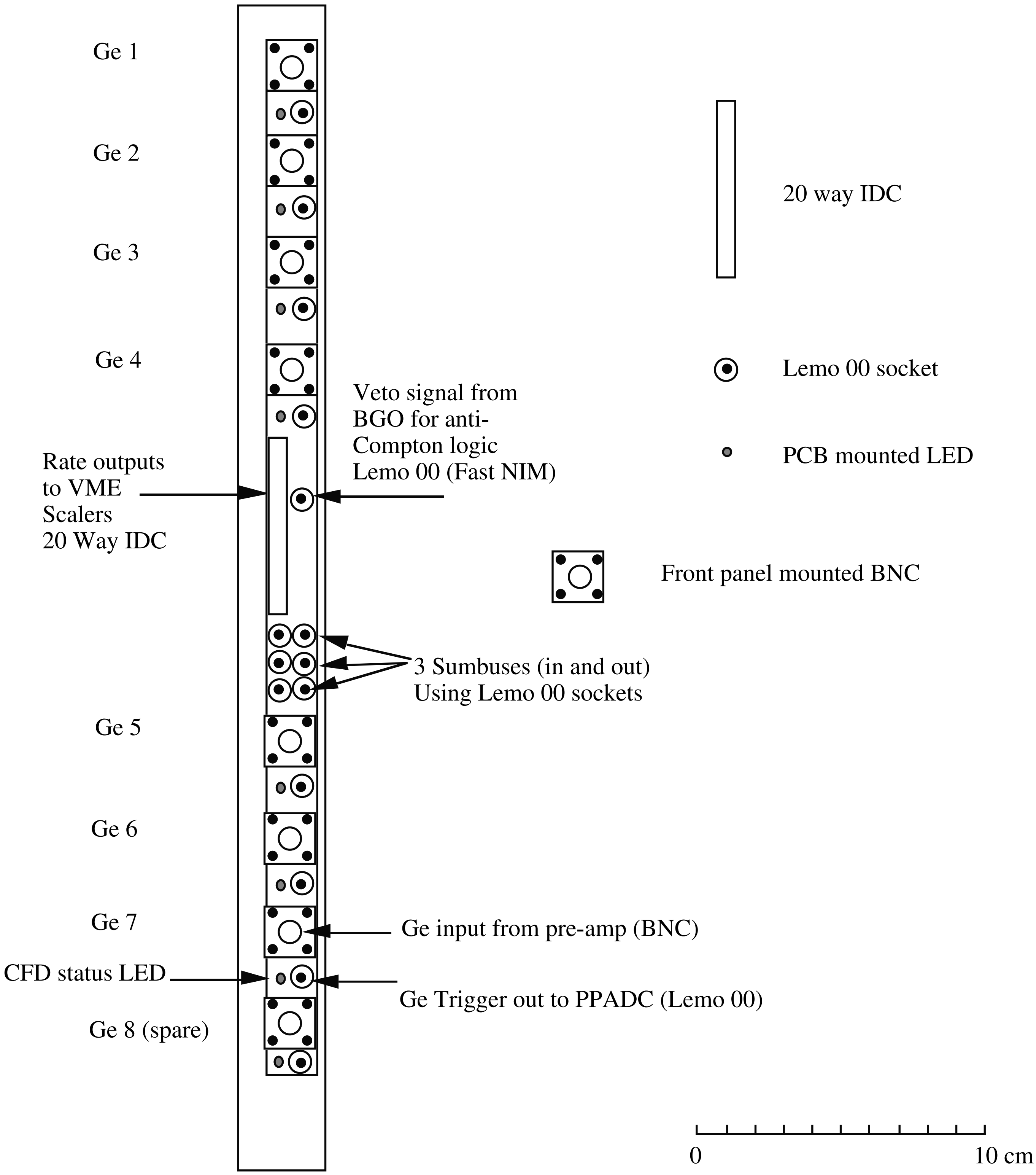

Fig 5 Front panel layout showing 8 Ge channels with Status LEDs + 3 sumbuses and external rate monitoring. (Drawn to scale)

Triggering and control

The trigger system will be the Euroball system, defined by Ender and Lazarus in 1989/90, as used in Euroball I and II and in the Crystal Ball VXI system. This comprises a 1st level trigger called a Fast Trigger which is usually generated on the basis of multiplicity information, and a 2nd level trigger called a Validation which is generated up to 10µs after the Fast Trigger. The Validation makes decisions using information not available immediately, for example from a downstream particle detector or recoil separator.

Each channel of Ge electronics has its own "local trigger" which samples the Fast Trigger and the Validation at a fixed (but programmable) time after that channel's discriminator has fired to check whether the system has chosen to accept the event it is processing. The BGO will have a single local trigger operating on all channels. The local trigger is inhibited during the times when the channel should not generate data which are:

1) While there is a previous event being processed by this cluster card (locally inhibited)
2) During the inter-event gap necessary to uniquely identify events (global inhibit)
3) When the readout system is blocked by a full FIFO or buffer (global inhibit)
4) When the user has paused operation by asserting the Inhibit Request line.

The local trigger performs the following jobs:

1) Initiates ADC conversion to synchronise with shaping amplifier's peak value
2) Detects and indicates pileup either from a preceding or succeeding pulse.
3) Starts and stops the channel's TAC.
4) Samples the Fast Trigger and Validations at programmed times.

Singles and local histogramming

Local singles histogramming was proposed as a later GIR upgrade. If implemented this will be true singles (without trigger bias), not the pseudo-singles based on multi-parameter event data which can already be collected using Eurogam VME histogrammers on DT32bus. There will be no local histogramming on the monolithic cards or the early version of the GIR.

Rate monitoring

Ge rate monitoring will be provided by external VME scalers. This system is carried over from Euroball I and II, and counts pulses from front panel outputs from Ge, Clover or Cluster VXI cards. Each time the channel's CFD fires, a pulse is sent to the scaler. The CFD can only be disabled by the VXI stop/go line, or the channel's disable bit. The local and global inhibits do not affect the firing of the CFD, so the scalers will always count all the pulses generated by a live channel without trigger bias.

Multiplicity:

All 3 multiplicities (Raw Ge, Clean Ge and BGO) will be distributed over the front panel via Lemo 00 sockets (looping in and out of each card) connecting a current summing bus. Each gamma ray detected causes a current contribution of 4mA.

The cluster card will produce a raw Ge multiplicity of 1 when one or more Ge crystals is hit. The multiplicity is a measure of the number of incident gamma rays, not of the number of times those gamma rays scattered (Euroball is an escape suppressed detector).

The Clean Ge multiplicity will produce a multiplicity of 1 when any of the 7 Ge crystals is hit, is not indicating pile-up and none of the BGO crystals is hit.

Additionally the Ge Raw and Clean sumbusses can indicate multiplicity 1 to 7 depending on the number of Ge crystals that are hit using a second set of sumbus outputs on the front panel of the analogue Ge card (or possibly the same outputs under the control of a jumper on the PCB. TBD). This allows the option of more esoteric triggers, and makes the cluster card useful as a more general purpose Ge detector card, albeit with one readout path shared between all 8 channels.

The BGO card's multiplicity output will indicate 1 gamma ray per crystal firing since the BGO crystals will stop a scattered gamma ray rather than scattering it again, so in theory it could indicate multiplicity of between 1 and 19 (4 mA per channel, so 4 to 76mA).

Anti-Compton Logic:

The inclusion of hardware anti-Compton logic is necessary. To omit it has repercussions for other parts of the system: 1) more processing power and/or time is required in the event builder to perform anti-Compton logic, 2) readout bandwidth requirements are doubled (anti-Compton rejection in hardware will remove typically 50% of data before readout).

Earlier versions of this specification included a complex method of hardware pattern matching for generation of clean multiplicity which checked for scattering from Ge to Ge as well as from Ge to BGO. It also allowed the use of different parts of the BGO shield for different Ge crystals. This scheme will not be included because it will not fit in the space available on the cards. Instead these complex suppression modes can be performed in the GIR card using its DSP (in later versions of the GIR only). The GIR will prevent readout of events for which it detects patterns of Ge and BGO crystals which indicate Compton scattering.

However, hardware anti-Compton logic will be provided in a very simple form where a Ge crystal is suppressed by the whole BGO shield *(should this include the back catchers too?)* using and OR function of all the BGO crystals and applying this BGO OR (BGO Veto) to the veto input of every Ge local trigger. The effect of the local trigger's veto input is to either mark or reject the channel (under software control) and always to gate off the Clean Ge sumbus.

The BGO Veto pulse width will be fixed at 1000ns.

Signals and levels

For every signal between the 3 VXI cards (and within a card to/from the GIR where it is used) it is necessary to define the following details:

a) signal name
b) electrical level (TTL, ECL, NIM, analogue...)
c) protocol and active level
d) whether unidirectional or bi-directional
e) connector type and mechanical details.

1) In the GIR specification (N.Karkour and D.Linget, CSNSM Orsay) the following interfaces are defined:

- VXI P1, P2, P3 to GIR (mainly in P2 rows a and c and P3; assume the rest is VME64 standard)
- Between GIR card and analogue Ge card.
- Between GIR card and BGO card.
- Between GIR card and PPADC.
- Between GIR Master and GIR Slave.

2) Between Analogue Ge card and PPADC card: there are 8 signals (apart from through GIR):

- Name: CFDnOUT (where n is 1 to 8 for the 8 Ge channels)
- Level: Fast NIM
- Active Level: Current flowing.
- Pulse width will be as programmed for CFD delay, typ 50ns.
- Unidirectional (Analogue Ge to PPADC)
- Connector type: Lemo 00

3) Between Analogue Ge card and BGO card: there is 1 signal (apart from through GIR):

- Name: Veto
- Level: Fast NIM
- Active Level: Current flowing
- Pulse Width: 1000ns
- Unidirectional: (BGO to Ge)
- Connector type: Lemo 00

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Functions of each sub-card.

The analogue Ge VXI module will contain 2 sub-cards, viz. the GIR and the analogue card. The PPADC module will contain 2 boards; one board with 8 PPADCs and the second a GIR card for set-up and readout. The BGO module will contain 19 BGO channel daughter boards plus one combined BGO channel all connected to a motherboard, and will connect to VXI via a GIR card.

GIR Card
- Interface to VXI bus as register slave.
- Perform card level readout using token passing 64 bit SSBLT transfers or Euroball I/II 32 bit token passing BLT transfers in each of 3 modes:
  a) Common Dead time: all cards dead (100% Eurogam compatible. For testing only)
  b) Parallel events where only active cards (detectors) are dead (Euroball),
  c) as b) but add simple 2 stage pipeline to allow new event during readout (Euroball).
- Allow data monitoring (and manipulation? or modification?) using on board DSP.
- Drive and receive all VXI lines as defined for Euroball I and II (AInsp, VInsp, Val etc.)
- Operate (selected by software) as either Master or Slave to allow either independent readout of all the 3 VXI cards, or one Master GIR with DSP to receive and process data from 2 Slave GIR cards (for example preventing readout for events which show evidence of Compton scattering).

Ge motherboard Card
- Receive inputs from 8 Ge pre-amps.
- Process and code the energy and timing information from these inputs.
- The ADC serial output stream will be converted to parallel data and corrected for Sliding Scale (using Euroball 12 channel SAROCs) before being transferred to the GIR card.
- DACs for control of CFD thresholds, local triggers etc. will be located within each of the 8 analogue channels.
- Rate monitoring scalers will be provided via front panel CFD outputs.
- Software selected anti-Compton logic using simple Veto input from OR of BGO channels.
- Raw and Clean Ge sumbus outputs will be generated.

PPADC Card
- House 8 complete PPADCs triggered by Lemo inputs from Ge analogue card's timing/trigger.
- Receive set-up signals from GIR card.
- Provide data in the same format as the SAROC in Ge card for readout via GIR card.

BGO Card
- Receive inputs from 18 BGO pre-amps.
- Process and code the energy and timing information from each of these inputs.
- Form a sum energy, pattern and earliest timing from the 18 BGO inputs
- Generate Veto output for Ge's anti-Compton logic using OR of all 19 channels.
- Receive set-up signals from GIR card.
- Provide data in the same format as the SAROC in Ge card for readout via GIR card.
- BGO sumbus output will be generated.

Readout

The VME64 SSBLT readout will improve the data rate over the Euroball I and II system but requires that the cluster cards be isolated in their own VXI crate with their own readout controller, the STR8080. So as to preserve existing investment, especially in small development systems, the readout will also operate in Euroball I and II mode. This means that the GIR cards are reprogrammed (XILINX FPGA and PAL change) so as to change the readout protocol. It is likely that the first "in system" tests will use this mode because the most likely array in which to perform the tests will be Euroball II. Crystal Ball investment is also preserved in that VME64 SSBLT readout can be used in Crystal Ball systems.

Whichever readout method is used, the data format provided by the GIR and STR8080 will be exactly compatible with the format used in Euroball I and II when the data reach the DT32 bus (this is a requirement of the data acquisition). This data format is as follows:

qual 1	qual 0	item (6 bits)	group (8 bits)	data (16 bits)

The Cluster electronics cards will all generate a 16 bit event number which will be incremented every time the Validation pulse is issued by the trigger, regardless of whether the card is actually participating in the event. The counter value is added to the event data along with a programmable 16 bit word containing the qualifier, item and group fields. This permits accurate event reconstruction. The counter's bottom 4 bits are checked each event against the 4 bit field issued by the trigger and any discrepancy reported by the GIR in the card's status register indicating either 1 count slip or a more serious > 1 count slip. In both cases the counter is resynchronised using the 4 bit count from the trigger (magnitude and direction of correcting counts is determined using a 4 bit difference calculation)

Euroball I and II also defines unique tokens for Start Event and end Sub-Event are respectively:

Start Event Token

1	1	item (=3f)	group (=ff)	data (16 bit Event Number)

End sub-event Token at the end of data from each ROCO, the last having item=3e (47)

Error 1	Error 0	item (= roco #)	group (=ff)	Word count (12 bit)	Ev No. (4 bits)

Other formats may be required later when a higher performance data acquisition system is used.

The STR8080 hardware is flexible in that it has a daughter board for the output data format, so that although the prototype uses differential VSB, the Euroball III system will initially use the DT32 bus exactly as implemented in Euroball I and II. This is essential since the first phase of the data acquisition is essentially a faster version of Euroball II. Later, when more exotic interconnection methods are used, the daughter boards can be changed to SCI, ATM etc. as required.

Software Interface

The Euroball I and II register group concept will be used so as to make the interface to the register server software as easy as possible. Essentially this means that each Ge or BGO channel is allocated its own sequential address space with the first space allocated for shared control bits and registers. The same map is used for all three card types.
The address offset map will look like this:

Address Space (offset into VXI address space)	**Name (Ge Analogue card)**
0x0000 to 0xffe	Common parameters
0x1000 to 0x10fe	Channel 1 Analogue Parameters (Ge A)
0x1100 to 0x11fe	Channel 2 Analogue Parameters (Ge B)
0x1200 to 0x12fe	Channel 3 Analogue Parameters (Ge C)
0x1300 to 0x13fe	Channel 4 Analogue Parameters (Ge D)
0x1400 to 0x14fe	Channel 5 Analogue Parameters (Ge E)
0x1500 to 0x15fe	Channel 6 Analogue Parameters (Ge F)
0x1600 to 0x16fe	Channel 7 Analogue Parameters (Ge G)
0x1700 to 0x17fe	Channel 8 Analogue Parameters (spare Ge)

Address Space (offset into VXI address space)	**Name (BGO)**
0x0000 to 0xffe	Common parameters
0x1000 to 0x10fe	BGO A parameters
0x1100 to 0x11fe	BGO B parameters
0x1200 to 0x12fe	BGO C parameters
0x1300 to 0x13fe	BGO D parameters
0x1400 to 0x14fe	BGO E parameters
0x1500 to 0x15fe	BGO F parameters
0x1600 to 0x16fe	BGO G parameters
0x1700 to 0x17fe	BGO H parameters
0x1800 to 0x18fe	BGO I parameters
0x1900 to 0x19fe	BGO J parameters
0x1a00 to 0x1afe	BGO K parameters
0x1b00 to 0x1bfe	BGO L parameters
0x1c00 to 0x1cfe	BGO M parameters
0x1d00 to 0x1dfe	BGO N parameters
0x1e00 to 0x1efe	BGO O parameters
0x1f00 to 0x1ffe	BGO P parameters
0x2000 to 0x20fe	BGO Q parameters
0x2100 to 0x21fe	BGO R parameters
0x2200 to 0x22fe	BGO Sum/pattern channel parameters

Address Space (offset into VXI address space)	Name (Ge PPADC card)
0x0000 to 0xffe	Common parameters
0x1000 to 0x10fe	PPADC Ge A parameters
0x1100 to 0x11fe	PPADC Ge B parameters
0x1200 to 0x12fe	PPADC Ge C parameters
0x1300 to 0x13fe	PPADC Ge D parameters
0x1400 to 0x14fe	PPADC Ge E parameters
0x1500 to 0x15fe	PPADC Ge F parameters
0x1600 to 0x16fe	PPADC Ge G parameters
0x1700 to 0x17fe	PPADC spare Ge parameters

The following tables show the address map for the Analogue Ge card in more detail.

The "real" VXI configuration registers will be contained in the GIR, but there will be an extra set of configuration registers for the analogue Ge, analogue BGO and PPADC cards which reflect the information about the analogue part so that revisions to the different parts of the module can be tracked separately, and potential incompatibilities detected from software. The Ge card will also use this PROM to hold the information about the configuration of the programmable output buffers in its serial DACs.

The analogue Ge card's **configuration registers** will be contained in a PROM as follows:

Address	Function
0 and 1	Manufacturer ID (16 bits)
2 and 3	Model Code (16 bits)
4 to 7	Not yet allocated
8 and 9	Serial Number (16 bits)
a and b	Revision Level (16 bits)
c to e	Not yet allocated
10	Buffer Configuration for DAC 0 (analogue Ge only)
11	Buffer Configuration for DAC 1 (analogue Ge only)
12	Buffer Configuration for DAC 2 (analogue Ge only)
13	Buffer Configuration for DAC 3 (analogue Ge only)
14	Buffer Configuration for DAC 4 (analogue Ge only)
15	Buffer Configuration for DAC 5 (analogue Ge only)
16	Buffer Configuration for DAC 6 (analogue Ge only)
17	Buffer Configuration for DAC 7 (analogue Ge only)
18	Buffer Configuration for DAC 8 (analogue Ge only)

Ge Analogue card common area (0->0x0FFE)

Hex Address	**Register Group**	**Function**	**r/w access and size**
0x00	Common DACs	CFD Width	w only 16 bits
0x02		Test Generator Amplitude	w only 16 bits
0x10	Card Control Regs	Module Control Reg. (MCR)	r/w 16 bits
0x12		Item+Group+Quals for Event Number	r/w 16 bits
0x14		Event Number Counter	r/w 16 bits
0x20	Inspection Lines	Logic Insp. 1 Channel Select	r/w 16 bits
0x22		Logic Insp. 1 Signal Select	r/w 16 bits
0x24		Logic Insp. 2 Channel Select	r/w 16 bits
0x26		Logic Insp. 2 Signal Select	r/w 16 bits
0x28		Analogue Insp 1 Chan. Select	r/w 16 bits
0x2a		Analogue Insp 1 Signal Select	r/w 16 bits
0x2c		Analogue Insp 2 Chan Select	r/w 16 bits
0x2e		Analogue Insp 2 Signal Select	r/w 16 bits
0x30		Voltage Insp Chan Select	r/w 16 bits
0x32		Voltage Insp Signal Select	r/w 16 bits
0x40	FIFO Access	Test access to data FIFO	r/w 32 bits
0x60	DAC Buffer Control	OverRide DAC0 Buffer Setup	r/w 16 bits
0x62	(Over-ride (volatile))	OverRide DAC1 Buffer Setup	r/w 16 bits
0x64		OverRide DAC2 Buffer Setup	r/w 16 bits
0x66	*DACs 0-1 shared by*	OverRide DAC3 Buffer Setup	r/w 16 bits
0x68	*Ge A and B etc.*	OverRide DAC4 Buffer Setup	r/w 16 bits
0x6a	*DAC8 is common*	OverRide DAC5 Buffer Setup	r/w 16 bits
0x6c		OverRide DAC6 Buffer Setup	r/w 16 bits
0x6e		OverRide DAC7 Buffer Setup	r/w 16 bits
0x70		OverRide DAC8 Buffer Setup	r/w 16 bits
0x80	DAC Buffer Control	DAC0 Buffer Setup	r only 16 bits
0x82	(from PROM)	DAC1 Buffer Setup	r only 16 bits
0x84		DAC2 Buffer Setup	r only 16 bits
0x86	*DACs 0-1 shared by*	DAC3 Buffer Setup	r only 16 bits
0x88	*Ge Aand B etc.*	DAC4 Buffer Setup	r only 16 bits
0x8a	*DAC8 is common*	DAC5 Buffer Setup	r only 16 bits
0x8c		DAC6 Buffer Setup	r only 16 bits
0x8e		DAC7 Buffer Setup	r only 16 bits
0x90		DAC8 Buffer Setup	r only 16 bits
0x100 to 17e	SAROC Addresses	SAROC 1 (Ge A to D)	r/w 32 bits
0x180 to 1fe		SAROC 2 (Ge E to H)	r/w 32 bits

Registers of which there are one per card

The **Module Control Register** contains the following bits:

Bit number	Meaning when = 0	Meaning when = 1
0	Mark Pileup & Veto Events	Reject Pileup & Veto Events
1	TFA gain setting x1	TFA gain setting x3
2	Sliding Scale Counter Off	Sliding Scale Counter On
3	If SS off, force SS DAC to 0V	If SS off, force SS DAC to 9V
4	*not allocated*	*not allocated*
5	Pipeline off **(must be off if bit 7=0)**	Pipeline on if parallel readout *(dead until data are in FIFO)*
6	Event Number Readout on	Event Number Readout off
7	Common Deadtime Readout	Parallel Readout
8	No action	Reset FIFO
9	Not Last Card	Last Card so use terminators
10	Controle des fenetres off	Controle des fenetres on
11	Event Number Q set by 0x12	Use real Event Number Q
12	Status: No fault	Status: Event fault 0
13	Status: No fault	Status: Event fault 1
14	Status: No fault	Status: Event fault 2
15	Status: FIFO empty	Status: FIFO not empty

The **Analogue, Logic and Voltage Inspection line Channel Select Registers** look like this:

Value	Channel Selected
0	Inspection Line Disconnected
1	Ge A
2	Ge B
3	Ge C
4	Ge D
5	Ge E
6	Ge F
7	Ge G
8	Ge spare channel
9	Common signals / GIR
10 to 255	Inspection Line Disconnected

The **Logic Inspection Line Signal Selection Registers** look like this:

Value	Signal Selected
1	End of Flat Top from shaping amplifier
2	LT reset output
3	FT sample
4	Val sample
5	4 MeV serial data out of ADC
6	TAC Reset (Start TAC)
7	Valack
8	Pre-pulse Pileup Indicator
9	Convert input to ADC
10	ADC Clock
11	CFD Direct
12	CFD Delayed
13-32	*Not used (LI lines disconnected if these select codes used)*
33	Fast Trigger Pulse
34	Validation Pulse
35	SAROC 1 Data Available
36	SAROC 2 Data Available
37	SAROC DTACK
38	RenIn to SAROC 1
39	RenOut from SAROC2
40	Transfer A to B in SAROC
41	OR of all 8 CFD Delayed outputs
42	Card Deadtime Signal
43	BGO Veto
44	Reset Local Triggers
45	Conversion Deadtime
46-48	*Not used (LI lines disconnected if these select codes used)*
49	RenIn from VXI
50	RenOut to VXI
51	FIFO DTACK
52	Bus DTACK
53	BLTACK
54	FIFOEMPTY
55	Read FIFO
56	Write FIFO
57	Readout Event Fault
58	Readout Event No. Match
59	No readout match in last 16
60	Reset from Readout Logic
61 to 65535	*Not used (LI lines disconnected if these select codes used)*

Codes 1 to 12 refer to channels 1 to 8 only.
Codes 33 to 60 refer to channel 9 (common/GIR) only.

The **Analogue Inspection Line Signal Selection Registers** look like this:

Value	Signal Selected
0	4 MeV energy
1	20 MeV energy
2	Bipolar signal for peak timing
3	TFA output
4	TAC output
5	LT fast ramp (FT)
6	LT slow ramp (Validation)
7	Pre-amp signal (after 1st buffer)
all others	*Not used (AI lines disconnected if these select codes used)*

The **Voltage Inspection Line Signal Selection Register** looks like this:

Value	Signal Selected
0	CFD Threshold
1	CFD Output Delay
2	PZ Adjustment
3	FT Sample Threshold
4	Validation Sample Threshold
5	Watchdog Timer Threshold
6	Pileup Threshold
7	Bipolar Crossover Threshold
8 to 15	*Not used (VI line disconnected if these select codes used)*
16	Vee24
17	Vee18
18	Vee12
19	Vee5.2
20	Vee5Analogue
21	Vee2
22	Ground
23	Vcc5Analogue
24	Vcc5
25	Vcc12
26	Vcc18
27	Vcc20
28	Vcc24
29	Test Generator Level
30	CFD Width
31	Ground
32 to 65535	*Not used (VI line disconnected if these select codes used)*

Registers Per Channel

Each Ge Channel area (eg 0x1000 -> 0x17FE for Ge A) contains 1 register, the Channel Control Register (CCR) and 8 DACS. The channel is addressed as follows:

Hex Address	**Register Group**	**Function**	**r/w access and size**
0x00	Channel A	CFD Threshold DAC (8 bit)	w only 16 bits
0x02		CFD OutputDelay DAC (8 bit)	w only 16 bits
0x04		PZ Adjust DAC (8 bit)	w only 16 bits
0x06		FT Sample DAC (8 bit)	w only 16 bits
0x08		Val Sample DAC (8 bit)	w only 16 bits
0x0a		LT Watchdog DAC (8 bit)	w only 16 bits
0x0c		Pileup Threshold DAC (8 bit)	w only 16 bits
0x0e		Bipolar Crossover DAC (8 bit)	w only 16 bits
0x10		Channel Control Reg	r/w 16 bits

The **Channel Control Registers** contain the following bits:

Bit number	Meaning when = 0	Meaning when = 1
0	Disable Channel	Enable Channel if VXIGO=1
1	Test Generator Disabled	Test Generator Enabled
2	*Not yet allocated*	*Not yet allocated*
3	*Not yet allocated*	*Not yet allocated*
4	*Not yet allocated*	*Not yet allocated*
5	*Not yet allocated*	*Not yet allocated*
6	*Not yet allocated*	*Not yet allocated*
7	*Not yet allocated*	*Not yet allocated*
8	*Not yet allocated*	*Not yet allocated*
9	*Not yet allocated*	*Not yet allocated*
10	*Not yet allocated*	*Not yet allocated*
11	*Not yet allocated*	*Not yet allocated*
12	*Not yet allocated*	*Not yet allocated*
13	*Not yet allocated*	*Not yet allocated*
14	*Not yet allocated*	*Not yet allocated*
15	*Not yet allocated*	*Not yet allocated*

Notes about changes in draft 2.1

The following pages have been re-written:

- Page 1 (introduction)
- Page 4 (NB TFA gain is now switcheable again)
- Pages 4 and 6 (footnotes referring to earlier versions have been removed)
- Page 5 (Logic inspection lines no longer synch/normal: all are available on both lines. Also, some of the VME and readout LI lines have been added, and the LT watchdog removed since it can be indirectly observed using the LT reset output.)
- Page 8 (Rate monitoring section updated)
- Page 10 (added reference to the BGO's local trigger)
- Page 11 (added note about BGO card's sumbus multiplicity output)
- Page 13 (functional descriptions of the cards updated)
- Page 14 (section on local event number counter added)
- Pages 17 and 18 added with details of Ge software interface

Notes about changes in draft 2.2

- Page 5 (Inspection Lines corrected)
- Page 6 (Sliding scale 8 bits, not 10 bits.)
- Page 15 (Address map separated into 3 parts for 3 cards)
- Page 18 (MCR extra bits 5-15 defined)
- Pages 19 and 20 (Inspection line information added)

Notes about changes in draft 2.2.1

- Page 19 Logic Inspection Line mapping corrected.

Notes about changes in draft 2.2.2

- Page 19 Logic Inspection Line mapping corrected again (code 32 not used, start from 33).

Notes about changes in draft 2.2.3

- Page 18 Module Control Register updated.