The Software Interface for the DT32-VME Buffer

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This document should be read in conjunction with EDOC075 (DT32-bus specification, J.R.Alexander) available from the EUROGAM document server on nnsa at Daresbury, and the 'DT32 to VME/VSB Buffer proposal Version 1.1' by P.J.Coleman-Smith and V.F.E.Pucknell.

VME specification

The card requires two regions of VME address space. One for the Registers and List RAM, A24/D32/D16, and the other for the Buffer RAM A32/D64/D32 MBLT. Except where specified all accesses to the registers are 16 bit only. The card is a VME Slave.
The buffer RAM supports 32 bit data accesses only. During 'Event storage' the Buffer is read only , and supports burst mode access.
The card is a type ROAK interupter. That is it removes the interrupt request during the acknowledge cycle.

VME accessible registers.

There follows a list of the registers on the card. The register base address is set in A24 address space using the jumpers provided on the card. Jumpers 11 -> 0 represent Address bits 23->12. If the jumper is in place then the relevant address bit must be a logic 0 for access to be enabled.

The registers occupy 4k bytes .

Card status register. **Register Base + 0**

Bit	Name	R/W	Function
0	List Ended	R/W	This indicates there is not another valid entry in the List RAM, and data storage has halted. This bit should be cleared by software.
1	MF has occurred	R/W	This indicates the memory full limit has been reached for a previous block. This bit should be cleared by software.
2	Block Change has occurred	R/W	This indicates when a block change has completed. This bit should be cleared by software.
3		R/W	
4	Event storage active	R	The event storage logic is active.
5	DTPASS	R	DT32 bus signal state.
6	DTREN	R	DT32 bus signal state.
7	DTPAUSE	R	DT32 bus signal state.
8	DTSTOP	R	DT32 bus signal state.
9	FIFO empty	R	OR of the FIFO empty flags.
10	FIFO full	R	OR of the FIFO full flags.

Card Control register. **Register Base + 2**

Bit	Bit Name	Function
8	Enable event storage.	When set event storage is started with the descriptor pointed to by the current setting of the List RAM address register. When cleared storage of the current event is completed, and then stopped. The current block entry in the List RAM is completed. The List RAM address register will contain the address of the next descriptor .
9	Software reset.	When set all registers are set to zero, the FIFO is reset. This bit should be cleared by software
10	FIFO reset.	The FIFO is reset. This bit should be cleared by software
11	Abort event storage.	Storage of data is stopped immediately. The current block entry in the List RAM is completed. The List RAM address register will contain the address of the next list entry .
12	Not used	Keep at logic zero.
13	A32 enable	This bit is set to enable access to the A32 address space of the buffer RAM. This bit should only be set after programming the Buffer Base Address Register (12)

Interrupt control register. Read/Write **Register Base + 6**

Bit	Name	Function
0	List ended Enable	Enable List Ended to cause an interrupt if Bit 7 is true
1	Memory Full Enable	Enable Memory Full to cause an interrupt if Bit 7 is true
2	Block Change Enable	Enable Block Change to cause an interrupt if Bit 7 is true
3	Not used	Keep at Zero.
4	Request Select 0	Select the interrupt request level used by this module
5	Request Select 1	
6	Request Select 2	
7	Enable	Enable the interrupts from this card.

Interrupt Vector. Read/Write **Register Base + 8**

Bit	Name	Function
0	Not used	The List ended status bit is used to create the vector.
1	Not used	The Memory Full status is used to create the vector
2	Not used	The Block Change status bit is used to create the vector.
8->3	Vector	These bits form the interrupt vector with the status bits.

Current List RAM address. Read Only ? **Register Base + 10**

10 bit register, bits 9 -> 0, containing the address used by the storage sequencer. It will be either pointing to the start of the next descriptor, or during event storage it will be pointing to the location in the current descriptor for the block status register to be written.

Buffer Base address. Read/Write **Register Base + 12**

The base address for the buffer RAM is loaded here by software. It forms the 16MS bits of the buffer RAM address when accessed from VME using A32. The A32 enable, Control register bit 5, must be set before access will work.

Current Buffer memory Read address. **Register Base + 16**
18 bit register containing the last address used by the VME access to the buffer RAM. This is Read only.

Current Buffer memory Write address. **Register Base + 20**
18 bit register containing the last address used by the DT32 bus storage control sequencer. This is Read only.

Read/Write FIFO (32 bit only) **Register Base + 24**
Single register provides access to the FIFO for test purposes. This must not be attempted when the 'Event Storage Active' status bit is set.

Read DT32 bus input. **Register Base + 28**
A read of this 32 bit register will return the state of the DT32 bus data lines when the last incoming WST occured. This must not be attempted when the 'Event Storage Active' status bit is set.

Write DT32 bus output. **Register Base + 32**
A write to this 32bit register will put the 32 bit data on the DT32 output, and strobe the WST line once. This must not be attempted when 'Event Storage Active' status bit is set.

Read/Write List RAM. **Register Base + 0x 800 to + 0xFFE**
Access is available at all times. Single 16 bit read and write cycles. If a change of block is in progress then the access will be delayed (DTACK* not sent) until it is completed.

Read/Write Buffer RAM. **Buffer Base to + 0xFFFFC.**
Access depends on the state of the module.
In Set up mode, after power up and when 'Event Storage Active' status bit is clear access is A32/D32 read/write.
In Event storage mode, 'Event Storage Active' status bit is set, access is restricted to read only. A32/D32, and A32/D32/D64 BLT. is available.

Modes of operation.

Overview

Set-up.
Access is enabled to all of the registers in the accessible registers list. There is no activity initiated by the storage control. No interrupts will occur.
This mode is entered after system, and soft reset.

Event storage.
This mode is entered by setting the 'Enable Event storage' bit in the card control register with valid descriptors in the List RAM. The storage control is active, DT32 events will be stored. Interrupts will occur as requested (interrupt enables) and in accordance with the rules stated for each one.
Access to the buffer RAM is restricted to read only. Access to the FIFO , and some registers may cause loss of data. See 'VME accessible registers'.

Co-processor.
This is when the links connecting the DT32 bus input to the FIFO are removed, and a co-processor board is attached. There is at present no plan for any communication between the two modules. The co-processor will be expected to emulate the DT32 bus. Thus no change to the method of use is required.

Operation

Initialisation

This is done in 'set-up' mode, and the following operations should be completed.

- Write the Buffer base address register.
- Write block descriptors to the LIST RAM, and set bit 15 of the final 'Next block descriptor start address' entry.
- Write the Interrupt vector.
- Enable the required Interrupts, and write the interrupt request level.
- Clear all other registers.
- Write the address of the start of the first block descriptor into the Current List RAM address register.
- Set the 'Enable Event storage' bit in the 'Card control' register. Wait for an interrupt, or poll the relevant bits in the 'Card status' register.

Event Storage

This occurs in the 'Event storage' mode. The DT32 bus is activated by setting the DTREN signal. Data is written into a FIFO using the DT32 bus WST signal. Data is read from the FIFO and written into the buffer RAM as it becomes available. Access to the Buffer RAM is shared between this writing from the FIFO, and block reads to the VME bus. This sharing is done as 1 read for 1 write cycle. This occurs transparently if both access types occur simultaneously.

Change of block

This occurs in Event storage mode when sufficient data has been stored from the DT32 bus for the buffer address counter to pass the HWM, and the current Event has ended.
The 'Card status' register is updated.
The 'Card status' register, and word count are written to the block descriptor in the List RAM.
Bit 15 of the 'Next block descriptor start address' entry is tested, if set then Event storage is halted, and the relevant bits set in the 'Card status' register. But if bit 15 is cleared the value is loaded into the List RAM address register, and the buffer address, HWM, and MF registers are loaded from the new block descriptor.
Then Event storage is resumed.

Interrupts

Interrupts occur when the relevant bit is set in the 'Card status' register, and its enable bit is set in the 'Interrupt control' register. Once an interrupt has been acknowledged then the card enable bit is cleared, and no more interrupts will occur until it is set.

RAM descriptions

Buffer RAM

This is a 512k x 32 bit SRAM module. It is only available for 32 bit accesses to and from the VME bus. There are 2 modes of operation. 'Set-up' and 'Event storage'. During 'Event storage' the buffer is read only to VME, and data is written from the DT32 bus. During 'Set-up' the buffer is read/write to and from the VME.

List Ram

This is a 1k x 16 bit SRAM, and contains one or more block descriptors of eight words. It is accessible at all times, but excessive accesses will slow the change between blocks. Each descriptor consists of eight 16 bit words. The first three are information about the memory block to use in the main store. The next two will be overwritten with information about the block as it is completed. The last location contains the address of the start of the next descriptor.

List RAM descriptor definitions.

0: Start Address. This 16 bit word is the most significant part of the 18 bit address of the start of the new block in the buffer RAM.
N.B. Start Address = VME Address >> 5.

1: High Water Mark (HWM) This is loaded into a down counter. One count is one 32 bit word. If the counter reaches zero the current event being stored is completed. That is the DT32 bus will not have another DTREN issued. Once the last word for the current event is stored , the word count, and status register are stored in the LIST RAM. (see later). At this time the 'change of block' occurs.

2: Memory Full limit (MF) This is loaded into a down counter. One count is one 32 bit word. If the counter reaches zero then the current DT32 event is aborted. The assumption is that the event is corrupted, it is longer than the difference between the MF and the HWM. The next block will not be started until the readout of the corrupt event is complete. This could lead to a hung system, but in any case something needs attention/re-boot !

3: Block status register. This is a copy of the Card status register written to this location at the end of the current block.

4: Word count. The number of words that have been stored in the buffer RAM for this block. (1 = a 32 bit word).

5: Next block descriptor address.
Bits 10 -> 0 The address of the next block descriptor in the List RAM.
Bit 15 Last descriptor flag. If this bit is set then this is the last descriptor in the current list. No further data storage will take place until a new list is create by software.

6 & 7: Unused These locations are not used by the module. They are implemented and could be used for inter processor communication in a multi-processor environment.