EUROGAM Phase 2 Clover Detector Card Specification

(This document will be updated later to describe the production cards exactly)

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Introduction

Each phase 2 Clover detector card will fully instrument one Clover Ge detector and its associated shield, including a spare Ge channel for each Clover.

The Clover card will be made from re-packaging parts of the phase 1 Ge card and the phase 1 BGO card into one new card. The card will operate in common deadtime like the phase 1 cards and provide data using the same trigger and readout system as is used in phase 1.

The inputs will be 4+1 spare Ge pre-amp signals and 8 BGO pre-amp signals (the Clover detector shield contains 16 BGO elements which are connected in pairs to 8 pre-amps). The signal processing elements will be the same as phase 1 viz.

* Ge Shaping Amplifier (4 hybrids)
* Timing Filter Amp (1 SMT card)
* CFD (1 SMT card)
* Dual Peak Detect and Hold (1 SMT card)
* Crossover Detector and buffers (1 SMT card)
* TAC (1 ASIC)
* ADC (1 SMT card)
* Sliding scale logic and DAC (2 SMT cards)
* ReadOutChIp (ROCI) (1 ASIC)
* Test Ge Tail Pulse Generator (1 SMT card)
* Test BGO Tail Pulse Generator (1 SMT card)
* Dual Line Receiver (1 SMT card)
* Summing/Shaping Amplifier (1 SMT card)
* BGO Pattern Unit (1 SMT card)

Obviously the performance of each of these analogue processing elements is now known and will be broadly similar in the Clover card to that seen now in Ge and BGO cards.

The spare Ge channel is available to facilitate re-cabling in the event of an electronics problem, and may be permanently configured in the Event Builder programs to be associated with its clover detector although it need not supply data unless required. There is no similar arrangement for BGO because there is not space for a full spare channel. The 2 unused inputs to the BGO channel are fanned in to common circuitry very early in the signal processing, and so there is no benefit in using these as spare inputs.

The control logic for each channel is presently performed in a Local Trigger card. This will be enhanced to allow more versatile operation of the Clover detectors, for example to distinguish between 1 or more Ge firing and exactly 1 Ge firing and to allow various anti-Compton options. Further details of the control logic/Local Trigger will be found later in the document.

The VXI interface exists in both XILINX LCA and Altera EPLD form on different phase 1 cards (the former on Ge and BGO cards, and the latter on Trigger, NAM and RM cards). The Altera version will be used because of easy access to development systems, the fact that the engineer doing the VXI interface has a lot of experience of Altera and the problems seen occasionally in Phase 1 where Xilinx chips have been vulnerable to power surges/spikes.

The software interface for the phase 1 Ge and BGO cards was designed to be as consistent as possible between the cards and this principle will be carried over to the Clover card which will use the same groups of registers and DACs as are now in the Ge and BGO cards.

Ge Signal Processing

Input:

200mV/MeV (±10%) pre-amp signal with 50Ω pre-amp output impedance.
50μs fall time constant (+/- 5%)
1K input impedance (approx)

Signal Shaping:

Unipolar output from 6th order quasi-triangular filter.
Peaking time of 4.4μs and FWHM 5 μs.
Pulse width at 0.1% is 11μs.
Output amplifier stage generates 4MeV and 20MeV ranges.
Bipolar (differentiated) outputs available for crossover timing.

Timing:

CFD: min threshold 30keV, pulse pair resolution 1μs
timing walk 3ns for 200:1 dynamic range, 25ns for 1000:1 (200ns Tr)
The CFD will be replaced by the smaller INDRA CFD with similar performance.
TFA with 50ns ***(??)*** integration and 180ns differentiation. Gain x3 or x10.
TAC 0-2μs, FWHM 0.6ns, INL <5%

Outputs for coding:

4 MeV unipolar signal
20 MeV unipolar signal
TAC measuring peaking time (CFD firing to bipolar crossover)
TAC measuring channel firing time before reference pulse (CFD to FT)

ADC:

13 bits resolution (8192 channels)
Sliding scale
Conversion time 4.5μs
DNL <1%
INL < 250ppm

BGO Signal Processing:

Input:

1000mV/MeV pre-amp signal with approx 5Ω pre-amp output impedance.
30ns rise time constant (+/- 10%)
10μs fall time constant (+/- 1.5%)
50Ω input impedance

Signal Shaping:

Bipolar output from 4th order semi-gaussian filter. (CR^2 RC^4, RC=2μs)
Peaking time of 5.2μs and FWHM 5.5 μs.
Pulse width at 0.1% is 12 x τ = 24μs.
Output 8 MeV full scale
Amplifier resolution is 3keV fwhm (3 channels in phase 1)

Outputs for coding:

8 MeV Energy signal
TAC measuring channel firing time before reference pulse (disc. to FT)
Also a serial bit stream indicating the hit pattern from BGO and Ge.

ADC:

13 bits resolution (8192 channels)
Sliding scale
Conversion time 4.5μs
DNL <1%
INL < 250ppm

Clover Detector Card Interconnections

* Primary interconnection mechanism is the VXI backplane as for phase 1.
* The front panel connections will be similar to phase 1, ie the Ge signals will come in via BNCs and the BGO via 20 way IDCs using similar LEMO-IDC cards to phase 1 but smaller to prevent mis-connection of phase 1 shields to phase 2 electronics and vice versa.
* There will be no external Veto inputs or outputs (no spare BGO channels to connect!)
* LEDs will be provided to indicate that BGO discriminators and Ge CFDs are firing as used in phase 1.
* Front panel rate monitoring CFD outputs (differential ECL) will be provided with the same 16 way IDC as for phase 1 Ge cards. If space permits the IDC size will be increased to monitor all BGO elements too (ie 13 outputs); if not, the signals will be 5xGe and an OR of all 8 BGO.
* Backplane sumbuses and all other VXI connections will be retained for full compatibility with phase 1. When the clover card is adjacent to phase 1 cards, the BGO local bus veto signals will be ignored and the Ge local bus Veto inputs will not be driven.
* There will be no external amplifier inputs.
* The Ge pre-amp inputs will use non-insulated BNC for better grounding and mounting.

Control Logic and Operating Modes for the Clover Detector

The control logic must provide signals for each channel of logic to control the PDS gate, the ADC coding, the start of readout. It must also check that the Fast Trigger and Validation inputs arrive at the correct time relative to the discriminator firing on that channel. This is the function of the phase 1 Local Trigger plus a small amount of external logic.

In the phase 2 Clover card, the local triggers will operate as they do in phase 1, but the external control logic will be changed and expanded to allow for the complex operational modes possible in a clover detector. Some probable modes of operation are described below:

Modes of operation:

1) Simple.
In this case, all 5 Ge inputs (4 'real' inputs + 1 spare) are treated as a single detector with a single BGO shield. When 1 or more Ge element fires, a multiplicity of 1 is indicated on the Raw Ge sumbus regardless of what happens in the BGO. The Clean Ge sumbus indicates a multiplicity of 1 if no element in the BGO shield has fired. If 1 or more BGO element does fire, then a multiplicity of 1 is indicated on the BGO sumbus and the Clean Ge sumbus current driver is inhibited.

2) Exactly One Ge.
In this case exactly 1 of the 5(4) Ge inputs must fire, with the other 4(3) Ge inputs being used with the whole BGO shield as anti-Compton vetos. The Raw Ge sumbus sees a multiplicity of 1 when 1 or more Ge elements fires (even though the 2nd Ge is part of the veto), but the Clean Ge sumbus indicates a multiplicity of 1 only if exactly 1 Ge has fired and no BGO element has fired. If 1 or more BGO element fires, then a multiplicity of 1 is indicated on the BGO sumbus and the Clean Ge sumbus current driver is inhibited.

3) Ignore Opposite Corner.
This mode is similar to the "Exactly One Ge" mode except that intelligence is applied to the processing of the BGO shield. The 4 BGO elements in the opposite corner are ignored, for example:

> Ge A is "clean" if there are no hits in any of the BGO pairs s1,s2,s3,s6,s7,s8 or Ge B-D.
> (ie BGO elements g, h, i and j in s4 and s5 are ignored.)

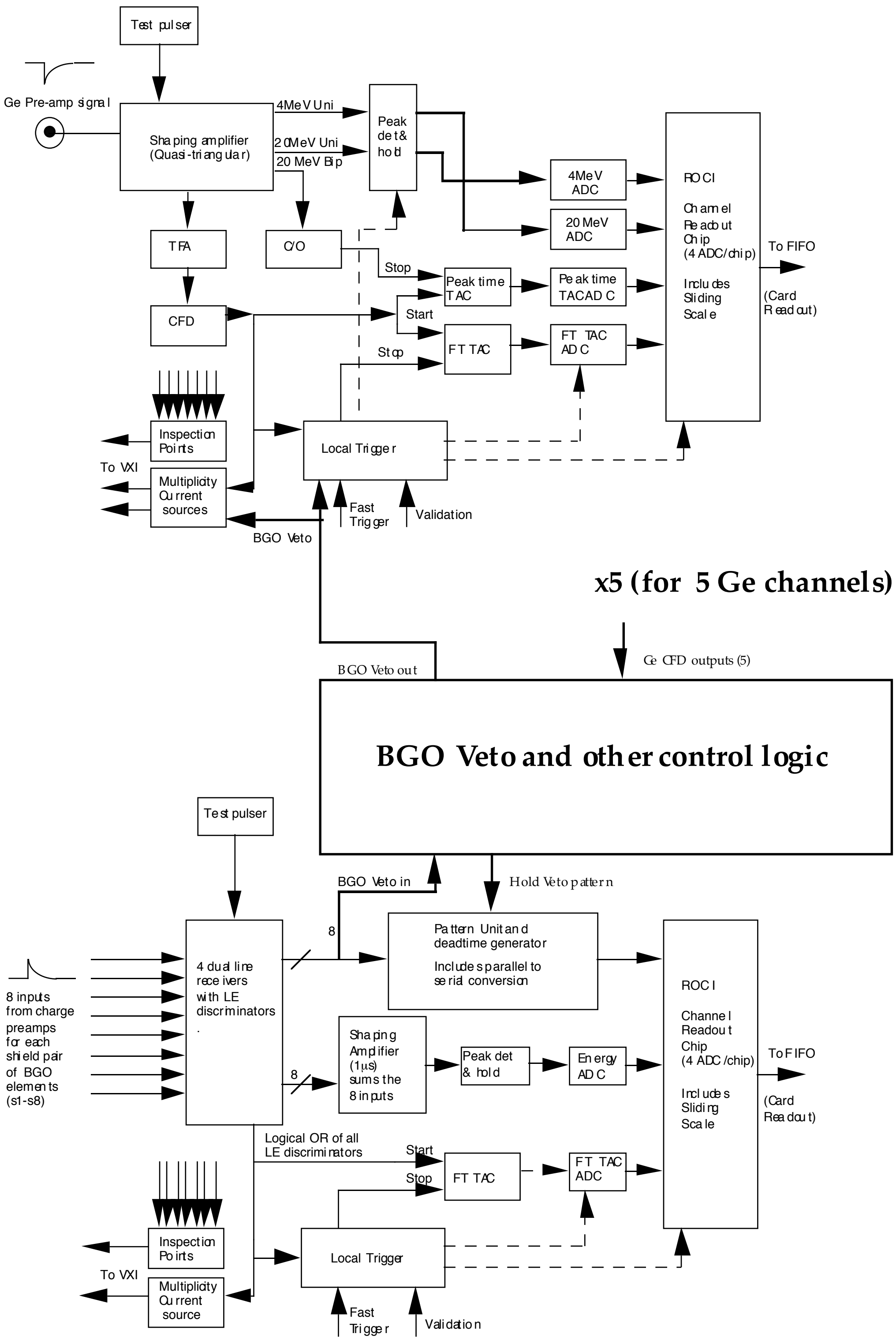
The Raw Ge sumbus sees a multiplicity of 1 when 1 or more Ge elements fires, but the Clean Ge sumbus indicates a multiplicity of 1 only if exactly 1 Ge has fired and there have been no BGO hits in the 12 relevant elements in the shield. If one or more BGO element (from the whole 16 element shield) fires, then a multiplicity of 1 is indicated on the BGO sumbus.

The following table summarises the 3 modes described here:

Mode	**Raw Ge $\Sigma=1$**	**Clean Ge $\Sigma=1$**	**BGO $\Sigma=1$**	**Anti-Compton**
Simple	≥ 1 Ge	≥ 1 Ge & not AC	≥ 1 BGO	16 BGO + 0 Ge
Exactly 1 Ge	≥ 1 Ge	= 1 Ge & not AC	≥ 1 BGO	16 BGO + 3 Ge
Ignore Opp Corner	≥ 1 Ge	= 1 Ge & not AC	≥ 1 BGO	12 BGO + 3 Ge

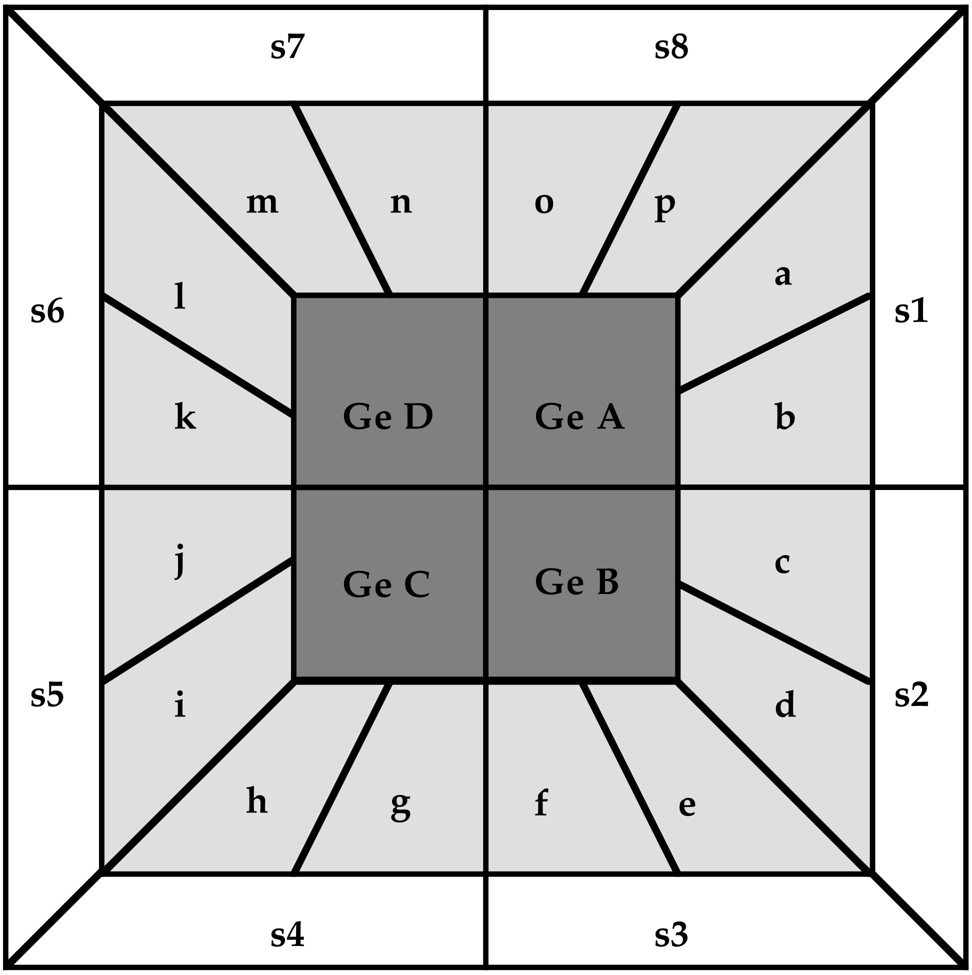
Operating modes will be defined by loading a look-up table whose addresses are all the 13 discriminator outputs (8 BGO and 5 Ge) and whose outputs control sumbuses and the veto decision. The 3 modes described above will be 3 different LUT configurations. The LUT may be loaded to always check all 5 Ge inputs in which case there is no need to change the LUT when swapping channels after a failure provided that the bad channel responds to its disable and ceases firing its CFD.

I have removed all reference to generating Ge multiplicity >1 on the grounds that the solid angle covered is similar to a tapered detector, so it is more likely that a hit in a second Ge within the clover is from a scatter than from a second gamma ray.



Block diagram of Eurogam Phase 2 Delector Card

Drawn: I.L. Jan 1993



Naming scheme for Clover Ge and BGO elements showing the mapping from 16 BGO elements to 8 BGO signals for the phase 2 electronics.

Drawn: I.L. Nov 1992

General Address Layout (Combined from Ge and BGO)

Address Space (offset into VXI address space)	Name
0x0000 to 0x00fe	Ge Common parameters ("Channel 0")
0x0100 to 0x01fe	Channel 1 Parameters (Ge A)
0x0200 to 0x02fe	Channel 2 Parameters (Ge B)
0x0300 to 0x03fe	Channel 3 Parameters (Ge C)
0x0400 to 0x04fe	Channel 4 Parameters (Ge D)
0x0500 to 0x05fe	Channel 5 Parameters (Ge Spare)
0x0600 to 0x06fe	Channel 6 Parameters (BGO)
0x0700 to 0x07fe	BGO Common parameters ("Channel 7")
0x2000 to 0x3ffe	Veto Pattern logic Table

The Module Parameters area is based on the Phase 1 Ge card address mapping. Some of these may also be used for the BGO channel and others (like FT sample) need to be separately adjustable. There is also some overlap of address usage between phase 1 Ge and BGO cards, so we define 3 address areas for the common parameters. Within channel 0 there is an area for Ge common parameters and one for Module (Ge + BGO) parameters. The rest of the BGO "common" parameters are mapped into channel 7 for software compatibility with Phase 1.

Channel 0 Sub-Address Spaces	Function
0x0000 to 0x002e	Ge Common Parameters
0x0030 to 0x00fe	Module Parameters (common to Ge & BGO)

Ge Common Parameters

Name	Offset	Access	Old Ge offset
CFD Width DAC	0x0000	w	0x0000
FT Sample Point DAC	0x0002	w	0x0002
Validation Sample Point DAC	0x0004	w	0x0004
Start Readout DAC (LT watchdog?)	0x0006	w	0x0006
Test Generator Amplitude DAC	0x0010	w	0x0010

Module Parameters (Common to Ge and BGO parts)

Name	Offset	Access	Old Ge/BGO offset
Analogue Multiplexor Selection	0x0030	*(temp W only)*	0x0030
Digital Multiplexor Selection	0x0032	r/w	0x0032
Voltage Inspection Line Selection	0x0034	r/w	0x0034
Controle des Fenetres	*0x0038 bit 6*	r/w	0x0036
Module Configuration Register	0x0038	r/w	0x0038
Test Pulse Attenuator on/off (Ge only)	*0x0038 bit 7*	r/w	0x003a
Test Write to Readout Data FIFO	0x003c	w	0c003c
Test Read from Readout Data FIFO	0x0040	r	0x003e

v2.2 Moves Controle des fenetres and test pulse attenuator bit registers into MCR (0x38).

0x38	*Test Att*	*CDF*	*not used*	*not used*	*Rst Fifo*	*not used*	*Rej/mark*	*LastCard*

At this stage in testing, AI lines are write only. Hopefully will revert to r/w later.

Channels 1-6

The addresses within the spaces allocated to channels 2 to 5 (Ge A to Ge Spare) will be the same as on the present phase 1 Ge Card in those address spaces and the addresses within channel 6 (BGO) will be the same as those within channel 6 of the present phase 1 BGO card. This permits the software to treat these channels exactly as at present which means that the EUROGAM Register Server software and the EG Session Ge and BGO windows can be used virtually unchanged.

BGO Common Parameters (Channel 7)

Name	Offset	Access	Old BGO offset
Veto Width DAC	0x0600 n/a	w	0x0000
Discriminator DeadTime Width DAC	0x0602	w	0x0002
Sumbus Pulse Width DAC	0x0604 n/a	w	0x0004
FT Sample point DAC	0x0606	w	0x0006
Validation Sample Point DAC	0x0608	w	0x0008
PDS Gate Width	0x060a	w	0x000a

Inspection Lines

The Ge and BGO inspection lines will be combined as follows:

Channel	Function
Channel 0	Disconnect Inspection Line
Channel 1	Ge channel 1
Channel 2	Ge channel 2
Channel 3	Ge channel 3
Channel 4	Ge channel 4
Channel 5	Ge channel 5 (spare)
Channel 6	BGO channel
Channel 7	Ge common parameters (logic only)

Channels 6 and 7 will overlap on certain signals such as Fast Triggers and Validations, but since the Ge and BGO will have different FT sample points, it is not unreasonable to keep the two sets of inspection lines entirely as they are now. This has the advantage also that all the phase 1 inspection line software can be re-used. The BGO elements s1-s8 map onto the old a-h inspection lines (analogue and digital); the old i and j inspection lines are not used on phase 2. The address mapping is not exactly as phase 1 and is shown in detail later along with the Voltage Inspection lines.

Veto Pattern Look-up Table

The pattern for Veto generation is loaded into a 8Kx4 memory array whose inputs are the pattern from the 8 BGO and 5 Ge discriminators and outputs are signals to determine the following:

* Veto the event?
* Drive Raw Ge sumbus?
* Drive Clean Ge sumbus?
* Drive BGO sumbus?

This table will be controlled by byte access at addresses from offsets 0x2000-0x3fff, each address corresponding to one possible pattern of discriminators. The pattern will be:

not used	not used	not used	Ge Sp	Ge D	Ge C	Ge B	Ge A	s8	s7	s6	s5	s4	s3	s2	s1
msb															lsb

The data at each location will be:

not used	not used	not used	not used	1= BGO sumbus on	1= Cl Ge sumbus on	1=Raw Ge sumbus on	1= Veto event.
d7	d6	d5	d4	d3	d2	d1	d0

Multiplexors and Voltage Inspection Lines

General layout of analogue and digital multiplexor control registers is unchanged:

d15	d14	d13	d12	d11	d10	d09	d08	d07	d06	d05	d04	d03	d02	d01	d00
fn 5	fn 4	fn 3	fn 2	fn 1	ch 3	ch 2	ch 1	fn 5	fn 4	fn 3	fn 2	fn 1	ch 3	ch 2	ch 1
Multiplex (analogue and digital) line 2								Multiplex (analogue and digital) line 1							

Analogue Inspection Lines

Changes are shown in italics

Ge (ch1-5) Function field: Analogue Muxes	**Name**
0	*4MeV PDS*
1	*TFA Input*
2	*TFA Output*
3	*4MeV Bipolar*
4	*FT TAC out*
5	*20MeV Unipolar*
6	*4 MeV Unipolar*
7	*PZ Adjust*

BGO (ch6) Function field: Analogue Muxes	**Name**
0	*Lecture (active H)*
1	*FIFOdtack (active H)*
2	*Renout* (active L)*
3	*Renin* (active L)*
4	*Test Generator output (mtxa113)*
5	*PDS output (mtxa112)*
6	*Shaping Amp output (mtxa111)*
7	*TAC output (mtxa110)*
8	*Line Receiver output H (mtxa100)*
9	*Line Receiver output G (mtxa101)*
10	*Line Receiver output F (mtxa102)*
11	*Line Receiver output E (mtxa103)*
12	*Line Receiver output D (mtxa104)*
13	*Line Receiver output C (mtxa105)*
14	*Line Receiver output B (mtxa106)*
15	*Line Receiver output A (mtxa107)*
16	*BGO Input A (mtxa114)*
17	*BGO Input B (mtxa115)*
18	*BGO Input C (mtxa116)*
19	*BGO Input D (mtxa117)*
20	*BGO Input E (mtxa118)*
21	*BGO Input F (mtxa119)*
22	*BGO Input G (mtxa120)*
23	*BGO Input H (mtxa121)*
24	*Line Receiver output H (mtxa100)*
25	*Line Receiver output G (mtxa101)*
26	*Line Receiver output F (mtxa102)*
27	*Line Receiver output E (mtxa103)*
28	*Line Receiver output D (mtxa104)*
29	*Line Receiver output C (mtxa105)*
30	*Line Receiver output B (mtxa106)*
31	*Line Receiver output A (mtxa107)*

Changes are shown in italics

Logic Inspection Lines

Ge (ch1-5) Logic Inspection Function Select	**Meaning**
0	CFD Delayed Output
1	Pre-pulse Pileup
2	PDS Gate
3	CFD Direct Output
4	FT Sample Point (W1)
5	Val Sample Point (W2)
6	LT reset
7	ADC Encode Command

BGO (ch 6) Logic Inspection Function Select	**Meaning**
0	*BGO Disable (mtxd118e)*
1	*BGO Valack (mtxd119)*
2	*BGO Encode (mtxd120)*
3	*Validation Pulse*
4	*Inhibit (Active Low)*
5	*LT reset*
6	*spare*
7	*spare*
8	*BGO TAC Start Pulse (mtxd110)*
9	*Fast Trigger Pulse*
10	*BGO PDS Gate (mtxd112)*
11	*BGO Fast Trigger Sample Point (mtxd113)*
12	*BGO Validation Sample Point (mtxd114)*
13	*BGO LT RO gate test point (mtxd115)*
14	*BGO Discriminator Deadtime (mtxd116)*
15	*BGO LT Start (orcfd-orlrec)*
16	*BGO disc h (mtxd100)*
17	*BGO disc g (mtxd101)*
18	*BGO disc f (mtxd102)*
19	*BGO disc e (mtxd103)*
20	*BGO disc d (mtxd104)*
21	*BGO disc c (mtxd105)*
22	*BGO disc b (mtxd106)*
23	*BGO disc a (mtxd107)*

Changes are shown in italics

Common (ch 7) LI line function select	**Meaning**
0	Fast Trigger Pulse
1	Validation Pulse
2	End of ADC Conversion
3	ROCI Data Acknowledge
4	OR all 6 ROCI Data Available (Active Low)
5	ADC Clock (4 MHz)
6	Last Pass
7	OR of ADC deadtimes

Voltage Inspection Lines

d7	d6	d5	d4	d3	d2	d1	d0
not used	V Select 4	V Select 3	V Select 2	V Select 1	Mux Sel 3	Mux Sel 2	Mux Sel 1
Voltage Inspection Lines: Bottom 3 lines select the Mux chip, and next 4 lines address it.							

Voltage Inspection Code (Data 7..0)	**Meaning**
xxxxx 000 (0, 8, 16, 24 etc)	Not connected to VXI
x0000 001 (1)	Ge 1 CFD Threshold (VO1(1))
x0001 001 (9)	Ge 1 CFD Output Delay (VO1(2)
x0010 001 (17)	Ge 1 PZ Adjust (VO1(3))
x0011 001 (25)	Ge 1 PDS gate (VO1(4))
x0100 001 (33)	Ge 2 CFD Threshold (VO1(5))
x0101 001 (41)	Ge 2 CFD Output Delay (VO1(6))
x0110 001 (49)	Ge 2 PZ Adjust (VO1(7))
x0111 001 (57)	Ge 2 PDS gate (VO1(8))
x1000 001 (65)	Ge 3 CFD Threshold (VO2(1))
x1001 001 (73)	Ge 3 CFD Output Delay (VO2(2)
x1010 001 (81)	Ge 3 PZ Adjust (VO2(3))
x1011 001 (89)	Ge 3 PDS gate (VO2(4))
x1100 001 (97)	Ge 4 CFD Threshold (VO2(5))
x1101 001 (105)	Ge 4 CFD Output Delay (VO2(6))
x1110 001 (113)	Ge 4 PZ Adjust (VO2(7))
x1111 001 (121)	Ge 4 PDS gate (VO2(8))
x0000 010 (2)	Ge 5 CFD Threshold (VO3(1))
x0001 010 (10)	Ge 5 CFD Output Delay (VO3(2)
x0010 010 (18)	Ge 5 PZ Adjust (VO3(3))
x0011 010 (26)	Ge 5 PDS gate (VO3(4))
x0100 010 (34)	Ge Test Pulser Output Level
x0101 010 (42)	CFD Width
x0110 010 (50)	Ge Fast Trigger Sample Point (DW1)
x0111 010 (58)	Ge Validation Sample Point (DW2)
x1000 010 (66)	Ge LT timeout (DW3)
x1001 010 (74)	*BGO Threshold*
x1010 010 (82)	*BGO Test Pulser Output Level (MTXC6)*
x1011 010 (90)	*BGO DAC ref (MTXC13)*
x1100 010 (98)	*BGO Fast Trigger Sample Point (MTXC15)*
x1101 010 (106)	*BGO Validation Sample Point (MTXC16)*
x1110 010 (114)	*BGO LT Timeout (MTXC17)*
x1111 010 (122)	*BGO PDS Gate (MTXC18)*
x0000 011 (3)	VREFDAC (Ge DAC reference)
x0001 011 (11)	Vee24
x0010 011 (19)	Vee18
x0011 011 (27)	Vee12
x0100 011 (35)	Vee6
x0101 011 (43)	Vee (-5.2V)
x0110 011 (51)	Vee2
x0111 011 (59)	*+3V regulator (BGO DAC ref)*
x1000 011 (67)	Ground
x1001 011 (75)	Vcc5 Analogue
x1010 011 (83)	Vcc5 Digital
x1011 011 (91)	Vcc6
x1100 011 (99)	Vcc12
x1101 011 (107)	Vcc18
x1110 011 (115)	Vcc20
x1111 011 (123)	Vcc24
xxxxx 1xx	*Connected to VXI, but not allocated on card*