University Of Liverpool

Eurogam Project

Eurogam Histogram Unit

Address map and Operation Instructions

12-November-1998

Release 3

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Eurogam Histogram Unit Memory and I/O address areas

A general description and operating instructions appear at the end of this document.

Look up table (RAM)	Size	64k Words
Write only		
(A32,D16)	Address (default)	F1000000-F101FFFF (SET on unit)
	(jumper selectable)	F1020000-F103FFFF
		etc.
		F10E0000-F10FFFFF
	(MVME147 window is	F1000000-FF7FFFFF for A32,D16)

I/O Addresses		
(A16,D8 & D16)		
	Addresses (default)	0000-000F (SET to FFFF000x)
	(jumper selectable)	0100-010F
		0200-020F
		etc.
		0700-070F
	(MVME147 I/O window	FFFF0000-FFFFFFFF)

I/O subaddress (WRITE)

subaddress (offset from base)			Data Range	Function
	0	word	0000-01FF	write MS word to reset counter (start RAM address)
	2	word	0000-FFFF	write LS word to reset counter (start RAM address)
note1	4	word	0000-01FF	write MS word to reset comparator (end RAM address)
	6	word	0000-FFFF	write LS word to reset comparator (end RAM address)
note2	9	byte	--00---1F	write VSB top address bits
	B	byte	--00---FF	write to status(control) register (as above)
	C	word	any value	reset missed hits counter

Note1-For 32 MByte of VME RAM the maximum value to clear all locations is 0080. This takes approximately 2 seconds. All VSB addresses and data are 32 bits wide.

Note2-The VME and VSB memory addresses MUST be set at the same locations on the MVME224A-4 RAM cards.
For a VME address of 10000000 hex the VSB top 5 address bits are set to 02 hex.

I/O subaddress (READ)

subaddress (offset from base)		Data Range	Function
B	byte	--00---FF	read status register
C	word	0000-FFFF	read missed hits counter MS word (must be read first)
E	word	0000-FFFF	read missed hits counter LS word (must be read last)

(All other short I/O address reads will not return valid data however no bus error is generated).

Status register

Bit number	Function	Logic levels
0	Run status	1=running 0=halted
1	Mode	1=Load/Test 0=normal (Test if running,Load if halted)
2	Test REN	1=REN set 0=REN cleared (only in TEST mode)
3	Stop on VSB data counter overflow	1=selected 0=do not stop
4	VSB ram clear	1=underway 0=finished
5	VSB data counter overflow	1=Overflow detected 0=no overflow
6	missed hits counter overflow	1=Overflow detected 0=no overflow
7	VETO enable	1=VETO enabled 0=VETO disabled

Control register

Bit number	Function	Logic levels
0	Run/Halt histo	1=RUN histogrammer 0=HALT histogrammer
1	Set mode	1=Test/Load mode 0=Normal mode
2	Set REN status	1=REN set 0=REN cleared (for TEST mode only)
3	STOP on Overflow	1=HALT if VSB data counter overflows 0=ignore overflow (do not HALT)
4	Start VSB RAM clear	1=start clear operation 0=no effect
5	Force RESET	1=forces full histogrammer reset 0=no effect (note - does not clear RAM)
6	-	-
7	VETO select	1=enable VETO input 0=ignore VETO input

After RESET is done status reads 02 i.e. all bits cleared and unit set to LOAD RAM mode.

Operation examples;-
(assumes RAM address set to F1000000-F101FFFF, I/O addresses FFFF000x)

For the following all values are in hex.

1) To initialize histogram unit
   a) write 20 to FFFF000B
   b) write 02 to FFFF0009 to set VME RAM address equal to VSB address

2) To clear VME data collection RAM.
   a) write 20 to FFFF000B (byte) (force RESET)
   b) write start address of area to be cleared MSB to FFFF0000 (word)
   c) write start address of area to be cleared LSB to FFFF0002 (word)
   d) calculate end address+1 of area to be cleared
   e) write end address of area to be cleared MSB to FFFF0004 (word)
   (max value with 32MByte is 80)
   f) write end address of area to be cleared LSB to FFFF0006 (word)
   g) write 10 to FFFF000B (byte) (start RAM clear)
   h) read and test status (FFFF000B) for bit 4 cleared (1=Ram clear in progress)

3) Loading redirection ram on histogram card
   a) write 20 to FFFF000B (byte) This sets histogrammer to Load mode and Halted.
   (load mode may also be entered by writing 02 to FFFF000B)
   b) write word wide data to RAM (start location F1000000-end F101FFFF)

bits D0-D14	offset address of data collection RAM
bit D15	histo this data (1=yes 0=no)

4) Normal mode of operation
   a) write 01 to FFFF000B for normal mode data collection running, no stop on data overflow, no VETO mode selected.
   or write 81 to FFFF000B for normal mode data collection running, no stop on data overflow, VETO mode selected.
   or write 09 or 89 for above modes with stop on overflow enabled.
   b) write 00 to FFFF000B to halt collection.

5) Test mode
   a) write 03,83 or 0B (as in 4 above but with test bit set i.e. 01,03,etc) to FFFF000B
   b) write data, word wide, to addresses F1000000-F101FFFF to simulate DT32 input
   c) repeat (b) above for data words required in test
   d) write 07,87 or 0F to FFFF000B to generate simulated REN signal (REN=1)
   (data is now transferred to data collection RAM unless VETO present in VETO mode)
   e) test may be repeated from (a) to (d) as required (REN cleared at (a)).
   f) write 20 to FFFF000B to reset unit on completion of test.

Description of Control bits

Bit 0	Run/Halt	This bit determines if input data from either the DT32 bus or in test mode will be collected. 1=collect data, 0=halt. This bit must be 0 for loading the onboard RAM and 1 in test mode.
Bit 1	Mode	This bit has two functions dependant on the state of bit 0 (see above). When set to 1 the unit is in Test or Load Mode and when 0 normal data collection mode is entered.
Bit 2	set REN state	During test mode it is nesessary to simulate the REN signal, normaly received on the DT32 bus after the last data word has been transmitted (to the event builder). The receipt of REN high is simulated by setting this bit to 1, returning it to 0 before further data is received. (REN must also be low (set to 0) when simulation data is written to the histogrammer. The REN signal must be low on the DT32 bus for the simulation to function correctly. The DT32 40way input cable can be removed to acheive this if nesessary though this should not be required normaly). This bit MUST be set to 0 for normal data collection.
Bit 3	Stop on VSB data counter overflow (histogram channel overflow)	When set to 1 data collection will be terminated if any histogrammed data value reaches FFFFFFFF. If set to 0 the data value will 'wrap around' through 00000000.
Bit 4	Start VSB ram clear	By setting this bit to 1 the VSB data collection RAM will begin to be cleared. Writting a 0 to this bit has no effect. The status bit 4 will reflect the state of the RAM clear operation and the bit is cleared on completion of the task.
Bit 5	Force RESET	When a 1 is written to this bit a master reset is generated which Halts data collection, clears the FIFOs and sets the unit to Load/Test mode. All status bits are cleared with the exception of the Load/Test bit which is set to 1.
Bit 6	No function	-
Bit 7	VETO enable	When set to 1 VETO mode of operation is entered. This mode is used with the LEMO -ve NIM input on the front of the unit to VETO all the data collected by the FIFO for the present REN cycle. The VETO input must be present (-1v/-20mA) at the input connector when the REN signal goes HIGH in order to VETO the event. A 0 written to this bit disables the VETO operation.

Description of Status bits

Bit 0 Run/Halt When set to 1 the histogrammer is collecting data. When 0 it is halted.

Bit 1 Mode When set to 1 the histogrammer is in either Load or Test mode depending on the setting of bit 0.

i.e.

Bit 1	Bit 0	Function
0	0	normal mode and halted
0	1	normal data collection going
1	0	Load on board RAM with data
1	1	Test mode

Bit 2 REN status Tests the state of the simulated REN signal generated for test use. Must be set to 0 for normal operation.

Bit 3 Stop on VSB data counter overflow (when histogram channel overflows)
Reflects the status of control bit 3. Set to 1 if the unit is to cease data collection on a data value of FFFFFFFF. Set to 0 if 'wrap around' selected. (see control bit 3)

Bit 4 VSB clear When responding with 1 the VSB RAM is in the process of being reset to zero. When set to 0 the clearing of the RAM is completed.

Bit 5 VSB data counter overflow
Set to 1 if the VSB data counter has overflowed in any location. Cleared by any control register write.

Bit 6 missed hits counter overflow
This bit is set to 1 if the counter which counts the data words not histogrammed overflows. It is cleared by any write to the control register.

Bit 7 VETO enable Set to 1 if the VETO mode of operation is selected. A 0 indicates that the unit is NOT in VETO mode.

General Description

The histogram module is a double width 6U high VME module which uses the VSB bus and a VSB/VME memory card to store data. Data is collected from the DT32 BUS input connectors mounted on the front of the histogram unit. The data passes back onto the DT32 BUS from the histogrammer output connectors and is unaltered. In VETO mode the PASS signal (DT-RENout) will be inhibited until an input FIFO within the histogrammer is available for further data. In NORMAL (non VETO) mode the DT-RENin is passed transparently to DT-RENout and is not delayed. The histogrammer should be positioned as the last unit in the DT32 BUS chain before the HSM interface and event builder. A VSB back- plane is required to connect the histogram card to the VSB RAM card (modified Motorolla MVME224A-4 32 MByte VME/VSB RAM card) but note that the VSB back-plane should not run behind the processor card. More than one histogram module may be fitted to a crate but each module must have a separate VSB back-plane and RAM card. One processor will control two or more units provided different addresses are used for the RAM and histogram cards of the two systems. If necessary two or more RAM cards can be fitted to one VSB bus to expand the histogram memory size in 32 MByte blocks. The maximum VSB memory addressable by one histogram card is 128 MBytes (which is unlikely to be required). Data is written 32 bits wide on the VSB bus with the top 5 bits of the VSB address being selected by loading a register from VME. The VME and VSB addresses must be the same. The least significant 5 bits of the byte written to the VSB address register define the VSB address most significant 5 bits. e.g. writing 02 to the VSB address register selects a VSB start address of 10000000_{HEX}. See Figure 1.

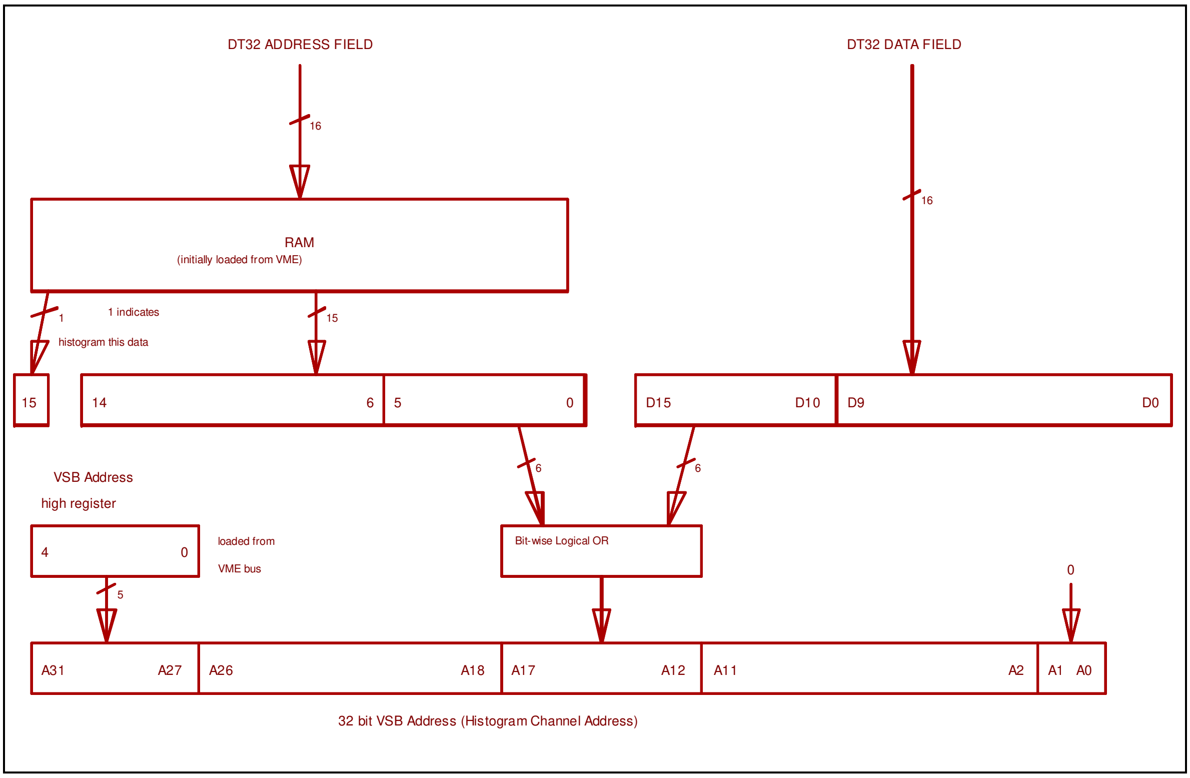

Fig 1. Formation of histogram VSB address.

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The values written into the DT32 RAM allow user selected detectors to be placed where required in VSB RAM. This dynamic positioning means that less VSB RAM space is required and that data may be placed within one VSB RAM area rather than in locations spread about as the original DT32 values may be. The top RAM bit determines if the particular detector information is to be histogrammed or not (1 or 0). To load the RAM initially from VME the status bits 0 and 1 in the control register must be set (bit 0=0 halted, bit 1=1 load).

Your attention is drawn to the documents from the Daresbury Laboratory, which specify the operation and format for the DT32 data transfers and the histogrammer use (Specification of Histogrammer, J Alexander)(DT32 Bus Specification: J Alexander)(Data formats on the DT32 bus:D Brightley).

Data is received on the DT32 bus, the top bits, as shown in figure 1, are fed to the RAM to redirect the data on the lower bits to the correct histogram channel in VSB RAM. The central bits are logical-ORed between data and address so that ADCs with greater resolution (i.e. number of bits) may be implemented without modifications to the unit. Normally the top data bits are set to 0 and the histogram channel address over-writes them. The 32 bit histogram channel address thus formed is fed into an input FIFO which fills with successive values until the REN signal goes high to indicate the end of the data transfer. In non-VETO mode the FIFO is now emptied into an output FIFO which starts to update the VSB channels while the input FIFO is freed to take further input. The values in the output FIFO are used as 32 bit addresses on the VSB bus.

The cycle on the VSB bus is as follows. The output FIFO value is placed onto the VSB bus and the data from the selected location is read into a counter on board the histogram card. The counter is incrimented by one and the data value thus generated is written back via the VSB bus into the same memory location from where it came. To ensure that the same address location is accessed for the write, a small modification is required to the Motorolla RAM card. This involves cutting pin 10 on U113 on the RAM card and wiring the pin to +5V through a 10k resistor. (The modification can be undone if required at any time by reconnecting the pin).

In VETO mode the transfer of data from the input FIFO to the output FIFO can be prevented by holding the VETO input on (-20mA into 50ohm or -1V) at the time the REN signal goes high, the end of the data transfer cycle. Data in the FIFO is discarded and the histogrammer will accept new input straight away. If no VETO input is received and both input FIFOs contain data when RENin goes high, then the RENout signal (PASS) is inhibited until space is available in one of the FIFOs. If however the output FIFO becomes full the RENout signal is released and the histogrammer shuts out data until space is available in an input FIFO. Data will only be collected again if the histogrammer input is released before any new data from an event is received, i.e. only full event data will be collected. All missed DT32 data words are counted and can be read out from the 'missed hits counter' on the histogrammer. Missed hits means any DT32 data word value that failed to histogram, due for instance to there being no input FIFO space. This counter must be read out in the correct address sequence, the most significant word first followed by the least (I/O offset from base, C_{HEX} then E_{HEX}, read word wide). The missed hits counter can be reset by writing any word wide data value to location I/O base+C_{HEX}.

Clearing data collection RAM

All operations on the VSB Bus are 32 bits wide which allows selected areas in RAM to be cleared very quickly. First the start address of the block to be cleared is loaded into the counters on the histogram card and then the address after the last to be cleared is loaded into the comparators (i.e. finish address+1). These values are stored and will not need reloading for subsequent clear operations unless new areas of RAM are to be cleared. Zero data is written into all locations in VSB RAM that lie between the start address and the end address and include the start address value. To start the RAM clear cycle a 1 is written to bit 4 of the control register. This bit cannot be reset to a 0 (except by doing a master reset command) but it will return to 0 when the operation of clearing the RAM is complete. This allows the status of the operation to be checked. If invalid addresses are specified (e.g. outside the available RAM area) for the counters and comparators RAM clear bit will not have reset to 0 after a period of a few seconds and this indicates that the VSB has hung up and a master reset will be required to free it. This should not occur in normal circumstances but only with programming or user error. It should take less than 2 seconds to clear 32MBytes of VSB RAM.

Test mode

The histogram unit enters test mode when control bits 0 and 1 are both set to 1 (run and test). Data is written to addresses as if loading the look up table RAM (same address field). The data lines from VME become simulated DT32 data input and the VME address becomes the DT32 address applied to the look up table RAM. e.g. writing to the 3rd RAM location on the histogrammer will redirect the VME data written at the same time to the destination address contained in the 3rd RAM location. The look up table RAM is not altered in test mode. The simulated REN signal (control/status bit 2) must be low at this time and multiple writes are possible to fill a portion of the FIFO. When sufficient test data has been written the REN bit is set to 1 to transfer the FIFO data to the output FIFO and then into the VSB memory. The simulated REN can be returned to 0 at any time but must be low before further test data is written to the histogrammer. The simulated REN must also be set low for normal histogrammer use. The VETO, if selected and present on the input connector, will operate in the test mode as it does in the normal mode of operation. It is advisable to do a RESET command (setting control bit 5 to 1) at the end of the test period before normal use resumes. This will ensure all FIFO contents are removed.
The unit reverts to halted, no VETO enabled, all counter overflows cleared, do not stop on data counter overflow, REN cleared (0) and load RAM selected.

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Addendum 12-Nov-1998 With thanks to Bernard Humbert (Fr). The histogram unit will apparently work with the RAM card from Micro Memmory type MM-6326D. A mod is required to the RAM card as follows.

1. Lift and isolate pin 12 of U65 (74f74 chip)
2. Connect a jumper from pin 12 of U65 to pin 7 of U65 (ground/earth).