EDOC226

Midas

Register Definitions for the Ortec 413 ADC

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Registers for the Ortec 413 ADC module

This document should be read in conjunction with the document **EDOC210** which describes the **Register Server** implementation for **CAMAC**.

This is a 4 channel ADC module with FERA and CAMAC data readout.

All register attributes include -c (crate address) and -n (station address)

Registers using the **xCAMAC** class of the **CAMAC** Register Server

control register 1 read by f(0) a(0) & write by f(16) a(0)

This control register is composed of two distinct sections. The least significant 8 bits contain the Virtual Station Number (VSN) which determines the address of the data source during FERA readout. The most significant 8 bits determine the readout modes.
Note that most of the control bits use bit=0 to enable the option and hence the register **enable**s the option when value=0.

bit 8	ZSE	Zero-Suppression Enable. Specifies zero-suppression readout (ZSE=0) as opposed to sequential mode (ECL or CAMAC) or random access (CAMAC) (ZSE=1) (see CSR).
bit 9	EEN	ECL port Enable (EEN=0) or CAMAC readout (EEN=1)
bit 10		not used
bit 11		not used
bit 12	CME	Specifies coincidence mode (CME=0) or singles mode (CME=1).
bit 13	CSR	Specifies CAMAC Sequential Readout (CSR=0) or CAMAC random access readout (CSR=1).
bit 14	CLE	Asserts CAMAC LAM (CLE=1) when data is ready to be readout on the CAMAC port. If CLE=0 no LAM is asserted.
bit 15	OFS	OverFlow Suppression: when OFS=0 then data is suppressed (ZSE=0) or reported as zero (ZSE=1). If OFS=1 then data overflows are reported with a value between 8064 and 8191.

ot413#*.control1	attributes -a 0 -f 0 -w 16 -p rw -l 0 -b 0 -z x -i 0
ot413#*.control.vsn	attributes -a 0 -f 0 -w 16 -p rw -l 8 -b 0 -z x
ot413#*.control.mode	attributes -a 0 -f 0 -w 16 -p rw -l 8 -b 8 -z x
ot413#*.control.zse	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 8 -z d
ot413#*.control.een	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 9 -z d
ot413#*.control.cme	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 12 -z d

ot413#*.control.csr	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 13 -z d
ot413#*.control.cle	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 14 -z d
ot413#*.control.ofs	attributes -a 0 -f 0 -w 16 -p rw -l 1 -b 15 -z d

control register 2 read by f(0) a(1) & write by f(16) a(1)

This control register contains 5 bits which determine which gate signals are enabled. If a gate signal is disabled then a pulse is accepted regardless of the state of the gate signal.
Again note that the register **enable**s the option when value=0.

bit 0	gate1	Front-panel gate for channel 1 enabled (gate1=0) - gate for channel 1 disabled (gate1=1).
bit 1	gate2	Front-panel gate for channel 2 enabled (gate2=0) - gate for channel 2 disabled (gate2=1).
bit 2	gate3	Front-panel gate for channel 3 enabled (gate3=0) - gate for channel 3 disabled (gate3=1).
bit 3	gate4	Front-panel gate for channel 4 enabled (gate4=0) - gate for channel 4 disabled (gate4=1).
bit 4	gatem	master gate enabled (mgate = 0) - master gate disabled (mgate = 1)

ot413#*.control2	attributes -a 0 -f 1 -w 16 -p rw -l 5 -b 0 -z x -i 0
ot413#*.gate1.enable	attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 0 -z d
ot413#*.gate2.enable	attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 1 -z d
ot413#*.gate3.enable	attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 2 -z d
ot413#*.gate4.enable	attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 3 -z d
ot413#*.gatem.enable	attributes -a 0 -f 1 -w 16 -p rw -l 1 -b 4 -z d

Lower level discriminator read by f(1) a(x) and write by f(17) a(x)

The lower level discriminator (8 bits) is accessed for channel x (0-3) using subaddress x. The initial value (36) is the hardware default. The register value is in units of 2mV.

ot413#*.adc*.lld attributes -a x -f 1 -w 16 -p rw -l 8 -b 0 -i 36

ADC data read by f(2) a(x)

random access or sequential readout of the 4 ADC values via the CAMAC dataway. Channel x (0-3) is selected using subaddress x in random access readout only (CSR=1). In sequential mode (CSR=0) the subaddress is ignored. Also requires EEN=1 (CAMAC readout enabled) and ZSE=1.

ot413#*.adc*.data attributes -a x -f 2 -w 16 -p ro -l 0 -b 0

Registers using the **cCAMAC** class of the **CAMAC** Register Server

These registers do not require data and have no initial value. However read-register operations may return Q and X as data.

clear	**write or read by f(9) a(0)**

module clear

ot413#*.clear	attributes -a 0 -f 9

test LAM	**read by f(8) a(0)**

returns Q=1 if the module LAM is set

lc4300b#*.testlam	attributes -a 0 -f 8