EDOC221
CDOC221

EUROGAM DATA ACQUISITION SYSTEM
CHARISSA DATA ACQUISITION SYSTEM

Register Definitions for the GANELEC QDC1612F ADC

Edition 1.0

Oct 1995

Nuclear Physics Support Group

Central Laboratory of the Research Councils
Daresbury Laboratory

Registers for the GANELEC QDC1612F ADC module

This document should be read in conjunction with the document **EDOC210** which describes the Register Server implementation for **CAMAC**.

This is a 8 channel dual integration ADC module with FERA and CAMAC data readout.

All register attributes include -c (crate address) and -n (station address)

Registers using the **xCAMAC** class of the **CAMAC** Register Server

status register read by f(0) a(0) & write by f(16) a(0)

The status register controls the readout mode and allows the duration of the Master gate to be selected.
Note - bit numbering is bit 0 (LSB) and bit 15 (MSB).

bit 0	EPS	ECL port Pedestal Subtraction: when EPS=1, pedestals are subtracted for ECL port readout
bit 1	ECE	ECL port data Compression Enable: when ECE=1, data zeros or zeros-and-overflows are suppressed for ECL port readout.
bit 2	EEN	ECL port Enable: when EEN=1 ECL port readout is permitted, when EEN=0 CAMAC readout is permitted.
bit 3	CPS	CAMAC Pedestal Subtraction: when CPS=1, pedestals are subtracted for CAMAC readout
bit 4	CCE	CAMAC data Compression Enable: when CCE=1, data zeros or zeros-and-overflows are suppressed for CAMAC sequential readout.
bit 5	CSR	CAMAC Sequential Readout: when CSR=0, CAMAC random access readout is enabled; when CSR=1, CAMAC sequential readout is enabled
bit 6	CLE	CAMAC Lam Enable: when CLE=1, LAM is enabled
bit 7	OFS	OverFlow Suppression: when OFS=1, data readouts are suppressed during ECL port readout in conjunction with ECE=1 and for CAMAC sequential readout in conjunction with CCE=1
bit 8	INDIV	INDIVidual. If INDIV=1, only the individual gates FIGi and SIGi are authorised; if INDIV=0, only the common gates FCG and SCG are enabled.
bits 9 to 12 (4 bits)		Duration of the Master gate in microsecs. Maximum duration is equal to 16 microsecs.

```
qdc1612#*.status          attributes  -a 0  -f 0  -w 16  -p rw  -l 0  -b 0  -z x -i 0
qdc1612#*.status.mode     attributes  -a 0  -f 0  -w 16  -p rw  -l 9  -b 0  -z x
qdc1612#*.status.Mgate    attributes  -a 0  -f 0  -w 16  -p rw  -l 4  -b 9  -z d
qdc1612#*.status.eps      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 0  -z d
qdc1612#*.status.ece      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 1  -z d
qdc1612#*.status.een      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 2  -z d
qdc1612#*.status.cps      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 3  -z d
qdc1612#*.status.cce      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 4  -z d
qdc1612#*.status.csr      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 5  -z d
qdc1612#*.status.cle      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 6  -z d
qdc1612#*.status.ofs      attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 7  -z d
qdc1612#*.status.indiv    attributes  -a 0  -f 0  -w 16  -p rw  -l 1  -b 8  -z d
```

Virtual Station Number #1   read by f(0) a(1) & write by f(16) a(1)

Accesses the virtual station number VSN1 of the first group of analog inputs 1 to 4 (8 bits).

```
qdc1612#*.vsn1      attributes  -a 1  -f 0  -w 16  -p rw  -l 8  -b 0 -z d
```

Virtual Station Number #2   read by f(0) a(2) & write by f(16) a(2)

Accesses the virtual station number VSN2 of the second group of analog inputs 5 to 8 (8 bits).

```
qdc1612#*.vsn2      attributes  -a 2  -f 0  -w 16  -p rw  -l 8  -b 0 -z d
```

Pedestal memory   read by f(1) a(x) and write by f(17) a(x)

The pedestal memory (8 bits) is accessed for integrating channel x (0-15) using subaddress x. Integrating channel 1 corresponds to analog input 1 and narrow integrating gate; integrating channel 2 corresponds to analog input 1 and wide integrating gate etc.

```
qdc1612#*.channel*.pedestal      attributes  -a x  -f 1  -w 16  -p rw  -l 8  -b 0
```

ADC data read by f(2) a(x)

random access or sequential readout of the 16 16 bit data words via the CAMAC dataway. Channel x (0-15) is selected using subaddress x in random access readout only (CSR=0). In sequential mode (CSR=1) the subaddress is ignored.

qdc1612#*.channel*.data attributes -a x -f 2 -w 16 -p ro -l 0 -b 0

DAC Voltage write by f(16) a(3)

Writes the voltage for the DAC delivering a common pedestal current to all integrating channels (8 bits).

qdc1612#*.Vdac attributes -a 3 -f 16 -w 16 -p wo -l 8 -b 0

Registers using the **cCAMAC** class of the **CAMAC** Register Server

These registers do not require data and have no initial value. However read-register operations may return Q and X as data.

reset write or read by f(9) a(0)

module reset

qdc1612#*.reset attributes -a 0 -f 9

test LAM read by f(8) a(0)

returns Q=1 if the module LAM is set

qdc1612#*.testlam attributes -a 0 -f 8

test LAM and clear read by f(10) a(0)

returns Q=1 if the module LAM is set and clears the LAM

qdc1612#*.testclearlam attributes -a 0 -f 10