CDOC220

CHARISSA DATA ACQUISITION SYSTEM

Event Control Module User Manual

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Event Control Module

General Description

In a Charissa D/A scheme an Event Control module works in conjunction with a Trigger Interface, a set of Silena ADCs (Silena 4418) and a Data Stack (LeCroy 2375). The ADCS are read over a fast bus FERA and held in the Data Stack until subsequently read by a Daresbury Read and Store module.This module will also read any associated Camac modules such as TDC's Scalers and Pattern Registers. The first group of ADC channels are termed FERA and these may be accepted subject to their content being within a prescribed range while the latter channels are termed NORMAL and these are read without reference to their content.

A basic system is arranged so that 128 channels may be included in a single event and this is transferred to the Daresbury Read and Store module in two blocks of 64 channels labelled Trigger 25 and 26 which are the first two trigger types following the Daresbury Trigger 24. If a system is restricted to FERA channels only then in a developed version of this basic scheme the Event Control module generates trigger types from 25 through to 32 so that 512 channels may be included in a single event.See Read and Store Format below.

General Operation

At the start of an event the user must supply a strobe followed by a gate signal which will start the conversion process at the ADCs (Silena 4418). When conversion is complete then the data is read sequentially along the FERA bus which is connected to the Event Control module and to the Data Stack (LeCroy 2375). The Event Control will test each channel word as it is generated on the bus and will select those channels that have been enabled and are within a preset dynamic range. Selected data is recorded in the Data Stack and is also marked in a hit word store within the Event Control. Once all the sequential data has been transferred then the hit word pattern from FERA channels is merged with the NORMAL channels within the Event Control and used to generate a control sequence of header and hit words that are sent to the Read and Store module. From this point the system operation follows that of the Daresbury D/A system and data is transferred to the Read and Store buffer first from the Data Stack and then from the Camac modules which make up the NORMAL channels.

Prompt and Delayed mode

An Event Control module operates in one of two modes either Prompt or Delayed.Prompt mode resembles the familiar Daresbury Trigger 24 where a set of channels are specified at the beginning of an event and then the Event Manager returns only those channels that have successfully converted. In the Charissa system a Trigger Interface is provided which enables a user to select patterns of channels that should be read by pulsing these at event start time. After the conversion is complete then the Event Control will select only those channels that have been defined at the Trigger Interface and are within a specified range.

Prompt mode starts when the Strobe and Gate signals have initiated conversion and it is signalled at the Trigger Interface by a Trigger Request. During the conversion period of 32 microseconds the user may either choose to abort the event by sending a Clear signal or set a trigger pattern and declare the rigger Ready. Where the choice of trigger pattern is already known at strobe time then the Trigger Request is connected directly to the Trigger Ready but the user may abort the event from 32 microseconds after it has been initiated. The read phase which follows conversion will wait until the trigger pattern has been written to a hit word store within the EC unit. This is usually done inside the conversion period so that readout of the data from the Silena ADCs will begin immediately after conversion is completed.

Each ADC contains eight channels and as each group of eight data words arrive at the Event Control then a byte of eight bits is selected from its hit word store. This byte contains a bit for each channel that has been enabled and only those channels that are enabled and are within the threshold set at the EC unit but below the upper level discriminator defined at the Silena will be transferred onto the data stack and marked in the hit byte. The hit byte is then restored to the store and this process of comparing and marking each channel continues until all of the FERA channels have been read. At this point the hit word store will contain a modified hit pattern of those FERA channels which have been accepted along with the original hit pattern for those NORMAL channels which must also be be read. The Event Control unit is then ready to prepare the header word and transfer the first block of header and hit words to the Read and Store module.

In the Delayed Mode the speed of the FERA bus (125ns/word) has been exploited by allowing the user access to the intermediate state of the data, immediately following conversion. (32 microseconds) The pattern of those FERA channels within range is returned at the Trigger Interface and the user may then describe additional NORMAL channels eg TDCs/Scalers which should be read in conjunction with an event.

When Delayed Mode is selected then all FERA channels are enabled and readout will follow immediately after conversion is complete. Again like the Prompt Mode a user may choose to abort an event within the 32 microseconds conversion time. During readout only those channels which are above the threshold set at the EC unit and below the upper level discriminator at the Silena will be transferred to the data stack and marked in the hit byte. At the end of the readout phase this pattern of accepted FERA channels is returned to the user as a trigger output pattern and the Trigger Request signal set. The user may now decide on additional NORMAL channels which should be read and these must be set at the inputs to the Trigger Interface. A Trigger Ready input will restart the Trigger Interface and the additional hit patterns will be written to the hit word store. The Event Control unit will then produce the header and hit word set for the Read and Store module to begin reading the event.

Trigger Interface

When Prompt Mode is set then all channels at the User Trigger Interface will be inputs indicated by green LEDs. A Channel Limit switch is mounted on the Trigger Interface and this defines the boundary between red and green channels.This switch should be set at zero for Prompt Mode. An input may either be permanently set by simply connecting a Lemo cable to the lower input socket or selectively set by connecting it to Fast NIM level. Any number of channels may be daisy chained together. In Delayed Mode the first set of channels equivalent to the number of FERA channels will be outputs while those channels which follow will be inputs. The Channel Limit switch is then set to the number of FERA bytes and this will also change the indicators so that FERA outputs are shown as Red while NORMAL inputs are shown as Green.In Delayed mode a NORMAL channel may either be defined by connecting it directly to a FERA output, a select Fast NIM level or permanently set by inserting a Lemo cable.

At the Trigger Interface all input sockets use a special Lemo connector which automatically removes a 50 ohm termination as the cable is inserted. It is this arrangement which permits any number of NORMAL channels to be linked together and driven from a single FERA channel.When the termination is removed but the input is not connected to an output then the input appears as if it is permanently enabled.

Accept All Data mode

The Silena ADCs that form the FERA channels have alternative operational modes which may be set through Camac and reference should be made to the 4418 User Guide for details of these formats.The readout mode used by the Event Control module is a full read of all eight channels from each ADC and uses the Event Control to suppress those channels that have zero content. In an alternative mode termed zero suppression the ADC will produce two header words to describe the address and hit pattern for each ADC followed by a sequence of data words 1 through 8. If no data is available from an ADC then the header words are also deleted and control simply skips past the ADC on the FERA bus.

If zero suppression is required then the Event Controller must be switched into an Accept All Data mode which effectively inhibits the threshold test and allows all data to go from the ADCs through to the Data Stack. In this mode the conversion time will vary from a minimum of 8.0 microseconds where only one channel has fired for any ADC through to a maximum of 32.0 microseconds where eight channels have fired in any ADC. This mode is particularly useful where very large channel arrays are used but only a few channels are active within any event. The Prompt and Delayed modes are no longer relevant since the data being transferred to the Date Stack in now controlled by each ADC in turn. If Delay mode is used then the number of FERA channels must be set at the maximum possible channels for an array of ADCs (10 * n) where n is number of ADCs. The Red channel indicators at the Trigger Interface now show the total channels being transferred over the FERA bus as a continuous sequence from channel 1 followed by a gap before the Green channels appear indicating the NORMAL channels

Read and Store Format

The format of the header word which precedes the hit word set sent to the Read and Store module has been extended to include extra information. The Daresbury Event Manager has 23 Trigger Types which may describe various set patterns of channels and a Trigger Type 24 which is a free form trigger that describes a set of channels that have successfully converted within a larger set that have been enabled. Triggers 25 through to 32 have been used in the Charissa scheme to describe the eight blocks of data that may be produced from a single event. Thus channels 1 through 64 are described as Trigger Type 25 ....channels 438 through 512 as Trigger Type 32. Bit 8 was spare in the header format and this has been used to show whether another block follows within the current event. This bit has been called the MORE bit and will be attached to all blocks except the final block in an event set.

Empty Events

If no data is present at any channels either FERA or NORMAL then the Event Control will sense this condition as it prepares the header information and will cancel the event so that the Read and Store does not record an empty event. This Empty Event test may be switched off so that all events are recorded irrespective of their content if this is required.

Limit and Fera Registers

A LIMIT register defines the total number of bytes that may be transferred and this register will control both the number of trigger words exchanged between the EC module and Trigger Interface along with the number of hit words in the header/hit word set sent to the Read and Store module. In this register 1 will be equivalent to 2 bytes which is the minimum number of bytes that may be transferred.

A FERA register defines those bytes which are reserved for Silena ADCs and again 0 will be equivalent to 1 byte so that the minimum system must include 1 FERA byte. A test switch is provided that will enable all channels to be defined as Camac channels for test purposes.

Camac Commands

The set of CAMAC command codes used to control the operation of this module are as follows.

When the module is in an operational state then error conditions are reported through the LAM interrupt. These errors include a timeout for FERA,Trigger and Read and Store failure along with a check for the FERA transfer which is called whenever the number of channels read is unequal to the limit value. All error states may be individually disabled.

F0	A2	Reads Digital Discriminator	Disabled by EMO
F1	A1	Read Total Limit and Control Status	
F1	A2	Read Cache Limit and Control Status	
F8		Test state of LAM	Q active if LAM
F11	A1	Complete clear of module	Disabled by EMO
F11	A2	Clear error status only	
F16	A1	Write to Digital Discriminator	Disabled by EMO
F17	A1	Write to Cache and Total registers	Disabled by EMO
F17	A2	Write Control Status	
F24		Disable LAM	
F25		Simulate STROBE	Disabled by EMO
F26		Enable LAM	
F27	A1	Test EMO state	Q active if EMO
F27	A2	Test TEST state	Q active if TEST

For the **F16,A2** command the digital threshold is written in an eight bit register. The least significant bit is equivalent to 2 in this register and corresponds to W1 with the MSB corresponding to W8.

For the **F17 A1** write to limit registers the Cache limit is set by W1 through W8 (W1=LSB) while bits W9 through W16 set the Total limit (W9=LSB)

For the **F0, A2** command the output of the digital register is read into R1 the LSB corresponding to channel 2 through to R8 the MSB

For the **F1 A1,A2** commands either FERA is read (A2) or the Total is read (A1) and both reads appear in the bits R1 through R8 (R1=LSB). The remaining bits R9 through R16 indicate status as follows:

R9	Module not Busy
R10	Delay Mode
R11	Accept All Data
R12	Channel Number incorrect for FERA read
R13	Timing Error in Read and Store cycle
R14	Timing Error in FERA cycle
R15	Timing Error in Trigger cycle
R16	Module Operation Enabled (EMO)

For the **F17 A2** write status command only bits W12 through W16 are used as follows.

W12	Enable cache read error
W13	Enable Read and Store timeout error
W14	Enable FERA timeout error
W15	Enable Trigger timeout error
W16	Enable Operation. EMO state

F25 may be used to simulate a Strobe input.

The EMO state must be set to enable the Event Control to operate and this will automatically inhibit many of the CAMAC commands. EMO state is sensed by **F27 A1**.

All Error returns will produce a LAM interrupt to Camac if this has been enabled by an **F26** command. Error state is sensed by **F27 A2**.

The LAM state is tested by **F8** and will return Q when Error is present and the LAM Enable state has been set by **F26**.

X status will be returned on all commands and Q status will also be returned on all commands except where stated above for **F8** and **F27** commands.

Strobe and Gate Input

An event is started by a Strobe Input signal which immediately sets a Busy level to inhibit any further strobes. The strobe is shaped to 100ns and sent out as a Strobe Output signal. Once the strobe has initiated the Event Control module then a Gate Input should be sent to overlap the peak of the analogue inputs to the ADCs (see Silena manual). This gate will be directed to all ADC channels that are attached to the FERA bus and will also inhibit any further gate inputs until the current event has been serviced.

The falling edge of the gate signal will initiate a conversion delay period which may be adjusted at the front panel. This delay is set to be greater than 32 microseconds and is used to protect the conversion period for the Silena ADCs on the FERA bus. In the Accept All Data mode the conversion period ends when the Request signal appears on the FERA bus. A Clear signal may be given at any time after the strobe and before the end of the conversion delay. This may be used to abort the current event.

Miscellany

When either a Gate Input or a Clear Input are accepted then they will produce a Gate Output or a Clear Output pulse respectively. The Event Control module may also be inhibited either through an input at the Inhibit Input or through the Camac dataway. The Busy or Dead Time output will begin at the Strobe signal and continue through until the Read and Store module has completed its Camac readout phase.

The Event Control will generate a Scaler Inhibit signal at the rear mounted Lemo whenever the system is halted by setting EMO to zero or when the EC is waiting for the Read and Store to recover from a clogged state. An External Inhibit is also located at the rear of the module and this will allow a user to hold the Event Control inactive during an experimental run.All input and output signals are fast NIM.

Indicator LEDs show the Dead Time, LAM interrupts to Camac and each phase of the EC module eg FERA/Trigger/Read and Store.

The modes of operation Delayed/Prompt and Accept All Data are set by switches at the rear of the module.
An automatic restart condition occurs whenever the EC has been in a Busy state for over 2 milliseconds and the error condition stored. This timeout will not occur while the Read and Store module is in a clogged state.

References

Other material which is related to the Event Control includes:

The Trigger Interface

Event Control Sequence Description which describes each state of the internal control based on a Signetics 82S100

Event Control Drawings

Event Control Drawing Description

EC592 Read and Store User Guide

Mod 4418 CAMAC 8 input ADC User Guide by Silena

Model 2375 DATA STACK Users Manual by LeCroy