EDOC072

# EUROGAM PROJECT

# NSF DATA ACQUISITION SYSTEM

## General Purpose Interface (GPI)

Edition 1.00
Feb 1991

NSF Electronics Development Group
UK Science and Engineering Research Council
Daresbury Laboratory

# General Purpose VXI Input Card Specification

Ian Lazarus
email: Lazarus%daresbury.ac.uk@UKACRL (bitnet)

THU 21 FEB 1991 11:07:27

## 1 Status and history

This document contains some thoughts which will form the basis for a fuller specification if they are agreed to describe what is actually required. Please make comments and suggestions to the author.

## 2 Why we need a General Purpose VXI Input card

The General Purpose VXI Input (GPI) card has many uses. The one which was in my mind when I suggested it was to allow a common real time stamp to be clocked into each crate of a system, and into separate data acquisition systems for very slow devices. For this application the fast trigger in each of the two (or more) systems clocks a register to staticise the real time clock. The event builder can later merge the data streams and correlate events with a fixed time relation.

Another use is to bring in RMS data directly to the VXI backplane so that it is read along with the Ge and BGO cards and the whole event is assembled on the VXI backplane rather than making a special derandomising readout controller for the RMS. This method was also proposed by John Cresswell in his discussion paper on RMS data collection.

The GPI card has the flexibility to cover other unforseen data sources or any bit patterns, status information and suchlike which have been overlooked. I think it is important to remember that the Liverpool 'bit box' ADC emulator had to be built for the Daresbury EMs and we shouldn't make the same oversight twice of not anticipating non-detector inputs on an event by event basis. It is finally a sort of insurance policy against things going badly wrong in that it is a simple card which can be made to treat the VXI/VME system purely as a digital readout system with all analogue processing external (maybe in NIM).

## 3 Overview of card

The GPI will have two main parts: the VXI interface which will be common to all variants, and the 'personality' module(s) which will vary with the application.

The VXI interface will look like the interface in the Ge or BGO card (register based devices, VME slave only without interrupter capability). The VXI configuration registers and control will come from the Clement/Deschamps LCA which will ensure compatibility with other Eurogam cards. The interface will permit the reading of data from its FIFO using either conventional VME reads or the high speed EUROGAM ren/pass style readout mechanism. The VXI interface will be on the main 'mothercard' and most of this card will be empty, accepting one or more personality daughterboard of whichever type is required.

The personality modules will contain as little or as much as is necessary for the application. A simple 32 bit parallel input register will suffice for such things as entering a bit pattern or a timestamp, while interfacing NIM ADCs from the RMS requires a more complex module to deal with ADC gating and resetting. Personality modules will have access to the trigger signals (fast trigger, validation and associated event number) and will implement their own version of a local trigger to control timing and ensure synchronisation with the rest of the system. Trigger signals are available as normal via the VXI backplane.

Each personality module will probably need its own front panel, although the simpler modules such as timestamp and parallel input register might well be able to use the same front panel. The modules themselves will be in the form of daughter boards which will connect to the front panel and, via a standard pinout at a fixed position, to the VXI interface. The standard connection to VXI will contain a VME interface for programming registers VXI signals the following other connections:
Inputs from VXI:

- Fast Trigger (1)
- Validation (1) (selectable from the 3 backplane Validation lines)
- Event Number (4) (for labelling the event)
- Data read strobe (1) (into fast readout FIFO)
- Inhibit Action (1)

Outputs to VXI:

- Data word (32 bits including parameter number and qualifiers)
- Inhibit request (1)
- Data read acknowledge (1) (into fast readout FIFO)
- Inspection lines (Analogue and digital) and other diagnostic signals

*Should we have multiple daughter board interfaces allowing a 'mix and match' approach (and an horrendous front panel problem!) or limit ourselves to a single daughter board typically with 8 identical channels and its own front panel?*

# 4 Some personality module proposals

## 4.1 Simple Parallel Input Module

- Inputs:
  - 32 channels on front panel per channel, 8 channels. (LEMO and IDC sockets in parallel with fast NIM and ECLLine thresholds respectively.)
  - All inputs registered with choice of common clock (Fast trigger or validation from VXI backplane or user supplied clock from front panel, either LEMO or IDC with fast NIM or ECLLine threshold.)

- Outputs
  - 32 bit output to VME bus using standard Eurogam VXI bus readout mechanism.
  - Output data may be optionally cleared by the VME read (for data which changes event by event or only appears in some events). In this case the data only go into readout if they are clocked in at the appropriate time.

### 4.2 NIM ADC module

For this module, cabling will be the limiting factor. Each NIM ADC has a 37 way D type connector from which its data is collected and some control may be performed. The ADC also has a VIEW/RTP output and a GATE input which might need to be controlled from the GPI NIM ADC Module (NAM). A 40 way IDC connection could handle all necessary signals, although extra LEMO sockets might be required for easier cabling of VIEW/RTP and GATE signals. These space requirements suggest that 8 ADCs could be connected to each single width GPI card with NAM.

The connections to NIM ADCs are not exactly identical (DL EC643 uses a different connector type to the Laben 8115, and the Silena 7420 is very similar to the EC643, but not quite the same) so although the GPI end of the cable will be standard, the cables themselves, and the NIM end will vary according to the ADC to be read.

There are 3 options for the NAM NIM interface:

1. Make it look like an 8 channel, trigger 24 only event manager with auxiliary trigger inputs to select the ADCs and a Master Gate for the timing. The master gate controls tha timing for ADC gating, but must take account of whether the ADCs are in coincidence with a Eurogam event, so the user's NIM logic must include the Eurogam Fast Trigger and validation signals in the master gate. The Fast Trigger is available to user electronics as a fast NIM signal on a coax cable direct from the Master Trigger card and the Validation on a multidrop ribbon cable sending ECLLine signals from the Master Trigger to the RMs and to user elctronics. (If it helps, Fast Trigger and Validation signals could also be made available directly from the NAM which gets them from the VXI backplane.)

   The 8 'auxiliary triggers' and the master gate would pass through a panel similar to what is now used and would be connected to the NAM via a single cable which would also carry the RTP/VIEW signals from the ADCs and the GATE inputs to the ADCs.

2. Supply Fast Trigger and Validation to users as above (either via NAM or from Master Trigger Card and Resource Managers) and leave users to take care of gating the ADCs. In this case the NAM would read data from all ADCs which indicated that they had data within a programmable time (typically 5$\mu$s) of the validation.

3. Use the Eurogam Validation as a GATE signal to all NIM ADCs. This is the simplest solution in theory, but probably places unreasonable constraints on the timing of the Eurogam Validation signal both in terms of duration and start time. This would be permissible in the common deadtime mode, but would be unacceptable for parallel or pipelined operation.

All 3 solutions would read data from the ADCs via their back connectors and put it in as part of the Eurogam VXI readout. The NAM could also disable individual ADCs and reset them with the ability to observe their status (enabled/disabled) too.

```
Back view of 4 NIM ADCs shown:
Real system could handle up to 8.
+--------+--------+--------+--------+
|  NIM   |  NIM   |  NIM   |  NIM   |
|  ADC   |  ADC   |  ADC   |  ADC   |<@@@@@@@@@@@@@@@@@
|        |        |        |        |                 @-----LEMO - BNC cables
|        |        |        |        |<@@@@@@@@@@@@@@  @     from panel to ADC
|        |        |        |        |              @  @     front panel for:
|        |        |        |        |<@@@@@@@@@@@  @  @         RTP/VIEW
|        |        |        |        |           @  @  @         GATE
|        |        |        |        |<@@@@@@@@  @  @  @     (1 set per ADC)
|  * 37  | * 37   | * 37   | * 37   |        @  @  @  @
|  * way | * way  | * way  | * way  |        @  @  @  @
|  * D-  | * D-   | * D-   | * D-   |        @  @  @  @
|  * type| * type | * type | * type |        @  @  @  @
+--#-----+-#------+-#------+-#------+        @  @  @  @
   #       #        #        #            +--------------------+ MASTER GATE
   #       #        #        #            | Panel for RTP/VIEW |<%%%%%%
   #       #        #        #     @@@@@@@| ADC GATE, AUX Trigs|
   #       #        #        #     @      | MASTER GATE sockets|<$$$$$$
   #       #        #        #     @      +--------------------+ Aux Triggers
   #       #        #        #     @
   #       #        #        #     @----- Ribbon Cable linking
   #       #        #        #     @      Panel to/from GPI
   #       #        #        #     @      (1 per GPI)
   #       #        #        #     @  ___________________________________
   #       #        #        #     @  |\ General Purpose Interface (GPI) \
   #       #        #        #     @  | +-----------------------+----------+
   #       #        #        ######@####|                       |          |
   #       #        #              @  | |                       |VXI       |
   #       #        ###############@####|        GPI            |Interface |
   #       #                       @  | |        Daughter Board |          |
   #       ########################@####|                       |and       |
   #                               @  | |        NIM            |          |
   ################################@####|        ADC            |VXI       |
      |                            @  | |        Module         |Readout   |
      |                            @  | |        (NAM)          |Mechanism |
  Ribbon cables linking            @@@@@|                       |          |
  GPI to ADC (1 per ADC)              | |                       |          |
  For data readout and                | |                       |          |
  ADC control                          \|                       |          |
                                        +-----------------------+----------+

Diagram of Option 1 for GPI NIM ADC Module connections (4 ADCs only shown)
-------------------------------------------------------------------------
```