Interface adaptor for FIC8230 to FPI - Draft 1.0 P.J.Coleman-Smith

Requirements

The adaptor is necessary to provide the data link from the Eurogam VME sort crate to the GEC.
The data link must be :-
A: Faster than 500Kbytes per second.
B: Bi-directional.
C: Between a FIC8230 in the Sort crate and an FPI in the GEC computer.

Interface descriptions.

FPI

The FPI module consists of two channels, one transmit, and one receive. They both have the ability to be 16 or eight bits. They both use an asynchronous handshake. The module sits in a GEC computer crate connected to the Normal Interface. Both channels have the ability to carry out block level control.

The channel will use the following signals.

FPI channel signals	Description
Data 0 - 15	TTL logic true data
DREADY	TTL negative logic, data ready on Data0-15, may only be asserted when DACCEPT is false.
DACCEPT	TTL negative logic, data has been taken from Data0-15 and may be removed.
RXACT	TTL negative logic, Receiver is active and able to take data.
TXACT	TTL negative logic, Transmitter is active and has data to send.

FIC8230

This is a VME single board intelligent controller. It contains a 68020, interfaces to VSB, and VME, and among other functions a four channel DMAC (DMA controller) with an 8 bit peripheral bus. The bus includes data strobe and acknowledge, channel selects, bus requests, and address lines.

The DMAC will carry out data transfers between its peripheral bus and the FIC RAM, VSB, and VME.The DMAC will pack and unpack bytes to form 32 bit words for transfer.to the RAM VME or VSB.

DMAC peripheral bus signals	Description
Data 0- 7	TTL true logic, data.
Address 0-4	TTL true logic address
Bus request0-3	TTL negative logic, address used during a bus transfer.
Channel select0-3	TTL negative logic, used to select peripheral accessed, corresponds to the request used.
Write	TTL negative logic, when true indicates a write to peripheral.
Data strobe	TTL negative logic, data transfer handshake initiator.
DTACK	TTL negative logic, peripheral acknowledges data cycle complete.
Peripheral done	TTL negative logic, used on peripheral to memory cycles to indicate when last cycle of a block transfer is occurring.

Implementation

Adaptor configuration.

The adaptor will be considered as two channels, one for each direction. Transmit will be from VME to GEC, and Receive will be from GEC to VME.

The transmit channel will be implemented as a 16 bit interface to the FPI, and an 8 bit to the FIC. The adaptor will contain two 8 bit latches, and a control PAL. The block control will be implemented. This will use one of the four DMAC channels.The DMAC will transfer bytes into the two latches, and then these will be written to the FPI.

The receive channel is a 16 bit interface to the FPI, and an 8 bit to the FIC. The adaptor will contain two 8 bit latches, and a control PAL. This will use one of the four DMAC channels.The block control will be implemented. The FPI will transfer data a word at a time to the latches, and then these will be read by the DMAC.

The FIC processor will be used to control the interface, that is setting up the DMAC, and handling error conditions and reporting. The adaptor will be controlled by an eight bit register accessible via the DMAC peripheral bus.

Transmit channel

The transfer of data will take the following course.

FIC side	Adaptor	FPI side
DMAC programmed with transfer size, source address, and control information.		FPI receive channel enabled
		RXACT goes true.
	sets request 1	
DMAC sets select 1, enables lsbyte onto data bus	sets TXACT true	
sets data strobe true	clocks data into lsb latch, and sets PDTACK true	
removes data strobe	removes PDTACK	
enables ms byte and sets data strobe true	clocks data into MSB latch and sets PDTACK true	
removes data strobe	removes PDTACK, sets DREADY	receives 16 bit data and sets DACCEPT.
enables next byte, and sets data strobe	removes DREADY	removes DACCEPT
	clocks data into Lsb latch and sets PDTACK	

From this point the data transfer repeats until the FPI sets RXACT false, or the DMAC transfer count reaches 0, and as a consequence removes select1. Either of these will cause the other to occur, however in the case of the DMAC terminating and a word left in the adaptor, the word will be transferred if the FPI can accept it.

Receive Channel

FIC side	Adaptor	FPI side
DMAC programmed with transfer size, destination address, and control information.		FPI transmit channel enabled
		TXACT goes true. 16bit word enabled , DREADY set true.
	sets request 0 latch 16 bit data into Lsb latch and Msb latch.	Remove DREADY and enable next word .
DMAC sets select 0, and sets data strobe true	sets RXACT true, enables Lsb latch onto peripheral bus, and sets PDTACK true	
sets data strobe false	removes PDTACK	
sets data strobe true	enables the Msb onto the bus , and sets PDTACK true	
sets data strobe false	disables data , and sets PDTACK false. Sets DACCEPT false	sets DREADY true

From this point the data transfer repeats until the FPI sets TXACT false, or the DMAC transfer count reaches 0, and as a consequence removes select0. Either of these will cause the other to occur, however in the case of the FPI terminating and a word left in the adaptor, the word will be transferred if the DMAC can accept it. The state of the block handshake lines will be available in the status register.

Adaptor status and control.

This will be a single eight bit word at select 2 which can be accessed by the processor on the FIC8230 via the DMAC peripheral bus. It is possible to access this by a processor byte read or write, there is no need to set up a channel transfer.

The bits will be allocated provisionally in the following manner.

Control(Write) / Status(Read)	Description
Bit 0	A write of a one to this bit will cause a reset pulse to be generated in the adaptor, resetting the adaptor. This will clear any hung transfers by forcing all block handshake lines false for the period of the pulse. A read will return 0.
Bit 1	Read only, this will reflect the state of the TXACT signal on the transmit channel
Bit 2	Read only, this will reflect the state of the RXACT signal on the transmit channel
Bit 3	Read only, this will reflect the state of the TXACT signal on the receive channel
Bit 4	Read only, this will reflect the state of the RXACT signal on the receive channel
Bit 5--7	Not yet allocated . ANY IDEAS ?