EDOC055

EUROGAM PROJECT

NSF DATA ACQUISITION SYSTEM

Eurogam Master Trigger Card

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Eurogam Master Trigger Module

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1 Introduction

This document describes the Master Trigger unit and is an expansion of the information contained in the overall Eurogam Trigger Specification document. It has been updated to contain small changes to the real production boards and now acts as a user guide as well as a specification.

Updated again July 1992. *Changes from rev 2.0 are partially textual (rewritten explanations) with the addition of the following hardware changes:*

- *Add FIFO Reset bit in 0x86 bit 15*
- *Change name of Setup Ge CFD bit to better describe its action (0x86 bit 6), see also text in section 6.3*
- *Change Status register (0x98) bits 0,3,4, all of which can be read elsewhere, to reflect 3 new error checks:*
  - *bit 0 is FIFO Error, i.e. one FIFO full or empty and others not.*
  - *bit 3 is Readout Sequence Error, i.e. parameters read from FIFO are not as expected by trigger readout logic.*
  - *bit 4 is ROCO Event Number Fault, i.e. the Event number from ROCO is not that expacted by Trigger.*
- *Prescaling factors range increased (0x88)*
- *2 new logic inspection line signals added (see section 8).*

The Master Trigger unit is a single VXI card which contains logic to decide when an event has occurred on the basis of logic and current sumbus inputs. It issues a Fast Trigger as soon as it recognises an event and follows this with a Validation pulse later which gives the user an opportunity to make an optional second logic decision. The Master Trigger module can handle all 3 possible modes of system operation: common deadtime, parallel and pipelined. The change between modes is achieved from software.

The Master Trigger also supplies data during readout over the VXI backplane containing an event header together with various optional information about the event itself such as digitised multiplicities.

The logic decisions as to whether or not to accept an event are programmable using reprogrammable logic arrays which may be modified by the user according to his experimental requirements.

2 Input stage

The inputs to the Master Trigger module are firstly from the physics of the event (Sumbuses and logic inputs) and secondly information about the status of the system.

2.1 Sumbuses

The physics inputs are primarily in the form of sumbuses. There are 4 different sumbus inputs to cater for raw Ge, clean Ge, BGO and a user defined sumbus from additional detectors other than the main Eurogam Ge/BGO ball. Each of the 3 main sumbuses has 8 Lemo inputs to service up to 8 crates in a star cabling configuration. The user sumbus has only 2 inputs since it is not expected to come from a large VXI system, and other signals were considered more important in the limited front panel space. The buffered sum of the sumbus inputs is also available to the user as an output for each of the four sumbuses (maximum 10mA).

The buffered signal from each sumbus is fed to four comparators, each with a programmable threshold set from a DAC. The output from the comparators is then available as a logic signal in triggering decisions. Each of the 4 sumbuses produces 4 outputs, making a total of 16 logic outputs from this section.

2.2 Logic Inputs

There are 6 front panel logic inputs for the Fast Trigger and another 6 for the Validation decision, each via Lemo inputs. The logic inputs are each fed to a comparator which compares them to a common threshold. This threshold is set by a DAC (one DAC for all 16 inputs) and allows either a fast NIM or ECL threshold. Other thresholds within the range ± 5V are also allowed (e.g. TTL, slow NIM).

2.3 Inhibit_req

There is a front panel (fast NIM level) Lemo input which has the same effect as the VXI Inhibit_req when asserted. This allows non-VXI ROCO devices to pause readout and also allows the system to be paused by other things, for example the autofill system might pause data acquisition when filling detectors to overcome microphonics problems.

2.4 System inputs

System inputs come from the Slot 0/RM cards via an ECLLine cable. These are signals such as Readout which are used in the common deadtime mode to determine when a new Fast Trigger may be issued, or Inhibit_req which means that a module somewhere is requesting a pause in data acquisition because it is not ready (e.g. ROCO buffers full or Slot 0/RM accessing a VXI module to change a parameter).

2.5 Other inputs

There are 3 other special front panel inputs for use in setup (see section 6.3). These are LEMO connections. The first is a fast NIM input which stops the TAC in the trigger card and comes from either a fast scintillator or maybe the CFD of a Ge chosen as time reference. The other 2 are used for a known delay line (cable delay) used in calibration of TACs in Ge or BGO cards.

3 Outputs

The Master Trigger module generates 3 main outputs: Fast Trigger, Validation and Inhibit. These are physics signals which happen on an event by event basis.

There are also system signals which happen under software control such as VXIGo, Clear, Synch Triggers, and Transfer_scalers_to_shadow_registers.

3.1 Fast Trigger

The Fast Trigger line is distributed over matched lengths of coaxial cable from the trigger card to each RM card from the 8 parallel outputs which service up to 8 crates. It is used to logically include Ge and BGO channels in an event and to stop the TACs of all the channels which are included in the event. Typically happens 200 to 300ns after the first CFD has fired.

3.2 Validation

The Validation is a second level trigger which allows slower information such as the detection of a recoil fragment to validate the current event between $2\mu s$ and $10\mu s$ of the CFD firing. The absence of a Validation pulse at the expected time in any channel signals that the current event has been rejected and will not be read. The front edge of validation is used to clock the event number lines on the VXI backplane; a minimum hold time of 200ns is guaranteed at the ROCO, Ge card and BGO card. Validation and the 4 bit event number are distributed via the ECLLine output cable to all Slot 0/RM cards.

3.3 Inhibit

This signal is used in Common Deadtime operation to inhibit all Local Triggers which are not involved in the current event. It is asserted with the Fast Trigger pulse and cleared at the end of readout. The benefit is that unused channels on a Ge card cannot now generate noise by trying to process a second event until the first has been read. In parallel and pipelined modes it indicates the period during which another event will not be accepted. In this case it is asserted from the Fast Trigger for a programmable inter-trigger gap, typically $2\mu s$. Inhibit is distributed via the ECLLine output cable to all Slot 0/RM cards.

4 Time Alignment

The logic inputs (sumbus threshold decisions and front panel logic signals) are all fed into a time alignment section where a gate and delay generator is triggered from the front edge to produce a pulse of programmable width after a programmable delay. The maximum delay is $2\mu s$ for the Fast Trigger logic inputs and the sumbuses with a longer delay of $10\mu s$ for the 6 Validation logic inputs. In each case the delay and width are programmable in 256 steps with an 8 bit code, giving resolutions of 8ns and 40ns respectively. The full scale value is set by an RC combination and cannot be changed by users.

All 28 gate and delay circuits are bypassed so that the signals produced by the input stage may be directly fed into the logic decisions.

5 Trigger logic decisions

There may be several possible trigger conditions, so the Master Trigger module can process and identify up to 4 different trigger conditions in parallel. The first condition recognised will cause the fast trigger output, i.e. the operation is a logical OR condition. The logic is implemented in 2 reprogrammable gate arrays (LCAs); one for fast triggers and one for validations.

The time aligned inputs from the gate and delay circuits and their bypass signals feed into the LCAs. Each LCA receives 4 gate and delay signals from each sumbus (one for each threshold) and 6 gate and delay signals from its own front panel logic inputs. The logic inputs also feed the LCAs directly. In addition, the FT LCA receives directly the 4 outputs from the 4 sumbus threshold checks on each sumbus. The Validation LCA also receives the pattern of Fast Trigger requests, one bit per trigger type or condition, called Fast Trigger Requests (FTR). The FTR pattern allows the Validation LCA to apply different validation conditions for different fast trigger types.

We will use the software supplied with the logic arrays to create a library of standard configurations. (Updates available on request for particular experiments, initially from the designer of the unit and later, after training, from the electronics support group.)

The FT LCA may be bypassed by the force FT input on the front panel although a trivial program is still required in the validation LCA.

The pattern of Fast Trigger requests is fed between the Fast Trigger logic and the Validation logic via a small FIFO because in parallel or pipelined mode we could receive 4 or 5 events before validating the first event, so we have a queue waiting for Validation. Obviously there must be a direct timing link from the Fast Trigger logic to the Validation logic to define the timing relation between the Fast Trigger and the Validation pulses which are separated by a constant (but programmable) time period. This is the StartVal signal. The width of the StartVal signal determines the period for which the validation LCA is active (i.e. looking for the validation condition) and the delay determines how long we wait from the start of the FT delay until the start of Validation.

The Fast Trigger output of the LCA is fed into a piece of logic which generates a Fast Trigger pulse to the outside world (FT G+D) of programmable duration after a programmable delay. The same logic also generates an Inhibit pulse of programmable width at the same time as the Fast Trigger pulse. In Common deadtime mode the Inhibit is of variable length, started by the Fast Trigger and stopped by the readout complete signal. For parallel or pipelined mode the Inhibit output represents the trigger deadtime (typically $2\mu s$ which is limited by the Ge card TAC range).

An Inhibit_req input from the ECLline front panel or from the front panel NIM Inhibit_req input prevents the generation of further Fast Triggers or Validations while it is true. This means that the current event is aborted if it has not yet been validated. The reason is that in parallel or pipelined mode the ROCO will use the Inhibit_req line to indicate that it has 16 outstanding Validations to be read into its memory and so all activity must stop until it has read one of these outstanding events. The ECLLine Inhibit output is asserted by the Master Trigger card to indicate this pause in acquisition to all crates.

5.1 Prescaling

The Fast Trigger requests may be prescaled to reduce the rate of such things as low multiplicity triggers. The scaling factors are 1,2,4,8 etc. and are selected from software via the FTR

Prescaling register.

6 Other Logic

The Master Trigger card contains other logic for: VME interfacing, VME readout, Setup, Monitoring trigger rates with scalers, Coding multiplicity levels with each Fast Trigger, Controlling the ECLline VXI connections to the Slot 0/RM card. All these are described in the following subsections.

6.1 VME Interfacing

The VME interface uses Altera EPLD chips which are common to the Trigger and the NAM board and will also be used in the GPI when it is produced.

6.2 VME Readout

The fast pseudo-VME readout mechanism is as specified in EDOC076. Implementation is in reprogrammable EPLD devices. Two additional readout methods exist: readout by individual VME Longword cycles from the FIFO, and readout of individual parameters in test mode by VME reads at the appropriate addresses. ROCI chips are not used because there are no serial output devices on the board.

6.3 Setup

For setup the trigger provides several special facilities.

1. TAC (range 1.8us) for setting up all Ge CFD output delays so that current pulses are aligned correctly at the Master Trigger card. Method is to set the "enable TAC and bypass FTLCA" bit in the Trigger's system control register and then disable all CFDs except the channel to be adjusted. The TAC will start when the selected sumbus indicates multiplicity = 1 and stop with a delayed signal from either a fast scintillator or a particular Ge whose CFD output is defined as a reference (so we must use a source with multiplicity 2 such as Cobalt-60). All Ge parameters are disabled, including the channel being adjusted, so the only data collected by the ROCO is from the trigger TAC. The Fast trigger condition is that raw Ge multiplicity=1, and Validation is a null step with no logical decision. Operating in this mode bypasses the FT LCA for better timing and connects one of the Threshold 1 sumbus outputs directly to the TAC start signal

   Alternatively we could enable all the Ge channels for this setup, collecting only 4 MeV energy from each Ge and using the address with this energy to route the trigger's TAC value into the appropriate Ge spectrum.

   The TAC is switchable (under software control) to comparator 1 on each of the 4 sumbuses to allow time alignment of all sumbus inputs.

   The TAC may also be used during normal running to digitize a timing measurement, but in this case the fast trigger logic is still bypassed and so only one multiplicity decision may be used for the fast trigger decision.

2. Calibration of Ge TACs. This is achieved by using one of two different delay references to bypass all the Fast Trigger generation logic and generate a Fast Trigger a fixed delay after multiplicity = 1 is detected. To achieve this, both the setup Ge TAC and the Enable Trigger TAC/bypass FTLCA bits in the system control register must be set. Validation is a null step with no logical decision, just a fixed delay after the Fast Trigger, and the Ge TAC is the only parameter enabled for readout. Using a source of multiplicity 1 we can enable all Ge channels for calibration at the same time since only one will be hit (except by background). When spectra have been accumulated with the first delay, the second is switched in its place by a relay controlled from software and a second spectrum is superimposed. The difference in the peaks is the time difference between the two delays which can be measured as accurately as necessary (sub nanosecond). This method does not set the zero point (start and stop at the same time) but does calibrate bin width exactly.

3. Test pulsers are provided in the Ge cards and BGO cards. The master trigger card drives the common 'synch triggers' line which fires the pulser in every Ge or BGO channels which has been switched to test mode by the software. The resulting 'event' proceeds as normal with a Fast Trigger based on multiplicity, and readout after Validation. The number of channels in test mode controls the multiplicity and the value programmed in each test generator DAC controls the size of its test pulse which appears to the system as energy.

6.4 Scalers

The Master Trigger card incorporates 6 scalers for rate monitoring of triggers. Each scaler may be individually enabled or disabled from software. The scalers are 32 bits wide. Scalers monitor the following:

- Fast Triggers generated successfully
- Validations
- Fast Trigger Request 1,2,3 and 4. (All after prescaling (see 5.1))

There is also a seventh scaler used for diagnostics and testing which is connected to the Fast Trigger LCA chip and used to monitor any signal within the chip which is routed to this scaler.

6.5 Coding Multiplicity

The Master Trigger card codes the analogue multiplicity indicated on the 4 sumbuses for every Fast Trigger. Calibration and conversion is required in software to convert coded values to multiplicity. This coding must be performed for every Fast Trigger and so is implemented using an 8 bit flash ADC to get sub microsecond conversion time. The phase 1 boards can only code multiplicity in common deadtime mode because there is no buffering of coded values. This could be added for phase 2 and phase 3 if required.

6.6 ECLLine VXI connections to Slot 0/RM card

There are two ECLLine connectors between the Master Trigger and the resource managers. The signals which are outputs from the trigger travel down a 40 way ribbon cable and the

signals into the trigger come from a 14 way ribbon cable. In both cases the electrical and connector specifications conform to the ECLLine specification produced by CERN[1].
All signals are active high on the ECLine cables.

- The following lines are driven under software control:
  - Synch triggers for testing
  - Transfer_scalers_to_shadow_registers
  - Clear
  - VXI Go
- The following lines are driven under hardware control:
  - Validation 1, 2 or 3 (only one driven; selected by software)
  - Event number (4 bits)
  - Inhibit
- The following lines are received from the Slot 0/RM card:
  - Coding
  - Readout
  - Inhibit_req

6.7 LEMO Connections to Slot 0/RM Card

The directly connected LEMO star topology lines (Sumbuses and Fast Trigger) have been described in sections 2.1 and 3.1. There are 8 outputs for the Fast Trigger pulse and 26 inputs for sumbuses (8 x 3 from 8 VXI crates plus 2 user defined inputs).

6.8 Summary

1. Connect "Sum" output of each RM to one of the 8 Raw Ge Sumbus inputs on the Trigger card.
2. If necessary, connect the AS1 and AS2 RM outputs to the Clean Ge and BGO sumbus inputs respectively.
3. Connect one of the FT outputs (FT1-8) to the SXin input on each RM. Use matched cable lengths to preserve timing of the signals.
4. Connect the 40 way output ECLline output cable to the RMs in a daisy chain (RMs have input and output clearly marked).
5. Connect the 14 way ECLline input cable to each RM in a daisy chain, and finally conect it to the trigger.
6. Connect any additional signals you require for special operations (eg stop TAC).

[1] 'A Specification for ECL Interconnections in Counter Logic' (EP-Electronics note 79-01) and 'A Specification for ECL Frontpanel Interconnections' by H. Verweij dated 5/7/82

7 Data supplied by trigger system to readout

The Master Trigger unit supplies the following information during backplane readout:

- Event Header, including 16 bits of event number (mandatory)
- Fast Trigger and Validation type number (Optional)
- Sumbus multiplicity (0 to 4 words) (Optional, BUT be careful; the same enable is used for the sumbus on/off and for the readout on/off)
- TAC word (Optional)

N.B. Since these data words, including the event header, are supplied via the normal VXI backplane readout process it places 2 very important restrictions on the Master Trigger card:

- **The trigger card must be in the first crate to be read on the DT32 chain.**
- **It must be the first device to be read over the backplane within its crate.**

This means that the crate containing the Master Trigger logic card has its normal slot 0/RM card in slot 0, the Readout Controller in slot 1, and the trigger card in slot 2, leaving slots 3 to 12 for Ge/BGO cards.

Failure to observe these restrictions will mean that the data stream will no longer start with an event header!

7.1 Data Format

The Eurogam data format was defined at the October 1990 Engineer's meeting in Strasbourg. The Master Trigger card conforms to that definition, producing the following data words:

```
Event Header word (mandatory)
-----------------------------
31  29          23              15                            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|1 1|1 1 1 1 1 1|1 1 1 1 1 1 1 1|<---- 16 bit event number ---->|
|qfy|   item    |     group     |msb                         lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+


Fast Trigger and Validation Request (Optional)
----------------------------------------------
31  29          23              15              07            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|1 1|i i i i i i|1 1 1 1 1 1 1 1|0 0 0 0 0 0 0 0|Val req  FTreq |
|qfy|   item    |     group     |               |1 --- 4 1 --- 4|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Item number is programmable between 30 and 3F
Group number is fixed at FF
For Val Req and FT Req all unused bits are 0. Untrue conditions are also 0.
FT and Val Requests which are logically true for the event are set to 1.
```

```
Sumbus Multiplicity (4 words, all with this format) (Optional)
---------------------------------------------------------------
31  29         23              15              07            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|1 1|i i i i i i|1 1 1 1 1 1 1 1|0 0 0 0 0 0 0 0|  Multiplicity |
|qfy|   item    |     group     |               |msb         lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Item number is programmable between 30 and 3F
Group number is fixed at FF


TAC word (Optional)
-------------------
31  29         23              15      11                    00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|1 1|i i i i i i|1 1 1 1 1 1 1 1|0 0 0 0|<---- TAC data  ------>|
|qfy|   item    |     group     |       |msb                 lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+

Item number is programmable between 30 and 3F
Group number is fixed at FF
```

The software must define the group and item fields in the 'parameter address' data fields. Software must also define the Header word.

8 Testing and Diagnostics

The card has test points connected to the VXI analogue and digital inspection lines by multiplexers. These are controlled from software, and the inspection points are made available on either or both of the analogue or the digital lines as appropriate.

The analogue lines allow inspection of:

- Raw Ge sumbus
- Clean Ge sumbus
- BGO sumbus
- User sumbus
- Threshold for front panel logic inputs
- TAC output

The digital lines allow inspection of :

- Output of comparator testing threshold 1 on each of the 4 sumbuses
- Output of gate and delay chips for the signals above.

- Fast trigger before gate and delay
- Fast trigger after gate and delay
- Validation before gate and delay
- Validation after gate and delay
- Inhibit output (after gate and delay)
- StartVal signal (delay from FT to Val and width of Val logic decision)
- FP stop signal for setup
- Start conversion signal for ADC (after TAC)
- Readout cycle AM code recognised
- VME address strobe
- Readout signal (backplane signal i.e. ANY readout)
- No data left for readout
- Clock VXI EPLD chip (maxclock)
- VXI readout pass signal.
- Write pulse into the readout FIFOs
- VXI Readout* line (inside the Mt card, i.e. Trigger readout)

The readout event data FIFO can be loaded and unloaded by VME accesses when the card is in test mode. It may also be loaded in test mode and then read using the fast pseudo-VME readout mechanism if the card is switched out of test mode before reading. This allows testing of the event data path.

9 VME Software Interface

There are many parameters to be programmed in the Master Trigger card, the largest single item being the RAM based logic arrays used for the logic decisions (8Kbytes allocated per chip). Also there are various computer controlled delays and registers, computer accessible scalers etc. to be written or read. Full details of the software interface will be found in the appendix.

The addressing uses groups of 20_{16} where each group performs a certain function. There are 4 groups of DAC's, 2 being DAC's for thresholds and 2 being DAC's from gate and delay circuits. The next group is for control and test functions, The 6th group is for scalers and the 7th is for parameter addresses. Finally there is the space for the Logic Array's program.

- **Group 0 DACs for timing and logic inputs**

  - 00_{16} Fast Trigger pulse width and delay

- 02_{16} Validation pulse width and delay
- 04_{16} Inhibit pulse width
- 06_{16} Fast Trigger to Validation delay and "Validation Active" width
- 08_{16} Threshold for front panel logic inputs
- $0A_{16}$ Sumbus test DAC
- $0C_{16}$ Sumbus select for test input.
- $0E_{16}$ to $1E_{16}$ unused

- **Group 1 DACs for Sumbus thresholds**
  - 20_{16} to 26_{16} Raw Ge sumbus thresholds
  - 28_{16} to $2E_{16}$ Clean Ge sumbus thresholds
  - 30_{16} to 36_{16} BGO sumbus thresholds
  - 38_{16} to $3E_{16}$ User defined sumbus thresholds
- **Group 2 DACs for gate and delay**
  - 40_{16} to $5E_{16}$ Gate and delay for sumbus comparator outputs
- **Group 3 DACs for gate and delay**
  - 60_{16} to $7E_{16}$ gate and delay for front panel logic inputs
- **Group 4 Control and test**
  - 80_{16} Analogue Multiplexing control
  - 82_{16} Digital Multiplexing control
  - 84_{16} Card Control register
  - 86_{16} System control register
  - 88_{16} FTR Prescaler register
  - $8A_{16}$ Scaler control register
  - $8C_{16}$ Read raw Ge multiplicity (test only)
  - $8E_{16}$ Read clean Ge multiplicity (test only)
  - 90_{16} Read BGO multiplicity (test only)
  - 92_{16} Read User defined multiplicity (test only)
  - 94_{16} Read TAC output (test only)
  - 96_{16} Read FTR and Val requests (test only)
  - 98_{16} Status Register (for error reporting)
  - $9A_{16}$ to $9E_{16}$ unused

- **Group 5 Scalers**
  - $A0_{16}$ Fast Trigger scaler
  - $A4_{16}$ Not used
  - $A8_{16}$ Validation scaler
  - AC_{16} FTR1 scaler
  - $B0_{16}$ FTR2 scaler
  - $B4_{16}$ FTR3 scaler
  - $B8_{16}$ FTR4 scaler
  - BC_{16} Diagnostic scaler
- **Group 6 Readout**
  - $C0_{16}$ Raw Ge sumbus parameter address
  - $C2_{16}$ Clean Ge sumbus parameter address
  - $C4_{16}$ BGO sumbus parameter address
  - $C6_{16}$ User defined sumbus parameter address
  - $C8_{16}$ TAC parameter address
  - CA_{16} FTR and Val request parameter address
  - CC_{16} Event Number (load counter)
  - CE_{16} Event Header
  - $D0_{16}$ Load Event data FIFO (for test only)
  - $D4_{16}$ Read Event data FIFO (for test only)
  - $D8_{16}$ to DE_{16} not used

APPENDIX: Software Interface

All registers and bit fields assume that the lowest number is the least significant. All bit field numbering starts from 0. All addresses are defined as offsets from the address defined by the *Offset Register* and the *required memory* field in the *Device Type* register.
The offset register must be on an 8 Kbyte boundary.

VXI operation is as a dynamically configured register based slave and follows the standard Eurogam software conventions for the *Configuration Registers*, i.e. in A16 address space in the 64 byte area defined by the logical address:

$$\text{Base\_Address} = ((\text{Logical\_Address}) * 64) + 49152$$

- ID and Logical Address register at 00_{16}
  Read=@cf20: Dev class (11=reg), Address Space(00=A16/24), Manufacturer ID (@F20)
  Write: Logical address.
- Device type register at 02_{16}
  read only (=@7130): Required Memory (0111=64K) and model Code (@130)
- Status and Control register at 04_{16}. As VXI spec, no device dependent bits.
  Write: bit 0= reset, bit 15 = A24 enable (no other bits used)
  Read: bit 2=passed (1), bit 3=ready (1), bit 14 MODID*, bit 15 A24 active
  (all others are 1)
- Offset register at 06_{16} (read/write) top 8 bits only
  Bottom 8 bits always 0.
- Serial Number at 08_{16} (read only)
- Modification level at $0a_{16}$ (read only)

The layout of registers and the offset of registers is defined as follows:

```
Name: Fast Trigger Pulse Gate and Delay    Offset: @0000  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<msb-------Delay-----------lsb>|<msb--------Width----------lsb>|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
Delay = 0 to 2us (7.8ns/step)
Width = 0 to 1us (3.9ns/step)

Delay starts when LCA recognises Fast Trigger condition.
```

Name: Validation Pulse Gate and Delay   Offset: @0002 write only

```
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<msb-------Delay-----------lsb>|<msb--------Width----------lsb>|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

Delay = 0 to 9.7us (38ns/step)
Width = 0 to 9.7us (38ns/step)

Delay starts when LCA recognises Validation condition.

Name: Inhibit Pulse width   Offset: @0004 write only

```
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<-----------Delay------------->|<msb-------Width-----------lsb>|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

Delay = 0 to 1us (3.9ns/step)
Width = 0 to 12us (47ns/step)

Delay starts when LCA recognises Fast Trigger. Should be set to either accompany or precede the Fast Trigger output (NOT to follow it).
In Common deadtime mode the width must be set to cover the period until readout starts. Recommended setting for common deadtime is 12us.
For Parallel/Pipelined operation, set width to trigger deadtime (typ 2us)

Name: Fast Trig to Validation Delay Offset: @0006 write only

```
 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<-----------Delay------------->|<msb--------Width----------lsb>|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

Delay 0 to 9.7us (38ns/step)
Width 0 to 9.7us (38ns/step)

Delay starts when LCA recognises Fast Trigger condition (NOT FT output from card after gate and delay).
Width defines the period for which the Validation logic is enabled, ie the time during which the Validation Front Panel Logic inputs are valid.

```
Name: Input Threshold DAC     Offset: @0008     write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
Threshold for Front Panel Logic inputs
+5V out = @0fff            1 lsb= 2*Vref/4096 (Vref=5V)
 0V out = @0800
-5V out = @0000
Useful values:
+2.0V out (TTL logical 1) = @0B33
-0.6v out (Fast NIM logical 1) = @070B
-0.9v out (ECL logical 1) = @0690


Name: Sumbus test DAC         Offset: @000A     write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |lsb|
|   |   |   |   |<------- DAC range 0 to 2.0V ----------------->|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
 DO NOT USE positive outputs  (@0801 to @0fff)
 0V out = @0800
 -5V out = @0000

Name: Sumbus select for test DAC         Offset: @000C    read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |sel|sel|
|<------------------- Not Used ---------------------->|sb1|sb0|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Select sumbus (bits 01 and 00)
sel   sel
sb1   sb0
---   ---
 0     0    Raw Ge sumbus
 0     1    Clean Ge sumbus
 1     0    BGO sumbus
 1     1    User defined sumbus
```

```
Name: Raw Ge Sumbus Threshold DAC 1  Offset: @0020   write only
Name: Raw Ge Sumbus Threshold DAC 2  Offset: @0022   write only
Name: Raw Ge Sumbus Threshold DAC 3  Offset: @0024   write only
Name: Raw Ge Sumbus Threshold DAC 4  Offset: @0026   write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
See separate calibration sheets

Name: Clean Ge Sumbus Threshold DAC 1 Offset: @0028  write only
Name: Clean Ge Sumbus Threshold DAC 2 Offset: @002A  write only
Name: Clean Ge Sumbus Threshold DAC 3 Offset: @002C  write only
Name: Clean Ge Sumbus Threshold DAC 4 Offset: @002E  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
See separate calibration sheets


Name: BGO Sumbus Threshold DAC 1 Offset: @0030  write only
Name: BGO Sumbus Threshold DAC 2 Offset: @0032  write only
Name: BGO Sumbus Threshold DAC 3 Offset: @0034  write only
Name: BGO Sumbus Threshold DAC 4 Offset: @0036  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
See separate calibration sheets
```

```
Name: User def Sumbus Threshold DAC 1 Offset: @0038  write only
Name: User def Sumbus Threshold DAC 2 Offset: @003A  write only
Name: User def Sumbus Threshold DAC 3 Offset: @003C  write only
Name: User def Sumbus Threshold DAC 4 Offset: @003E  write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
See separate calibration sheets


Name: Gate and Delay Raw Ge 1   Offset: @0040       write only
Name: Gate and Delay Raw Ge 2   Offset: @0042       write only
Name: Gate and Delay Raw Ge 3   Offset: @0044       write only
Name: Gate and Delay Raw Ge 4   Offset: @0046       write only
Name: Gate and Delay Clean Ge 1 Offset: @0048       write only
Name: Gate and Delay Clean Ge 2 Offset: @004A       write only
Name: Gate and Delay Clean Ge 3 Offset: @004C       write only
Name: Gate and Delay Clean Ge 4 Offset: @004E       write only
Name: Gate and Delay BGO 1      Offset: @0050       write only
Name: Gate and Delay BGO 2      Offset: @0052       write only
Name: Gate and Delay BGO 3      Offset: @0054       write only
Name: Gate and Delay BGO 4      Offset: @0056       write only
Name: Gate and Delay User Def 1 Offset: @0058       write only
Name: Gate and Delay User Def 2 Offset: @005A       write only
Name: Gate and Delay User Def 3 Offset: @005C       write only
Name: Gate and Delay User Def 4 Offset: @005E       write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<msb-------Delay-----------lsb>|<msb--------Width----------lsb>|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
delay = 0 to 2us  (7.9ns/step)
width = 0 to 3.2us (12.6ns/step)
delay starts when sumbus input first crosses programmed threshold
```

```
Name: Gate and Delay Logic FT1   Offset: @0060       write only
Name: Gate and Delay Logic FT2   Offset: @0062       write only
Name: Gate and Delay Logic FT3   Offset: @0064       write only
Name: Gate and Delay Logic FT4   Offset: @0066       write only
Name: Gate and Delay Logic FT5   Offset: @0068       write only
Name: Gate and Delay Logic FT6   Offset: @006A       write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<msb-------Delay-----------lsb>|<msb--------Width----------lsb>|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
Gate and delays for all 12 Front panel logic inputs.
FT logic inputs (@060 to @06A) use the following:
delay 0 to 2us  (7.9ns/step)
width 0 to 3.2us (12.6ns/step)
delay starts when input crosses threshold set by DAC at @0008


Name: Gate and Delay Logic Val1  Offset: @0070       write only
Name: Gate and Delay Logic Val2  Offset: @0072       write only
Name: Gate and Delay Logic Val3  Offset: @0074       write only
Name: Gate and Delay Logic Val4  Offset: @0076       write only
Name: Gate and Delay Logic Val5  Offset: @0078       write only
Name: Gate and Delay Logic Val6  Offset: @007A       write only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<msb-------Delay-----------lsb>|<msb--------Width----------lsb>|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Validation Logic inputs (@070 to @07A) use the following:
delay 0 to 9.7us (38ns/step)
width 0 to 9.7us (38ns/step)
delay starts when input crosses threshold set by DAC at @0008
```

```
Name: Analogue Multiplexing Control  Offset: @0080  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<-----------Spare------------->|AI2|Sel AI2 sig|AI1|Sel AI1 sig|
|   |   |   |   |   |   |   |   |on |  8:1 mux  |on |  8:1 mux  |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
AIx on bit:  1=analogue inspection line driven; 0= not driven
Select lines choose signal to be inspected:
000 Raw Ge sumbus                   100 Logic Threshold DAC output
001 Clean Ge sumbus                 101 TAC output
010 BGO sumbus                      110 spare
011 User defined sumbus             111 Sumbus test DAC output
```

```
Name: Digital Multiplexing Control   Offset: @0082  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|n/u|LI2|Sel Logic Insp 2 signal|n/u|LI1|Sel Logic Insp 1 signal|
|   |on |     64:1 multiplexer  |   |on |    64:1 multiplexer   |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
n/u = not used.
LIx on bit:  1= logic inspection line driven;  0= not driven
bits 0 to 5 and 8-13 define 1 of 24 signals to inspect.
The following Hex codes put the appropriate signal on insp line 1
(shift by 8 bits for insp line 2)
code       signal name
----       -----------
@48        Raw Ge sumbus threshold number 1 (set by @020) true/false
@49        Clean Ge sumbus threshold number 1 (set by @028) true/false
@4A        BGO sumbus threshold number 1 (set by @030) true/false
@4B        User defined sumbus threshold 1 (set by @038) true/false
@4C        Raw Ge threshold 1 output after gate and delay
@4D        Clean Ge threshold 1 output after gate and delay
@4E        BGO threshold 1 output after gate and delay
@4F        User def threshold 1 output after gate and delay
@50        Fast Trigger before gate and delay
@51        Fast Trigger after gate and delay
@52        Validation before gate and delay
@53        Validation after gate and delay
@54        Inhibit Action after gate and delay
@55        Start Validation signal after gate and delay
@56        Front panel stop (to TAC)
@57        Start conversion (TAC ADC)
@58 to @ 5f not used
@60        Fast Readout AM code recognised
@61        VME address strobe
@62        Readout* (VXI backplane signal) Used in fast readout.
@63        Noneleft (MT has no data left to be read for current event)
@64        Maxclock (MT data readout control signal)
@65        Pass signal (used in fast readout: next module may send data)
@66        Write pulse into Readout FIFo
@67        Trigger Readout (1= readout of trigger card)
Other codes are not used (ie there are 40 unused signal addresses)
```

```
Name: Card Control Register  Offset: @0084  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|RDO|dis|rst|mde|lst|tst|prg|clr|val|val|o/p|o/p|o/p|o/p|o/p|o/p|
|mde|LCA|LCA|LCA|crd|   |LCA|scl| 1 | 0 |TAC|typ|sb3|sb2|sb1|sb0|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
 Cleared (@0000) on powerup.
bit   meaning
---   -------
 0    On/off Raw Ge sumbus multiplicity                 (1=on, 0=off)
 1    On/off Clean Ge sumbus multiplicity               (1=on, 0=off)
 2    On/off BGO sumbus multiplicity                    (1=on, 0=off
 3    On/off User defined sumbus multiplicity           (1=on, 0=off)
 4    On/off Fast Trigger and Validation type       (1=output, 0=don't output)
 5    Output Trigger's TAC word                     (1=output, 0=don't output)
 6    Select Validation line bit 0 (00=not used, 01=Val 1, 10=Val 2, 11=Val 3)
 7    Select Validation line bit 1 (00=not used, 01=Val 1, 10=Val 2, 11=Val 3)
 8    Clear all scalers on the card                         (0=clear, 1=count)
 9    Program trigger logic LCA          (0 to 1 transition (re)programs LCA)
10    Put card in test mode                                 (1=test, 0=normal)
11    Lastcard (switch in terminators)                    (1=last card, 0=not)
12    LCA mode                                             (1=master, 0=slave)
13    LCA reset                                            (1=reset, 0=normal)
14    Disable LCA                                        (1=disable,0=normal)
15    Readout Mode                          (1=VME LWord reads, 0=Fast Readout)
```

```
Name: System Control Register  Offset: @0086   read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|fif|<- Spare ----->|s/u|s/u ext|s/u|s/u|xfr|end|Par|Go |trg|clr|
|rst|   |   |   |   | 1 | 0 |dly|TAC|CFD|scl|r/o|CDT|stp|syn|   |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

 Cleared (@0000) on power-up
bit   meaning
---   -------
 0    Level of VXI Clear line                           (1= clear, 0=normal)
 1    Level of VXI Trigger Sync Pulse line           (1=sync on, 0=sync off;
                                                      active on 0 to 1 edge)
 2    Level of VXI Go/Stop bit                                (1=Go, 0=Stop)
 3    Common Deadtime or Parallel/Pipelined mode. (1=Parallel/Pipelined 0=CDT)
 4    Select source for 'Readout Complete' in CDT      (1=Coding, 0=Readout)
 5    Transfer scalers to shadow register            (1= transfer, 0=normal;
                                                      active on 1 to 0 edge)
 6    Enable Trigger TAC and bypass FT LCA                     (1=on, 0=off)
 7    Setup Ge TAC                                             (1=on, 0=off)
 8    Enable External delay                          (1=enabled, 0=disabled)
 9    Select Sumbus for CFD setup (bit 0)        (00 = raw Ge, 01 = clean Ge)
 10   Select Sumbus for CFD setup (bit 1)        (10 = BGO,    11 = user def)
11-14 Spare (5 bits)
 15   Reset readout and inter-LCA FIFOs [VXIGO must be OFF] (1=reset 0=normal)


Name: FTR Prescaler Register         Offset: @0088  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|n/u|<- FTR 4 ->|n/u|<- FTR 3 ->|n/u|<- FTR 2 ->|n/u|<- FTR 1 ->|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
000 divide by 1
001 divide by 2
010 divide by 4
011 divide by 8
100 divide by 16
101 divide by 32
110 divide by 64
111 divide by 128
```

```
Name: Scaler Control Register        Offset: @008A  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|TST|FTR|FTR|FTR|FTR|Val|n/u|FT |   |   |   |   |   |   |   |   |
|   |4  |3  |2  |1  |   |   |   |<---------- Not Used --------->|
|<----- Enabled/Disabled -----> |   |   |   |   |   |   |   |   |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
0 = Disabled     1 = Enabled
(bottom 8 bits no longer used: were used on protypes)
```

```
Name: Raw Ge Multiplicity ADC (test only)  Offset: @008C  read only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: Clean Ge Multiplicity ADC (test only)  Offset: @008E  read only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: BGO Multiplicity ADC (test only)  Offset: @0090  read only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: User def Multiplicity ADC (test only)  Offset: @0092  read only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |msb|   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: TAC Output (test only)   Offset: @0094  read only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: FTR and VAL request (test only)   Offset: @0096  read only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<---------- Not Used -------->|val|val|val|val|ftr|ftr|ftr|ftr|
|   |   |   |   |   |   |   |   | 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: Status register (error reporting) Offset: @0098  read only

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
|<----- Scaler Overflow ------->|LMs|Inh|VXI|ROC|RDO|FIF|FIF|FIF|
|   |FTR|FTR|FTR|FTR|Val|   |FT |not|Act| go|O  |seq|O  |O  |O  |
|TST|4  |3  |2  |1  |   |n/u|   |prg|   |   |enf|ERR|MPT|FUL|ERR|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

Normally the status register will be @0000 unless an error is reported.
Bit cleared automatically when fault is fixed (e.g. by clearing scaler)

 Bit      Meaning
 ---      -------
 0        FIFO Error (0=OK, 1=error) (Remains set until FIFO reset)
 1        Readout FIFO Full* (0=full, 1=not full)
 2        Readout FIFO Empty* (0=empty, 1=data available)
 3        Readout Sequence error  (1=error, 0=OK) (Remains set until FIFO rst)
 4        ROCO Event Number Fault (1=ROCO reading wrong event, 0=OK)
                                  (Remains set until FIFO reset)
 5        VXIGO (1=VXI active, 0=VXI stopped)
 6        Inhibit Action (1=active, 0=not active)
 7        Logic modules not programmed (0=not both programmed, 1=OK)
8,10-15   Scaler Overflow indication.
 9        not used (always 1)
```

```
Name: Fast Trigger Pulse Scaler          Offset: @00A0   read only
                                                         Longword Only

31                                                            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|msb                                                         lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: Validation  Scaler                   Offset: @00A8   read only
                                                         Longword Only

31                                                            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|msb                                                         lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: FTR1  Scaler                       Offset: @00AC   read only
                                                         Longword Only

31                                                            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|msb                                                         lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: FTR2  Scaler                       Offset: @00B0   read only
                                                         Longword Only

31                                                            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|msb                                                         lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: FTR3  Scaler                       Offset: @00B4   read only
                                                         Longword Only

31                                                            00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|msb                                                         lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: FTR4  Scaler                      Offset: @00B8   read only
                                                         Longword Only

31                                                           00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|msb                                                       lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+


Name: Diagnostic Scaler (for Testing)   Offset: @00BC   read only
                                                         Longword Only

31                                                           00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|msb                                                       lsb|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+


Name: Raw Ge Sumbus parameter address   Offset: @00C0  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: Clean Ge Sumbus parameter address   Offset: @00C2  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: BGO Sumbus parameter address        Offset: @00C4  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
```

```
Name: User defined Sumbus parameter address  Offset: @00C6 read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: TAC parameter address   Offset: @00C8  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: FT and Val req parameter address   Offset: @00CA  read/write

 15  14  13  12  11  10  09  08  07  06  05  04  03  02  01  00
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
| 0 | 0 |msb|   |   |   |   |   |   |   |   |   |   |   |   |lsb|
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+


Name: Event Number (load counter)      Offset: @00CC  read/write

15                              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|<--16 bit hardware event no.-->|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
Access in test mode only.


Name: Event Header      Offset: @00CE  read/write

15                              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|<---Header Reg Default=0000--->|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
```

```
Name: Event data FIFO (test only) Offset: @00D0   write only
                                                         Longword Only

31                              15                              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|<--- Don't care (not used) --->|<---------- Data ------------->|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
Writes to this address are only successful in test mode and with
VXIGO true If false, the logic sees the fifo as full and doesn't
do the write. This is very  useful in normal operation, but a pain
for testing! (Only safe thing to do is to disable all the sumbuses
and the LCA first before setting VXIGO.) NB 16 bits of data, but
must be longword access.
```

```
Name: Event data FIFO (test only) Offset: @00D4   read only
                                                         Longword Only

31                              15                              00
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
|1|1|<---Parameter Address----->|<---------- Data ------------->|
+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+-+
The parameter address is added by the readout mechanism, so the
longword read will only give 16 bits which the programmer can
directly control. The read is intended for diagnostic testing only.
```

```
Name: Trigger Logic module Program (2x8Kb) Offset: @1000 to @2FFE
                                              and  @3000 to @4FFE
(Format defined by XILINX LCA software. Eurogam software must load
 the data file it receives from XILINX software into VXI memory,
 starting at address @1000,then set LCA mastermode bit to initiate
loading of the LCA's)
```

End of document