EDOC035

EUROGAM PROJECT

NSF DATA ACQUISITION SYSTEM

Eurogam VXI line use

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NSF Electronics Development Group
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Daresbury Laboratory

Eurogam VXI lines their sources, destinations, and path through the RM

Patrick Coleman-Smith

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1 Introduction

This document describes my understanding of the current specifications for the use of the VXI lines during the EUROGAM collaboration. REF *'Utilisation des Lignes VXI'* Alphonse Richard 13/7/90 , and *'Eurogam VXI line usage'* Ian Lazarus July 1990.

I intend to list the type (analogue, ECL, TTL), source, destination, disconnected state at the VXI backplane (i.e. when it is not driven from its source), and how it is affected by passage through the RM card to and from the backplane.

I hope this will allow all those concerned to be able to ensure that their specification/requirements are being met.

In the following text RM refers to the resource manager VXI module being manufactured by STRUCK for the EUROGAM collaboration.

P2 refers to the sub-module in the RM which buffers the VXI lines on the 2nd of the 96-way backplane connectors.

P3 refers to the sub-module in the RM which buffers the VXI lines on the 3rd of the 96-way backplane connectors. P3 also acts as support for the Fast ADC sub-module being developed by Ch.Ender.

All ECL logic referred to is 10K.

2 VXI lines

2.1 Local Bus

- LBUS0 Supplementary analogue sumbus 1 .
  Type: Analogue.
  Source : Ge/BGO card onto the backplane. Destination : Master Trigger
  Via: RM P2 card buffer to a front panel single pin (size 00) LEMO. No inversion. Buffer is an AD9617.

- LBUS1 Supplementary analogue sumbus 2 .
  Type: Analogue.
  Source : Ge/BGO card onto the backplane. Destination : Master Trigger
  Via: RM P2 card buffer to a front panel single pin (size 00) LEMO. No inversion. Buffer is an AD9617.

- LBUS2 Analogue inspection line 1
  Type: Analogue.
  Source: Any VXI card onto the backplane. Destination: Front panel (size 00) LEMO or fast ADC.
  Via: RM P2 card buffer to a front panel (size 00) LEMO or Fast ADC daughter board. Buffer is LH0033. No inversion.

- LBUS3 Analogue inspection line 2
  Type: Analogue.
  Source: Any VXI card onto the backplane. Destination: Front panel (size 00) LEMO or fast ADC.
  Via: RM P2 card buffer to a front panel (size 00) LEMO or Fast ADC daughter board. Buffer is LH0033. No inversion.

- LBUSA4 RENin LBUSC4 RENout (Readout ENable daisy chain)
  Type: TTL.
  Source: RM. (any readout controller will be down the daisy chain.) Destination: Data source card in VXI (BGO, Ge, Master Trigger).
  Via: This is set/cleared from a register in the RM slave. It is intended for signalling VME readout by the RM. TTL signal cleared to logic 0 at power-up.

- LBUS5 Voltage inspection line
  Type: Analogue.
  Source: VXI backplane. Destination: Front panel (size 00) LEMO and slow ADC on RM P3.
  Via: RM P2 card buffer . No inversion. Buffer is an INA101M.

- LBUS6 Contrôle des fenêtres
  Type: Analogue.
  Source : Ge/BGO card onto the backplane. Destination :Front Panel (size 00) LEMO.
  Via: RM P2 card buffer to a front panel single pin (size 00) LEMO. No inversion. Buffer is an AD9617.

- LBUS7 not allocated

- LBUS8 Event Number bit 1.
Type: Externally differential ECL , backplane single ended ECL.
Source: Master Trigger. Destination: All data source cards, and Readout Controller.
Via: RM P2 and P3 cards. Received at the RM as differential ECL into a removable 100Ω termination. Connector is 40 pin IDC. Buffered by MC10116 on P3 card to MC10101 on P2 which drives the signals onto the backplane. The backplane is monitored by a MC10115 on P2 which drives an MC10116 on P3. This drives differential output to a 40 pin IDC connector. There are no inversions in the buffering. When disconnected the bias resistors on the differential input lines produce a logic 0 at the backplane.

- LBUS9 Event Number 2
See LBUS8 for information.

- LBUS10 Event Number 4
See LBUS8 for information.

- LBUS11 Event Number 8
See LBUS8 for information.

- LBUS12 Reserved (Anti-Compton veto in Eurogam)

- LBUS13 Reserved (Anti-Compton veto in Eurogam)

- LBUS14 Reserved (Anti-Compton veto in Eurogam)

- LBUS15 Reserved (Anti-Compton veto in Eurogam)

- LBUS16 Reserved (Anti-Compton veto in Eurogam)

- LBUS17 Reserved (Anti-Compton veto in Eurogam)

- LBUS18-35 not allocated.

2.2 ECLTRG 0-5

- ECLTRG0 Validation 1
Type: Externally differential ECL, backplane single ended ECL.
Source: Master Trigger. Destination: Any VXI card participating in an event.
Via: RM P2 and P3 cards. Received as Differential ECL into a removable 100Ω terminator. Connector is 40 pin IDC. Buffered by MC10116 on P3 card to MC10123 on P2 to drive the backplane. MC10123 enabled by setting an 'enable triggers' bit in Slave register. Backplane monitored by MC10116 with protection as per figure B.10 in the VXI specification revision 1.3. This passes to P3 where it is driven off the board by an MC10116 as differential ECL to a 40 pin IDC connector. There is no inversion through the RM. When disconnected the bias resistors on the input produce a logic 0 at the backplane.

- ECLTRG1 Synchronisation of triggers for test mode.
  Type: Externally differential ECL, backplane single ended ECL.
  Source: Master Trigger. Destination: Any VXI card participating in a test event
  Via: RM P2 and P3 cards. See ECLTRG0 for information.

- ECLTRG2 Inhibit (D size)
  Type: Externally differential ECL, backplane single ended ECL.
  Source: Master Trigger or RM. Destination: Any VXI card in the crate, and the Master Trigger. *It has been suggested that this provides a method of stopping acquisition temporarily to allow software access to sensitive registers in VXI data acquisition cards. This will be a modification to the RM prototype.*
  Via: RM P3 card. See ECLTRG0 for information.

- ECLTRG3 Logic inspection line 1
  Type: Externally differential ECL, backplane single ended ECL.
  Source:Selected VXI card, BGO, Ge etc. Destination: RM front panel (size 00) LEMO for monitoring, and FADC.
  Via: RM P3 card. Backplane monitored by MC10115 with protection as per figure B.10 in the VXI specification revision 1.3. This is driven off the board by an MC10192 as single ended ECL to a (size 00) LEMO connector. There is an inversion through the RM.

- ECLTRG4 Logic inspection line 2
  Type: Externally differential ECL, backplane single ended ECL.
  Source:Selected VXI card, BGO, Ge etc. Destination: RM front panel (size 00) LEMO for monitoring, and FADC.
  Via: RM P3 card. See ECLTRG3 for information.

- ECLTRG5 Validation 2
  Type: Externally differential ECL, backplane single ended ECL.
  Source: Master Trigger. Destination: Any VXI card participating in an event. Via: RM P3 card. See ECLTRG0 for information.

2.3 TTLTRG 0-7

All the following TTL trigger lines have common buffering through the RM. They are received as differential ECL with removable 100Ω terminators , and jumpers to select for single ended input with the inverting input pin terminated at ground. The input signals are converted to TTL by MC10125s and passed to P2 where it is buffered by a 74ALS641 to drive the backplane. All signals will be logic 1, except TTLTRG4 which will be Logic 0, when disconnected.

The backplane is monitored by a 74ALS645 which buffers the signals from the back plane on the P2 card onto the P3 card. There it is converted into differential ECL by MC10124s and driven off the RM via a 40 pin IDC connector. There are jumpers to change this to single ended ECL with the inverting output connector pin tied to ground.

- TTLTRG0 End of coding
  Source: All VXI cards forming part of a readout daisy chain. Destination: Master Trigger.

- TTLTRG1 End of readout
  Source: All VXI cards forming part of a readout daisy chain. Destination: Master Trigger.

- TTLTRG2 Transfer all scalers to shadow registers. Not used in EUROGAM - only the Master Trigger has scalers.
  Source: Master Trigger. Destination: All VXI cards participating in Data acquisition.

- TTLTRG3 Clear
  Source: Master Trigger. Destination: All VXI cards participating in Data acquisition.

- TTLTRG4 Go/Stop.
  Source: Master Trigger. Destination: All VXI cards participating in Data acquisition.

- TTLTRG5 Event reject.
  Source: Unknown. Destination: Unknown.

- TTLTRG6 Validation 3 .
  Source: Master Trigger. Destination: All VXI cards participating in Data acquisition.

- TTLTRG7 Inhibit (C size).
  Source: Master Trigger or RM. Destination: Any VXI card in the crate, and the Master Trigger. *It has been suggested that this provides a method of stopping acquisition temporarily to allow software access to sensitive registers in data acquisition cards. This will be a modification to the RM prototype.*

2.4 STAR lines

- STARX Fast trigger
  Type: Differential ECL.
  Source: Master Trigger. Destination: Ge and BGO cards.
  Via: RM P3 card. The input is jumper selectable between two buffers, one is a differential signal from the 40 pin IDC connector, MC10116, when disconnected gives logic 1 at backplane; and the other is single ended ECL from a single pin (size 00) LEMO, MC10116, when disconnected gives logic 0 at the backplane. The selected buffer drives the MC10E111 low skew differential drivers for the backplane. There is an inversion as the signal passes through the RM.

- STARY Fast trigger
  Type: Differential ECL.
  Source: Any card on VXI backplane (Ge,BGO etc.). Destination: Master Trigger.
  Via: RM P3 card. The individual backplane lines are buffered onto P3 with MC10116s wire ORed in three groups to the inputs of an OR gate. The differential output is buffered off the board by an MC10116 to the 40 pin IDC connector, and as a single ended signal buffered by a MC10192 to a single pin (size 00) LEMO connector. There is an inversion as the signal passes through the RM.

2.5 Sumbus

- SUMBUS.
  Source : Ge/BGO card onto the backplane. Destination : Master Trigger
  Via: RM P2 card buffer to a front panel single pin (size 00) LEMO. No inversion. Buffer is an AD9617.

2.6 Other Lines

All lines in this section are as defined in the VXI specification

- CLK10
  Type: Differential ECL at the backplane.
  Source: Derived from CLK100 by division. Destination: VXI backplane.
- CLK100
  Type: Differential ECL at the backplane.
  Source: 200Mhz oscillator on the RM , or via a single ended ECL buffer from a front panel (size 00) LEMO. Destination: VXI backplane.
- SYNC100
  Not implemented.
- MODID(00-12)
  Driven from the RM as per specification.