Ge Card Specification (UK version)

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1 Introduction

This document records the current UK understanding of what will be in the Eurogam Ge card and how it will fit into the system.

2 Overview of Ge card

The Ge card may be split into several different functional blocks which may in turn be subdivided. Each functional block will be described in its own section with subsections for each component. Figure 1 shows an overview of the card in simple block diagram format with some detail included in one Ge channel.

- Analogue Pulse Processing
  - Receiver and buffer
  - Shaping Amplifier
  - Peak Detect and Hold
  - Timing Filter Amplifier (TFA)
  - Constant Fraction Discriminator (CFD)
  - Time to Amplitude Converter (TAC)
- Digitization
  - ADC
  - Sliding scale correction and serial to parallel conversion
- Readout
  - Channel Readout
  - Card Readout
- Local Trigger
- Diagnostics and Testing Facilities

In brief, the Eurogam Ge card works as follows. It accepts analogue inputs from Ge preamplifiers and produces 4 digitized outputs per input: three energy outputs (low and high gain and very high gain) and one timing output derived from the Ge input relative to a a common signal. The outputs are only produced if a user defined global trigger condition is satisfied and so the Ge card sends information to and receives trigger signals from the system's central trigger unit. The digitized data are transferred to the crate readout controller after each event. Each Ge card will handle 5 Ge channels (i.e. 15 energy outputs and 5 timing outputs).

3 Analogue Pulse Processing

This is the section of the card which deals with the preamplifier input signal. It is the most noise sensitive in the card because of the low signal levels (typical preamplifier signal is around 100 mV for a 2 MeV gamma ray). The receiver circuit buffers the preamplifier input to the shaping amplifiers and the TFA for energy and timing respectively. The shaping amplifiers are followed by the peak detect and hold circuit which holds the analogue input for the digitizing section of the card. The TFA is followed by the CFD and the TAC from which timing information is available. *Cumulative error must be so low that accuracy through the whole energy chain will be at least 13 bits; i.e. better than Ortec 571 shaping amplifier! We should use a 'sum of squares' approach to calculating errors since presumably the errors are independent in sign and magnitude although they will propogate through the system from one stage to the next.*

3.1 Receiver and buffer

The receiver circuit is implemented in a hybrid. It will accept either unbalanced differential signals or a single ended signal (with the second input grounded).

3.2 Shaping Amplifier

3.2.1 Semi Gaussian shaping on the VXI card

The shaping amplifiers will provide semi-gaussian shaping with rise time approximately 2.2τ and width at baseline of 3 times the rise time. The value of τ will be fixed during design between absolute limits of 0.25μs and 10μs. The shaping will take place in 2 stages; first a gain stage and then a shaping filter stage. The filter element is a 3 stage filter (i.e. 6 integrations) and there will be another integration in the BLR circuit. Gain will be fixed in each amplifier so there will be three possible energy ranges:

- Low Gain: 20 MeV with resolution of 2.5 keV.
- High Gain: 4 MeV with resolution of 0.5 keV.
- Very High Gain: 800 keV with resolution of 100 eV.

It is not clear that the very high gain (800 keV) range can be implemented in a VXI card because of background noise level. The 20 MeV and 4 MeV ranges will be implemented first in order to gain experience of amplifiers in VXI on which a decision about the 800 keV range can be based.

The only controllable parameter is PZ adjustment which is performed under software control using a DAC while monitoring the bottom part of the pulse from the gain stage (diode limited) on an oscilloscope (see section 7). By controlling the preamp decay time constant to $\pm 2\%$ we should be able to use only a small PZ adjustment range using a DAC and FET (or analogue multiplexer) circuit. It is intended that BLR adjustment will not be necessary. (NOT auto adjustment but no adjustment.) Auto BLR will, however, be provided if tests prove it to be necessary.

The amplifier will be implemented using surface mount components.

3.2.2 External Gated Integrator

It is agreed that in the first Eurogam phase there is not sufficient time to develop either ballistic deficit correction or a gated integrator circuit. It is, however, necessary to use one of these techniques to obtain acceptable peak shape and width from large coaxial Ge detectors. As an interim solution it will be possible to bypass one of the shaping amplifier stages by cabling through[1] an external NIM module such as the Ortec 973 gated integrator. This will also allow the coverage of the 800 keV range externally should it prove difficult to achieve in VXI. The external input will be connected to the peak detection circuit of the very high gain energy channel via a switching mechanism. It would not replace the 4 MeV or 20 MeV ranges unless it is decided to save space by changing back to the original 2 energy channel proposal, in which case the external GI/800 keV input would be connected into the low gain (20 MeV) peak detect circuit.

Note that the ADC expects a 3V input whereas the Ortec 973 (and most other NIM shaping modules) generate a 10V output (full scale) which would drop to 5V using a series/shunt terminated cable from the GI to the VXI card. An attenuator is, however, still required at some point between the external input and the ADC.

Controllable parameters are determined by the functionality of the external amplifer or gated integrator. For example the Ortec 973 provides switches for:

- Integration time: selection of 2.5μs or 5μs.
- Gain: continuously variable from x 1.25 to x 375[2].
- PZ adjustment for preamp decay time constants from 40μs to ∞.
- PZ adjust/GI output selection switch.
- Switches for input polarity and normal/differential inputs.

3.3 Peak Detect and Hold

A surface mount circuit which might be hybridized. It follows the pulse shaping output and holds the peak value for use by the ADC. It starts tracking the shaped signal when the CFD fires and stops just before the channel control logic indicates that the ADC should begin conversion.

[1] This requires that the preamplifier has two outputs; one for the GI and the other for the VXI Ge card's receiver stage which must still provide triggering and timing information.

[2] With preamplifier sensitivity of 50mV per MeV, a gain of 1.25 means that a full scale 10V output represents 160 MeV(!), and with a gain of 375 full scale represents 500 keV. This means that the 973 can also cover the 800 keV range requirement.

3.4 Timing Filter Amplifier (TFA)

The TFA will be made in two different versions (both using SMT) to cope with either stacks or coaxial detectors. The difference will be in the preset time constants for integration and differentiation (10ns integration and 100ns differentiation are the current 'best guess' for coaxial detectors). The gain will be fixed; for a 50mV/MeV pre-amp the gain will be X10. The output will be a maximum of 5 v into 100Ω. The amplifier must be linear over the range 0 to 10 MeV. Above 10 MeV the amplifier may be allowed to saturate because the CFD works on the bottom 2 MeV only. The limiting factor in the saturation is the recovery time. There are no controllable parameters in the TFA[3]. To change the time constants it is necessary to change the whole TFA element.

3.5 Constant Fraction Discriminator (CFD)

The CFD delay is fixed. Two versions of the CFD will be produced to match the two versions of the TFA. The dynamic range requested by physicists of 1000:1 is not achievable[3]; a realistic figure is 300:1 which would cover the range 20 keV to 6 MeV with good timing, and would distort signals over 6 MeV by saturating. The design will not include slow rise time rejection and will be implemented in surface mount technology.

There will be several programmable parameters associated with the CFD:

- Threshold (12 bit DAC = 4096 steps, each step 0.5 keV over range 20 keV to 2 MeV) *12 bits is a revision to the specification suggested at March meeting.*
- Pulse Width (8 bit DAC = 256 steps over range 0 to 255ns in 1ns steps)
- Output Delay for time alignment of pulses. (8 bit DAC. 0 to 100ns in 0.5ns steps.)

3.6 Time to Amplitude Converter (TAC)

The TAC range is 0 to 2μs with a precision of 1ns. There is also a shorter 200ns range which may be selected by changing an external capacitor (using an on-board switch). This might be useful for short lived isomers. The TAC accepts start and stop inputs of $\geq$5ns. If it receives a start and no stop it will clear itself when it goes overrange. It also accepts a reset input with pulses $\geq$10ns.
Start will be a fixed input from the CFD pulse.
Stop will be a fixed input from the front edge of the fast trigger pulse[4].

Note that the present trigger specification allows for a worst case channel to channel skew of 5ns in the fast trigger signal (TAC stop). Within a single channel the successive pulses will all arrive with exactly the same delay relative to the generation of the fast trigger pulse so there is no variation with time, only from detector to detector. The effect would only be seen when superimposing spectra and would not have any effect on the shape of any single time spectrum. The channel to channel skew comes from the crate backplane, from the board to board variation and from cables which are not matched exactly. It could be reduced by a

[3] A recent suggestion is that there could be a software switchable x 1 or x 5 gain selection to overcome the dynamic range problems in the CFD.

[4] There is also a suggestion that we use the fast trigger as a common start, and a delayed version of the CFD pulse (the back edge of the local trigger acceptance window) as the stop. See local trigger section for timing accuracy.

small programmable delay in the slot 0/RM card which distributes the trigger within a crate. *Is this a problem? If so, why and what skew would be acceptable?*

The implementation is in a Thompson ceramic resistor/transistor array.

4 Digitization

Implementation is intended to be on a hybrid combining ADC, sliding scale DAC and adder, and serial to parallel chip.

4.1 ADC

All ADCs throughout the system on Ge and BGO cards will be identical. Each Ge channel will have 4 ADCs; 3 for energy and one for timing. The chosen ADC is the Burr Brown PCM78P 16 bit successive approximation ADC. Its input range is ± 3v, but it is intended to use only the positive half of this range. The ADC will not be required to work to 16 bits of accuracy; the two lsbs will be discarded, leaving 14 bits of data. The PCM78P has no internal sample and hold stage, so the voltage for conversion must be held externally; in this system it will be in the Peak Detect and Hold circuit (section 3.3). The ADC converts in under 5μs using the internal clock, and may be made to convert faster using an external clock which would also synchronise all the ADCs in a crate. The ADC output is serial (MSB first), and emerges as it is generated during conversion. There are no controllable parameters in the ADC.

4.2 Sliding scale correction and serial to parallel conversion

The serial to parallel conversion of ADC output and most of the sliding scale circuit are implemented in the same ASIC, each chip handling 8 ADCs with a common sliding scale counter. *Is 8 the best number of ADCs to handle in a single chip? What about 10?* The chip also provides programmable digital upper and lower thresholds. These can be used to select certain energy or time ranges, and maybe could remove a channel from readout if the TAC indicated the detection of a neutron rather than a γ-ray? The sliding scale counter and digital subtraction stages are in the ASIC and it provides a serial output to the external DACs generating the analogue value to be added to the ADC input.

5 Readout

5.1 Channel Readout

Channel readout involves the reading of all ADCs on the board via the serial/parallel conversion ASICs, using the on chip windows to perform an expanded type of 'zero suppression' to remove empty channels and channels outside the programmable digital window. These data will be available for diagnostic purposes via VME the ADC being selected by VME address. Channel readout takes place under the control of the local trigger section of the Ge card.

5.2 Card Readout

Data from ADCs is matched up with 2 qualifier bits (pileup indication) and a 14 bit ADC identifier to form a set of 32 bit words held in a FIFO. The FIFO is accessible from VME and maybe also from the VXI local bus depending on discussions currently taking place. Card readout is initiated by the central trigger unit via a readout controller in each crate.

6 Local Trigger

This is the section of the channel which controls its operation. It contributes to the formation of the global fast trigger decision and acts on the results. It also detects and signals pileup.

Timing will be performed using a ramp generator started by the CFD over a range up to $10\mu s$. Timing points will be defined by DAC/comparator combinations using 10 bit accuracy to resolve down to 10ns. Note that the $10\mu s$ range limits the time we can wait for validations. The system trigger specification allows this time to be as long as required at the expense of deadtime, but this implementation of the Ge card will limit it to $10\mu s$. *The $10\mu s$ limit comes from the comparator having a 5V range and 5mV sensitivity which defines a 10 bit range. We can then choose to run for $5\mu s$ with 5ns steps (too short), $10\mu s$ with 10ns steps (the selected mode of operation) or longer than $10\mu s$ with coarser resolution (not worthwhile to degrade step size to cater for tiny fraction of experiments).*

For Compton Suppression the Ge card must supply a CFD output pulse for each Ge channel (i.e. 5 ouputs) via the front panel for connection to an anti-Compton decision module. Anti-Compton processing is explained more fully in a separate document. For other 'user triggers' the Ge card should also provide Leading Edge discriminator outputs for each Ge channel.

7 Diagnostics and Testing Facilities

Monitoring points will be switched to a VXI local bus line for observation on an oscilloscope. One of the following signals from any channel may be selected by software:

- Shaping amplifier gain stage output (clipped) for PZ adjustment.
- Output from shaping amplifier filter stage.
- CFD output
- TFA output
- TAC output

There will also be a test input, isolated by a relay, which provides pulses to the receiver hybrid in place of a preamplifier. These pulses could be generated either by a transistor chopper circuit or derived from the backplane 10 MHz clock and a divider. The latter solution has the advantage that it lines up all test inputs in time provided all dividers start to count from the same clock pulse.

8 Setup

Setup will be described in a separate document. The Ge card must provide facilities to allow matching of time and gain between detectors, both within a card and from card to card.

9 Setup of Ge cards

9.1 Programmable Parameters

- Pole zero adjustment: 8 bit DAC (1 per channel)
- CFD threshold: 8 (or 12) bit DAC (1 per channel)
- CFD Output delay: 8 bit DAC (1 per channel)
- CFD width adjust: 8 bit DAC (1 per module)
- Test generator: 16 bit DAC (1 per module)
- ADC low window: separate address (4 per channel)
- ADC high window: separate address (4 per channel)
- Channel inhibit: separate address (Full word per channel)
- Channel enable: separate address (Full word per channel)
  (*Why isn't this the same address as channel inhibit with different data?*)
- Test enable: separate address (Full word per module (or channel?))
- Test disable: separate address (Full word per module (or channel?))
  (*Why isn't this the same address as test enable with different data?*)
- ADC Identifier: separate address (4 per channel)
- Local trigger parameters (all are comparator inputs to generate timings by comparing DAC output voltage with timing ramp voltage):
  - Fast trigger window end: 10 bit DAC (1 per module)
  - Validation window end: 10 bit DAC (1 per module)
  - Hold shaped signal and start conversion: 10 bit DAC (1 per module)
  - Start of Readout time: 10 bit DAC (1 per module)[5]

All these parameters will be readable, returning the same value as was written to them.

The Ge card will conform to the VXI configuration and communication register scheme as set out in section C of the VXI specification.

9.2 Other settings

The following settings may be adjusted by electronics support staff (**NOT** users):

- Link (or switch) to ground one side of receiver input to change from differential input to single ended.
- Link (or switch) to either internal shaping amplifer or external gated integrator from peak detect and hold circuit. *Maybe using relay contacts, controllable from software.*
- Link (or switch) capacitors to swap TAC range between 200 ns and 2 μs.
- Change TFA and CFD modules when changing between stack and coax detectors. (The front panel should clearly indicate which setting is in use.)

[5]May be derived from ADC EOC output or something similar without timing.

10 Mechanical and Electrical Specification

This section defines the electrical and mechanical interface for all signals which will pass through either the front panel or the VXI bus.

10.1 Mechanical Interface

- All VXI connections are fully defined mechanically in the VXI bus Specification and require no further definition.
- Front panel connectors are used for inputs from preamplifiers and external shaping amplifiers (GI) and for outputs from the CFDs used in anti-Compton logic and the LE signals for user triggers.
  - All signals from preamplifiers will come into the unit via BNC sockets, 2 per preamplifier (to allow differential operation). Total 10 BNC sockets. *Only 5 with BNC sockets floating instead of grounded. Is this useful/desirable?*
  - All Gated Integrator ouputs will come into the unit via BNC sockets, one per channel. Total 5 BNC sockets.
  - All front panel CFD and LE outputs will go through IDC ribbon cable connectors (e.g. 3M M50 system). Total one 34 way connector including 14 grounds and 10 differential signals.

10.2 Electrical Interface

All VXI signals will conform to the VXI bus specification. VXI Local Bus signals will be either single ended ECL or IEEE P1194 BTL (Futurebus) drivers except for the analogue monitoring line (section 7).

Analog sumbus will receive 1mA per active Ge channel (i.e. max 5mA per card).

Front panel CFD and LE outputs will be differential ECL.

Pre-amp inputs will be 1V max into 1200Ω. *This will give nearly 93Ω when connected in parallel with a 100Ω terminator to match 93Ω coaxial cable.*

11 Software Interface

Each board, i.e. 5 Ge channels, will occupy one VXI Logical Address. The board will provide configuration registers within the 64 byte area allocated to its Logical Address in accordance with the VXI specification.

The map of internal registers will be defined later. The setup parameters to be included will be found in section 9.1. In addition there will be 20 VME addresses (one per ADC) for diagnostic data readout and one VME address from which the card redout FIFO is accessible. There are over 100 VME addresses per board, so the offset register at 06_{16} will be used to point to the area of memory space containing the registers. *Should we put either commonly used registers or registers common to all 5 Ge channels in the device dependent register area of the 64 byte address space?*

The Ge boards will be Register based VXI devices. *Does anyone think they should be message based devices? Why? Dynamic configuration doesn't appear to be worth the extra complication either so is not planned.*