Eurogam Trigger System

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1 Introduction

This document relates only to Eurogam and will differ from the Euroball trigger specification in many places. The main difference is that the Eurogam trigger is not pipelined. It is intended that the Eurogam trigger system will be upgradeable to the full Euroball pipelined parallel system and the design will not hinder that upgrade unless it is absolutely necessary. The Euroball system will allow parallel event collection for non-overlapping events. It has not yet been decided whether the first implementation of Eurogam will allow a limited type of parallelism using common deadtime per card or whether the simpler common deadtime across the whole system is sufficient. This document will initially assume the common deadtime across the whole system which is simpler to implement. If the document or ensuing discussions demonstrate a need for some parallelism then a more detailed description and specification will be written. Finally, this document describes the trigger system and is not intended to fully define the master trigger logic unit which will be specified properly elsewhere.

I will include comments and notes (mainly to remind me about details) using this italic typeface to distinguish them from the trigger specification.

2 What is a trigger system?

The question in the title may sound elementary but I have discovered that different people mean different things by 'trigger'. I will explain here what I mean by the term trigger in this document.

The trigger system identifies and confirms the existence of an interesting physics event. The trigger in Eurogam will take place in two stages: the fast trigger and the validation. The fast trigger must happen before the Ge pulse shapers reach a peak, and the validation must happen after the fast trigger but before ADC readout.

The trigger system also defines the interaction of the modules which comprise the system with the fast trigger and the validation. Thus the trigger system requires certain behaviour of the Ge cards, the BGO cards and the readout cards.

2.1 Definitions

Trigger Signals generated by the master trigger logic as a result of a physics event to indicate that the event is to be collected by the data acquisition system. Trigger is a generic term which covers both fast and slow components (see below).

Fast trigger This signal has two uses: logical and timing. The timing use is that the front edge stops the TAC in each Ge or BGO channel which was started earlier by the CFD in that channel. The logical function is to confirm that the possible trigger denoted by the CFD firing is in fact part of an event which is to be collected.

Slow Trigger Validation of the fast trigger (see Validation).

Validation A signal generated by the master trigger logic after a trigger to indicate that another, slower, set of criteria has confirmed that this is a good event and is to be collected.

Deadtime The time taken by the system to process an input during which it is unable to distinguish or accept any further inputs.

Pileup A condition where the separation of pre-amp output pulses is less than the time taken for the pulse shaping circuit to return to its baseline.

3 Implications of Ge shaping method for Trigger Timing

There are two or three different proposals under discussion as to the method of shaping in the Ge cards. The two most important criteria in choosing between a semi-gaussian shaping, another new shaping function and a gated integrator are firstly Ge resolution (peak shape and width) and secondly throughput (how long does it take to get acceptable resolution). For the trigger system the second of these is obviously very important.

The shaped pulse should be available to the ADC within 5μs of the γ-ray interaction in the Ge. For semi-gaussian shaping this allows a time constant of 2μs which has a peaking time of 4.4μs. For a gated integrator we would use a time constant of 0.5μs which means that integration is complete after 5μs. The semi-gaussian shaping with a 2μs time constant would require some form of ballistic deficit correction to give acceptable resolution with a large HPGe coaxial detector. The gated integrator provides inherent ballistic deficit correction and would provide acceptable resolution with a 5μs processing period. The main difference, however, is the amplifer deadtime. The gated integrator is ready for its next input as soon as it has finished integrating (5μs) but the semi-gaussian amplifier has a long recovery time, typically around 13μs for τ=2μs. This is only recovery to 0.1%, 10 bits[1]!

It is clear that there is no advantage to be gained by implementing pipelining without using gated integrators since the semi-gaussian amplifier deadtime covers the time required for ADC conversion and readout anyway. It is also clear that using semi-gaussian amplifiers with such a long deadtime will reduce the array efficiency with or without pipelining since the amplifier deadtime leads to a singles deadtime in each channel of 16.5% and will reduce the multiparameter rate (fold 3 and above) by 3%.

The trigger system requires that the shaped signal is ready to be digitised after 5μs. It also requires that after 15μs (common deadtime) or 5μs (pipelined) that the shaping amplifier is ready to accept a new input. For the common deadtime system either amplifier type could meet these requirements, but for pipelining we must use the gated integrator.

4 Deadtime

For a fold of 3 or more in a 70 Ge system the coincidence rate is around 30 KHz, so the typical 15μs deadtime represents 45%. It is proposed that we will have a pipelined trigger

[1] Details of timing for semi-gaussian shaping taken from Ortec 571 data sheet.

system for the 70 Ge system which will reduce the deadtime to the 5μs pulse integration time which is only 15%. For common deadtime we need only consider a 45 detector system, hence a 20 KHz coincidence rate leading to a deadtime of 30%[2]. Deadtimes greater than 10-20% are undesirable because they alter the distribution of collected events by making it more regular, leading to non-Poisson statistics. Thus we must try to reduce our deadtime by using additional trigger criteria such as Compton suppression (factor of 3 rate reduction; 10% deadtime.). These are of little or no use if amplifier deadtime predominates and keeps the array dead after event rejection. Benefits in deadtime reduction by better triggering using such things as Compton suppression will not be seen without gated integrators.

Assuming that we use gated integrators and can reduce deadtime below the 13μs semi-gaussian recovery time, it is probable that the readout phase can be reduced below the original 5μs estimate presented at the February meeting. This could be achieved by releasing the system for a new event when all data are in the crate's readout controller and using the next event processing time (10μs) to transfer the data from readout controller to event builder. The readout time is then typically under 2μs since each crate reads in parallel, leading to 12μs deadtime. *Latest figure indicates 15KHz coincidence rate (with 25 parameters), so 15μs is now 22.5% deadtime. If the 15 μs can be reduced as indicated above by shortening conversion or readout phases to 12μs then we reach an acceptable 18% deadtime.*

5 Information used in a trigger decision

In gamma ray spectroscopy the primary trigger method is the multiplicity of coincident hits in Ge detectors. Secondary information will include the Compton suppressed multiplicity, recoil fragment identification, energy sum, beam pulse timing[3], additional detectors (BGO ball, charged particle ball, neutron wall, SUSAN) and other parameters specific to the experiment.

The primary timing task of the trigger system is to check the Ge multiplicity quickly and accurately with a well defined coincidence window.

6 Implementation

There are many possible methods of implementation and many questions arise such as whether the trigger system explicitly aborts unsuccessful events or relies on timeouts in the Ge cards, whether we use a centralised trigger or a distributed trigger system and how we calculate multiplicity.

The distributed versus centralised trigger discussion has major implications for upgrading the system to pipelined operation and so in order to make the system upgradable we will use a distributed trigger mechanism. (A distributed system is also essential for any parallelism in trigger handling.)

[2] It is also possible to reduce the deadtime by using an external clock on the PCM 78 ADCs. Dividing the CLK100 by 16 gives a 6.25 MHz clock and reduces conversion time from 5μs to 2.7μs, giving a 25% deadtime. It is not possible to reduce the deadtime any further without using gated integrators because of amplifier deadtime.

[3] NSF Linac produces beam bunches of sub-nanosecond width at a rate which is a sub-harmonic of 150 MHz, typically 9.375 MHz or 4.6875 MHz

6.1 Fast Trigger

A distributed trigger system means that the Ge/BGO channels must be self timing, defining their own trigger acceptance window timed from the moment the CFD fires. If no fast trigger pulse is received by the end of this window then the Ge/BGO channel will know that nothing interesting happened and it must reset itself. In practice this will mean that the Ge/BGO channel will not convert the shaped value. It is unlikely that a reset circuit can be provided in an accurate shaping amplifier, so the channel stays dead anyway until the shaping amplifier returns to baseline. The effect of the trigger on the energy part of the Ge/BGO channel is purely to allow or to prohibit conversion. It is used by the timing part of the Ge/BGO channel to time against the CFD firing for neutron rejection (or maybe some other purpose).

6.2 Validation

Once the fast trigger has been generated we are ready to consider the validation. Again the ADC has no reset input, so it not possible to save time by aborting in mid-conversion. It is possible that sometimes a validation decision could be made before the start of conversion, and in this case we can save time by aborting the event without conversion. The result of the validation decision will be either an event reject signal or the validation pulse. If the event rejection arrives after the start of conversion or the validate pulse does not match the timing defined by the validation acceptance window then readout will not take place following conversion.

6.3 Notes

At the first Eurogam meeting the decision was made that the Ge and BGO cards would not be pipelined so that analogue and digital processing would not take place concurrently on a card. The use of a distributed trigger requires that at least one programmable gate and delay circuit runs on each Ge and BGO card during pulse shaping. This violates the 'no digital during pulse shaping' principle if we use the obvious counter type gate and delays driven from the VXI 100 MHz clock and so some thought must be given to either programmable analogue timing or good noise suppression.

It is technically possible but philosophically unacceptable to generate all timing signals centrally for a common deadtime system. This would mean that the trigger system sent a pulse to Ge cards saying 'sample shaped pulse now', another saying 'begin conversion' and another to say 'begin readout'. BGO cards would require different timing because of different shaping and so a second set of signals would be required. This method does not permit upgrades to parallel or pipelined operation and so will not be used in Eurogam.

6.4 Very Slow Devices

The Euroball 'very slow trigger' concept (after readout) will not be supported in hardware by the Eurogam trigger system. It will, however, be possible to delay validation (and hence readout) to wait for these slow devices. This will obviously increase the deadtime and will not be a normal mode of operation, but the facility to delay will be provided. The delay will be covered by the programmable validation window and the end of the window acts as a timeout.

6.5 Readout

The trigger system will initiate readout by sending a pulse to every crate in the system and will receive an acknowledgement by way of a wired 'OR' signal from every crate. When readout is complete in a crate the readout controller for that crate releases its contribution to the wired 'OR' signal. The trigger system is told when the readout is complete by the final release of the wired 'OR' signal by the last crate and knows that the event is now complete and it may start looking for a new fast trigger.

As suggested in the deadtime section, the readout controllers can easily incorporate a single event buffer without any correlation problems. This will work without increasing deadtime as long as the data can be transfered out of all readout controllers to the event builder in under $10\mu s$, i.e. for typical 25 word event, 400ns/word. If the readout controller implements any more buffering the trigger system must use some technique such as distributed event counters (1 per crate, incremented by fast triggers) or broadcasting event number with fast trigger (*requires a lot of cabling!*) in order to correlate the different components.

6.6 Multiplicity

The obvious method for calculating the Ge multiplicity is to inject current on the VXI analog sumbus which is intended for exactly this type of usage. Each active CFD will cause the injection of a current of 1mA by its Ge channel for a programmable period. The same method may be used for BGO multiplicity if required, although Ge and BGO must be located in physically different crates. In systems where the Ge cards extend beyond a single crate (or for BGO multiplicity) it is necessary to buffer the analog sumbus via a cable to the trigger logic unit. For a 45 detector system and 5 Ge channels/card it will not be necessary to buffer the analog sumbus since the trigger control logic should be located in the Ge crate from crate space considerations. From the timing point of view it is also better to put the master trigger logic trigger card physically close to the Ge cards since Ge is slower than BGO.

6.7 Trigger logic decisions

There may be several possible trigger conditions, so the master trigger logic unit will have 2 (possibly 4 depending on space) logic modules operating in parallel on the trigger information for both fast trigger and validation. Inputs will be aligned in time and then fed in parallel to the logic modules. The exact capability of the logic module can vary with the application, the simplest being just combinational logic in an electrically erasable gate array, maybe with some sort of gate and delay circuit (or maybe a fixed monostable) on the output to fix the fast trigger/validation pulse width. More complex decisions can be made with additional gate and delay units for example to look for a recoil particle a fixed time after detecting a gamma ray interaction. The i/o specification, pinout, and programming method for the logic modules will be specified so that special units may be easily produced to cope with unusual trigger conditions. The fast trigger logic modules must produce an output to indicate whether or not validation is required, and if so which validation logic module is to be used. *Do we fix fast trigger-validation logic module pairings (simple); if not how do we know which validation to use without hardwiring connections - maybe 1 output for each validation logic module from fast trigger logic modules?*

6.8 Summary

The master trigger logic unit will comprise the sections described above:

- Analogue comparators with programmable thresholds for Ge and BGO multiplicity checks. (2 for Ge, one for BGO)
- Logic inputs with time alignment from two 16 input front panel connectors, 16 for fast trigger and 16 for validation. Also latched version of Ge multiplicity for use in validation. The front panel inputs will have many uses such as using beam timing pulses in trigger decisions or accepting a signal from the autofill to say that the dewars are being filled and so data acquisition should be temporarily halted to prevent the collection of data corrupted by microphonics.
- Logic modules to operate on time aligned logic inputs and generate fast trigger or validation signals. (Total 4, maybe 8, with half used for fast trigger and half for validation.)
- Infrastructure comprising bus interface logic, diagnostics etc.

7 Trigger System Signal Definitions

The following signals are passed within the distributed trigger system:

7.1 CFD analogue outputs

These signals are sourced by the Ge or BGO channels onto the VXI sumbus and used to count coincident hits on either the Ge channels or the BGO channels. Ge and BGO cards will be in separate VXI crates and will use separate VXI sumbuses. Each active channel sources 1mA for a programmable period which must be long enough to cover the worst case Ge-Ge skew time (typically 50-100ns) plus the comparator resolution period. These outputs, along with the response time of the master trigger logic unit, define the coincidence window. The signals are controlled from the Ge and BGO cards and must be aligned by a CFD output delay so that the only Ge-Ge skew is introduced by the charge transit times in the Ge detectors. The master trigger logic unit will fan in buffered versions of the VXI sumbus from all Ge crates to two comparators[4] and from all BGO crates to another comparator. The signal must be gated off in the Ge card as soon as pileup is detected. *Is this fast enough or do we need another pileup rejection system?* Buffered analog sumbuses are front panel inputs to the master trigger logic unit. The sumbus will be buffered in the Ge/BGO crate by the Slot 0/RM module (or perhaps the readout controller module).

7.2 Fast Trigger

This signal is generated by the master trigger logic unit in response to inputs according to a user defined set of checks and logic functions. Typically these checks would be only multiplicity, maybe in coincidence with some machine parameter such as beam bunching or polarization state. The signal must be sent over matched path lengths to all crates and distributed via the VXI STARX lines to every module. This means that it must be routed via the Slot 0/RM module in every crate. The first effect of the fast trigger (front edge) within

[4] To allow alternative trigger conditions. An example is the typical experiment in section 14

the Ge or BGO channel is to stop a TAC which was started when the channel's CFD fired, hence the need for good matching. Using star lines and matched cables means that the fast trigger arrives at all channels with a skew of under 5ns from channel to channel although pulse to pulse variation within a channel will be much less. (2ns STARX skew plus non-ideal cable matching and variation between Slot 0/RM cards). *Is this good enough?* The fast trigger also has the logical function in a Ge/BGO channel of including that channel within the event provided it arrives within the channel's fast trigger acceptance window (see 7.6). The logical inclusion means that the channel may progress to conversion when pulse shaping is complete. Within the master trigger logic unit, the production of a fast trigger inhibits the production of any further fast triggers until either the event rejection pulse or the end of readout.

The timing limits are defined by the Ge-Ge resolving time at the earliest, and the end of pulse shaping (5μs) at the latest. In practice the coincidence of Ge's will be the main trigger criterion so the fast trigger will normally be generated within a few hundred ns of the γ-ray interaction. If it is delayed beyond 1μs the TACs in the Ge and BGO cards will go overrange. Pulse width is programmable in conjunction with the Ge/BGO trigger acceptance window such that it covers the back edge of the window with defined setup and hold times (min 5ns).

The fast trigger is also available to non-VXI devices where its meaning is that an event of some type has occured and might be collected after some further checks.

7.3 Validation

The validation signal is generated by the master trigger logic unit to indicate that readout is to take place for the current event. It may be used to signal the results of a second level of trigger checks, typically the arrival of a recoil fragment in the recoil separator or a Compton suppressed Ge multiplicity. If the checks prove that the event is not interesting (e.g. no recoil fragment detected in expected time window) then no validation pulse is produced and the Ge/BGO channels included in the event will timeout at the end of their validation acceptance window (see 7.7). If no checks are performed or if the checks prove successful, the validation pulse is generated and indicates that readout may follow conversion in the Ge/BGO channels.

The timing constraints relate to the earliest start of the validation pulse. It may be internally generated any time in the master trigger logic unit, but because of its dual meaning and the self timing nature of the channels it must not be transmitted to the Ge cards before the start of their conversion phase. Normally it will be sent out during the Ge conversion phase, but it may, however, be delayed after the end of conversion at the user's discretion for unusually late event validation signals (e.g. very long flight time to additional detectors) although care must be taken that the late component belongs to this event rather than one which we have missed during the deadtime period. The pulse width must be such that it covers the back edge of the validation acceptance window with defined setup and hold times (min 10ns).

It is possible that different logic modules produce validate and reject pulses for the same event. In this case the earlier signal takes priority.

The signal is distributed via the Slot 0/RM module in each crate. It is not time critical and so could use one of the ECLTRIG lines. The setup and hold times for the back edge of the validation acceptance window can be reduced to the same value as the fast trigger by using the STARY lines, but this is not essential if they are needed for other purposes.

The validation signal is available to non-VXI equipment. In this case its meaning is that readout will take place as soon as data are available in VXI crates and so the non-VXI equipment should organise its own readout for the current event.

7.4 Event Reject

This is the alternative to validation, generated by a negative validation. It means that all Ge/BGO channels which accepted the fast trigger must stop at the earliest opportunity. We have already noted that the shaping and conversion stages proceed to completion once started, but it may well be possible to prevent the start of conversion by generating event reject within the first 5μs. The system will not derive any performance advantage from this signal without gated integrators for shaping.

The signal will be distributed to each Slot 0/RM unit which will in turn distribute it via a VXI ECLTRIG line.

The timing constraints are that it must be generated after the fast trigger pulse and may not be generated after the end of the Ge/BGO validation acceptance windows. Additionally it may not be generated at the same time as or after a validation pulse. If it is generated before a validation pulse, the validation pulse will be ignored (this resolves the potential conflict between multiple logic modules where one validates and the other rejects the event: the earlier signal takes precedence.) Pulse width is not particulary important and it is probably unnecessary to make it programmable. A fixed length pulse of 500ns is proposed.

7.5 Readout Complete

This is a high active open collector type signal from all readout controllers, and any non-VXI equipment involved in data collection, to the master trigger logic unit. It is driven low (false) in response to the Validate signal by each readout controller. The readout controllers must continue to drive it low until they have successfully completed readout when they may release it to its high state. When the last readout controller has finished readout the master trigger logic unit will see the readout complete signal go high and will begin to look for a new event, removing the inhibit condition imposed by the fast trigger. The Readout complete signal will be protected by a programmable timeout within the master trigger logic unit. It would be easier from a cabling perspective if the readout complete signals were passed over the VXI backplane (local bus line?) from the readout controller to the Slot 0/RM module so that all the crate-master trigger logic connections pass through a single front panel.

7.6 Fast trigger acceptance window

This is a time window defined in each Ge/BGO channel during which that channel is waiting for a fast trigger. At the end of the window the back edge is used to sample the state of the fast trigger pulse on the VXI STARX line and if it is present then the channel is included in the event and can convert the input it is shaping. If there is no fast trigger pulse when it is sampled the channel allows the amplifier to return to baseline with no further action. The start of the window is defined by a programmable delay (0 to 5μs by 5ns steps) from the CFD detecting an input, and the width must be programmed in conjunction with the fast trigger pulse in the master trigger logic unit so that the back edge can sample the fast trigger pulse correctly. Absolute maximum is the end of the shaping period (5μs) but typical value is a few hundred ns. (The Ge TACs go overrange at 1μs.) The Fast trigger acceptance window is local to the appropriate Ge/BGO channel, although pulse width could be programmed on a per card basis.

7.7 Validation acceptance window

This window is very similar to the fast trigger acceptance window and is also local to the appropriate Ge/BGO channel but again could be programmed for width on a per card basis. It is timed either from the start of conversion or by a delay from the CFD firing initially. In either case it must start during the ADC conversion phase of operation and can extend beyond the end of that phase although normally it is contained within it. The back edge of the window pulse samples the validation pulse, the presence or absence of validation indicating readout or abandonment of event respectively.

7.8 Clear

There is no clear signal. The reason is that the trigger system is distributed and self timing. In the case of VXI modules the question of clearing does not arise because all channels will fail (or be aborted) at the end of either the shaping or readout phase or else successfully complete to readout; in any case an explicit reset is not required since the amplifier/gated integrator is effectively free running, the ADC returns to a sensible state after conversion and the readout register is overwritten by successive words. TACs must be self clearing. *Are they?*

Do we need a Deadtime output?

8 Non-VXI devices supplying data

In order to accept data from non-VXI devices such as Camac FERA ADCs or the Daresbury High Efficiency Recoil Mass Separator with its NIM ADCs plus NIM-FERA converters, we must use the common readout complete signal between the master trigger logic unit and the non-VXI readout controller.

For non-VXI devices it may sometimes be necessary to generate a local 'clear' signal (e.g. for NIM ADCs), and this could be derived from the back edge of the wired 'or' readout complete signal. If readout doesn't take place then there will be an event reject pulse from which to generate a clear. The fast trigger and validate signals will be available to non-VXI devices, but the timing may not be very helpful in generating ADC gates etc.

All non-VXI timing is the responsibility of the user.

9 User triggers

The user may use the CFD and LE discriminators on each Ge/BGO channel to construct complex triggers using CFD timing and LE energy thresholds. These may be either validations or fast trigger inputs. The master trigger logic unit will accept 16 front panel inputs for fast trigger and 16 for validation. In both cases the logical function to be performed on these inputs and the analogue multiplicity comparator is programmable.

Compton suppression as described below is a special case of a user trigger.

10 Compton Suppression

Compton suppression reduces the data rate by a factor of about 3. There are several possible methods of performing suppression and that proposed for Euroball will be used in Eurogam. The method is to use front panel connections from each Ge and BGO card to a large correlation logic map. The signals from the Ge and BGO cards will be pulses generated by CFDs on a one per channel basis. The logic map will be held in electrically erasable gate arrays[5] and will correlate every Ge signal with its neighbouring BGO signals. The result could take several forms:

- Suppressed Ge hit pattern (series of 3 (45 Ge) or 5 (70 Ge) 16 bit words.)
- Suppressed Ge multiplicity (either as a binary number or a series of bits used to switch on current sources).

Typical processing time will be 100 to 200 ns depending on the exact logic functions implemented. The logic map requires 70 Ge and 350 BGO inputs and generates 16 data bits with associated control/status pins. Obviously this must be split across several programmable gate arrays, each having typically 84 user i/o pins (Plessey ERA 60100 in 120 pin PGA). If this is split so that there are 16 output pins, 4 control/status pins and 64 input pins then we can handle 10 Ge/shield sets per chip, requiring 5 chips for a 45 Ge system and 7 for a 70 Ge system.

The output would normally be used as part of the validation, but could possibly be used in the fast trigger with a wide coincidence window.

11 Data supplied by trigger system to readout

The master trigger unit will supply the following information during readout:

- Event Number (32 bits)
- Real Time timestamp (64 bits; programmable to 100ns or 1μS resolution)
- Fast Trigger and Validation type number from each logic module in the trigger card.

12 Diagnostics and monitoring

It is important that the users are able to check exactly what the trigger system is doing. The main monitoring facility will be by scalers measuring the following:

- Fast Triggers
- Validations (Slow Triggers)
- Fast Triggers rejected while busy (per logic module)
- Fast Triggers accepted (per logic module)

13 Possible additional features

During discussion of trigger requirements several new features have come to mind. This section will describe those features and if there is sufficient interest from physicists the features will be incorporated.

[5] Xilinx LCA, Plessey ERA or similar device.

The first two features arise from discussions of isomer experiments. One possibility is to measure energy from a short lived (under $1\mu s$) isomer by having effectively two fast triggers, the second being armed by the first. The second trigger would be programmed to look for the isomer by looking for, for example, one or two gamma rays (or anything in an inner ball detector) within the expected isomer lifetime. This will only work for short isomer lifetimes because of randoms problems (is it really an isomer or is it another beam interaction?). The additional detecting elements would respond to the second fast trigger (using the STARY lines) using a second trigger window in the Ge cards set slightly later than the first. Obviously this will complicate the Ge cards and the trigger system, but if it allows new or interesting physics then it might be worthwhile.

The second feature is the inclusion of TDCs in the master trigger logic unit. These would overcome the fixed TAC start/stop limitations in the Ge cards, having access to all the signals at the trigger logic unit (Ge front panel CFD/LE signals, beam timing, fast trigger(s), multiplicity etc.). They could perhaps be started and stopped by logic modules similar to those used for fast trigger generation. They would be simple counter style TDCs which would probably have a resolution of between 1 and 5ns per bin, and a range limited only by the counter width (32 bits at 1ns = 4 seconds; 16 bits = $65\mu s$). They could even time event separation if that were thought to be useful. They would be included in the readout only if selected.

The third feature is the recording of a raw Ge multiplicity in the event data: if the array is used in a Compton Suppressed mode then the number of Ge cards in the readout gives the suppressed multiplicity, but there is no record of the raw Ge multiplicity.

14 An example experiment

Consider an experiment where the user runs Eurogam with the Daresbury high Efficiency Recoil Mass Separator (RMS). A typical trigger condition might be γ-γ-recoil (unsuppressed) but additionally we might want to collect any γ-γ-γ-γ coincidences (after Compton suppression) regardless of recoil particle detection.

In this case the time of arrival of the 'recoil present' signal will be between $0.5\mu s$ and $2\mu s$ after the reaction depending on mass. The gamma rays will arrive at the Ge's within 1 ns of the reaction. The readout of the Ge will be ready in $10\mu s$ and the readout of the recoil separator TAC's will be ready about $6\mu s$ after the 'recoil present' signal (via TFA, CFD, TAC, NIM ADC and NIM-FERA converter).

The fast trigger decision must be made on Ge multiplicity alone since this is the only information available initially. We will define a minimum coincidence period in the master trigger logic unit's fast trigger logic module and will arrange the CFD analogue pulse widths from the Ge channels such that they overlap for at least that period. The multiplicity cut off must be set at 2 which selects potential events of both γ-γ-γ-γ and γ-γ-recoil types. Detection of at least a γ-γ coincidence means that we will generate a fast trigger to define the event's participating channels and to stop their TACs.

(If the γ-γ-γ-γ did not need to be Compton suppressed we could use a second logic module to look for the second fast trigger condition with no further validation.)

The validation condition will now be either a suppressed multiplicity of 4 or the presence of a recoil particle. If either condition (or both) is true we allow readout to take place. This decision can be made with the help of a timeout period, set to be slightly longer than the latest expected recoil particle. If no 'recoil present' signal arrives before the timeout and the suppressed multiplicity (from Compton suppression logic) is not at least 4 then we issue an event rejection pulse. Since this decision can be made during the pulse shaping phase, the event rejection should be fast enough to prevent conversion and reduce deadtime to just the shaping time plus amplifier recovery time (5μs for a gated integrator; over 13μs for semi-gaussian amplifier). The wait for the recoil particle must not be set any longer than necessary to avoid the problems caused by a second reaction occuring during deadtime and sending a reaction particle into the RMS which gets collected with the first interaction's γ-ray energies.

In the successful validation case, the validation logic module will delay the issue of the validation pulse until after the start of conversion. This validation pulse also means that readout will take place, so the readout controllers in the VXI crates and whatever controls the NIM ADCs/NIM-FERA converter know that they will take part in event readout. Each one negates the common 'readout complete' line and attempts to read its ADCs, releasing the 'readout complete' line when they have successfully read all available data.

When all readout controllers have released 'readout complete' to its logically true state the trigger system knows that the event is complete and it may look for a new event.

The RMS requires a clear signal for its NIM ADCs (the TACs are Ortec 566 and will self clear). The clear can be generated from the end of the common 'readout complete' signal and fed to the ADCs via the NIM-FERA converter. Alternatively if the event is rejected the event reject line can be used as a clear.

15 Electrical and Mechanical Connections

This whole section is taken from the Euroball specification with a few minor changes to remove pipelining. It is largely correct but is certainly not complete and exhaustive.

15.1 Electrical Connection

All digital signals will be differential 100K series ECL, using normal 100K series thresholds. The only possible exception is that the local bus lines on the VXI backplane might use Futurebus driver/receivers instead of ECL because of their slower transition times which will reduce noise and signal reflections.

The analog sumbus signals will be 1mA per channel for both BGO and Ge, up to the maximum defined in the VXI specification (520mA).

15.2 Mechanical Connection

All fast trigger, validation, event reject and event readout signals are distributed in a star topology with the master trigger module at the hub of the network and a path of equal delay from the hub to every backplane.

The fast trigger, validation, event reject and readout complete signals will all travel as single ended signals over coaxial cable using 1 pin locking LEMO sockets in the Slot 0/RM unit and the master trigger logic unit, and the corresponding locking 1 pin LEMO plugs on the cable. The Master trigger logic unit will have 8 outputs for each of the fast trigger, validation and event rejection signals, and 10 inputs for the readout complete signals (8 VXI crates plus 2 non-VXI crates). *Could we daisy chain all the readout complete signals and use just one input on master trigger logic unit?*

The analogue multiplicity inputs will be 2 pin locking LEMO sockets to accept 2 pin LEMO plugs mounted on the end of coaxial differential cable. There will be 8 inputs from which Ge multiplicity is calculated, and another 8 from which BGO multiplicity is calculated.

The trigger and validation logic inputs to the master trigger logic unit's front panel will use twist 'n' flat ribbon cable to carry the differential signals. The front panel connectors will be 34 way headers with a locking extractor mechanism. A coded keying mechanism must be used to ensure that each of the cables to the master trigger card can only be inserted in the correct header. (This is in addition to the normal 'bump' orientation polarisation.) Contacts on both headers and connectors must conform to the DIN 41651? level 3 specification for gold plating to ensure reliability and long life.

The specification for CFD+Leading edge discriminator signals from Ge and BGO cards is the same as for trigger and validation logic signals.

16 Interface with Ge card

16.1 Signals output from Trigger System to Ge

- Fast Trigger Pulse (Backplane, 1 signal)
- Validation Pulse (Backplane, 1 signal)
- Event Reject Pulse (Backplane, 1 signal)

16.2 Signals received from Ge by Trigger System

- Analog multiplicity level (From a buffered VXI Sumbus supplied from each crate) (Front Panel, 1 per crate)
- CFD Logic pulse (Front Panel, 1 per Ge channel)
- Leading edge discriminator pulse (Front Panel, 1 per Ge channel)

16.3 Programmable timers etc. required by trigger system inside Ge card

- Width of Front Panel CFD pulse
- Width of Fast Trigger acceptance window
- Width of VXI Sumbus current pulse
- Width of Front Panel Leading Edge discriminator pulse
- Width of Validation acceptance window
- Width of internal 'phase A' (shaping)
- Width of internal 'phase B' (conversion)
- Width of Pileup window
- DAC for CFD trigger level
- DAC for Leading edge discriminator level

All these timers and DACs are provided on a per detector basis, so typically 5 per card.

In addition to these timers there is also a requirement that the Ge card provides logic using the timers in the way described in this document.

17 Interface with BGO card

17.1 Signals output from Trigger System to BGO

(same as for Ge)

- Fast Trigger Pulse (Backplane, 1 signal)
- Validation Pulse (Backplane, 1 signal)
- Event Reject Pulse (Backplane, 1 signal)

17.2 Signals received from BGO by Trigger System

- Analog multiplicity level (From a buffered VXI Sumbus supplied from each crate) (Front Panel, 1 per crate)
- CFD Logic pulse (Front Panel, 1 per BGO channel)
- Leading edge discriminator pulse (Front Panel, 1 per BGO channel)

17.3 Programmable timers etc required by trigger system inside BGO card

- Width of Front Panel CFD pulse
- Width of Fast Trigger acceptance window
- Width of VXI Sumbus current pulse
- Width of Front Panel Leading Edge discriminator pulse
- Width of Validation acceptance window
- Width of internal 'phase A' (shaping)
- Width of internal 'phase B' (conversion)
- Width of Pileup window
- DAC for CFD trigger level
- DAC for Leading edge discriminator level

All these timers and DACs are provided on a per detector basis, so typically 15 per card.

In addition to these timers there is also a requirement that the BGO card provides logic using the timers in the way described in this document.

18 Interface with Readout card

18.1 Signals output from Trigger System to Readout Card

- Initiate Readout (Validate) (via backplane)

18.2 Signals received from Readout card by Trigger System

- Readout Complete (preferably via backplane and Slot 0/RM card)

18.3 Logic and timers required inside Readout card

The trigger system expects that the Readout card will use the Validate pulse to initiate readout and will acknowledge this by driving Readout Complete low until it has successfully completed readout whereupon it will release Readout Complete. The Readout card must accept this initiation of readout during the ADC conversion phase without losing data. This assumes FERA style REN/PASS operation and that the Ge/BGO cards block REN during conversion. If this operation is not implemented the readout controller must still look to the trigger system as if it is implemented!

Additionally, the readout controller must not contain more than a single level of data buffering, and must not readout the next event until the current one has been transferred to the event builder. Deeper buffers require a new method of event identification with a broacast, or a self generated, event counter in each crate (see 6.5).

19 Interface with Slot 0/RM card

19.1 Signals output from Trigger System to Slot 0/RM card

- Fast Trigger Pulse (for distribution on backplane, STARX)
- Validation Pulse (for distribution on backplane)
- Event Reject Pulse (for distribution on backplane, ECLTRIG)

19.2 Signals received from Slot 0/RM card by Trigger System

- Buffered analog sumbus
- Readout Complete (wired OR) (via backplane from Readout Controller)

19.3 Logic and timers required inside Slot 0/RM card

No logic or timing is required of the Slot 0/RM card, but it must be designed such that board to board variation in timing from the front panel Fast Trigger input to the VXI STARX lines is less than 2ns (this is in addition to the 2ns slot to slot skew allowed in the VXI specification for STARX distribution over the backplane).

All trigger signals in and out of the VXI crate will be routed via the Slot 0/RM card (except Ge/BGO front panel CFD and LE signals for user triggers).

20 Interface with non-VXI equipment

20.1 Signals output from Trigger System to non-VXI equipment

- Fast Trigger
- Validation (start readout when ready)
- Event Rejection Pulse (abort and clear everything)

20.2 Signals received from non-VXI equipment by Trigger System

- Readout complete (Wired OR)
- Input(s) to Fast Trigger logic decision
- Input(s) to Validation logic decision

20.3 Logic and timers required inside non-VXI equipment by Trigger System

There is no specific requirement for logic or timers but some more general points must be observed. The first is that the non-VXI equipment must timeout and clear itself in the absence of an expected Fast Trigger: there is no centrally generated clear in the proposed distributed trigger system other than the event rejection signal. Secondly the non-VXI equipment must negate ‘readout complete’ in response to Validation if it has data to be included as part of the current event, and it must release ‘readout complete’ when the data are successfully read.