CH/Tech/98/03

Guide to the MEGHA DA System

A simple guide for first time users

Author: K L Jones

Date: May 26, 1998

A User's Guide to the MEGHA Data Acquisition System

1 Introduction and General Overview

This document gives an introduction to the DA system associated with MEGHA, including the amplifiers, logic units, digital converters and computer interfacing.

The data acquisition system for MEGHA has been designed such that all the digital conversion takes place within Time to Digital Converters (TDCs) instead of Analogue to Digital Converters (ADCs). The conversion from amplitude to time signals happens within the amplifiers, reducing the complexity of the associated electronics and cabling. The DA system includes an initial fast trigger, described here with the option to veto the fast clear using a second level master trigger, which is described here only briefly in the last section.

A pre-amplifier signal entering a MEGHA amplifier will result in two pulses being produced. A discriminator pulse is sent to a series of logic circuits and triggers which select whether or not the pulse is associated with a "useful" event. The second pulse, which is proportional to the amplitude of the amplified pulse, is converted within the amplifier into a logic signal. This logic pulse under-goes a further convertion such that its length is proportional to the amplitude of the initial energy signal. The pulses are then digitized and "packaged" into events which are stored in a memory buffer before being written to tape.

The processes involved with acquiring data can be divided into three stages, which will be described in more detail later.

1.1 Stage 1 - Encoding

An amplifier signal from a detector triggers the CAMAC logic opening a gate, so that other signals associated with that event may be accepted. All relevant signals are converted into logic time signals and passed to the TDCs. These logic signals contain both energy and timing information. This stage is controlled by the TAIL units.

1.2 Stage 2 - Readout

This is controlled by the FIACREs. Data from the TDCs are labeled and sent to the data stacks in the master CAMAC crate.

1.3 Stage 3 - Storing

Header words are added to the data which are then sent to the F2VB (fast memory) where they are broadcast onto the ethernet and also written onto tape. Once the cycle is finished, “re-set” signals are sent to all the amplifiers, ready for the next event.

2 Overview of Hardware

A total of 10 amplifier crates each containing 16 dual-amplifiers (32 channels) are incorporated into the DA system. These are controlled via three “slave” CAMAC crates, which are in turn controlled by a “master” CAMAC crate. A fifth CAMAC crate contains the multiplicity units (MALUs) which are used as an initial fast trigger.

Most of the logic and data transfer units controlling individual events are located within the CAMAC crates. The VME crate, located at the bottom of the left hand rack adjacent to MEGHA, controls the flow of data from the DA system, into buffers, onto tape and the broadcast onto the ethernet.

The layout of the amplifier and CAMAC crates in the electronics racks adjacent to MEGHA is shown in Figure 1

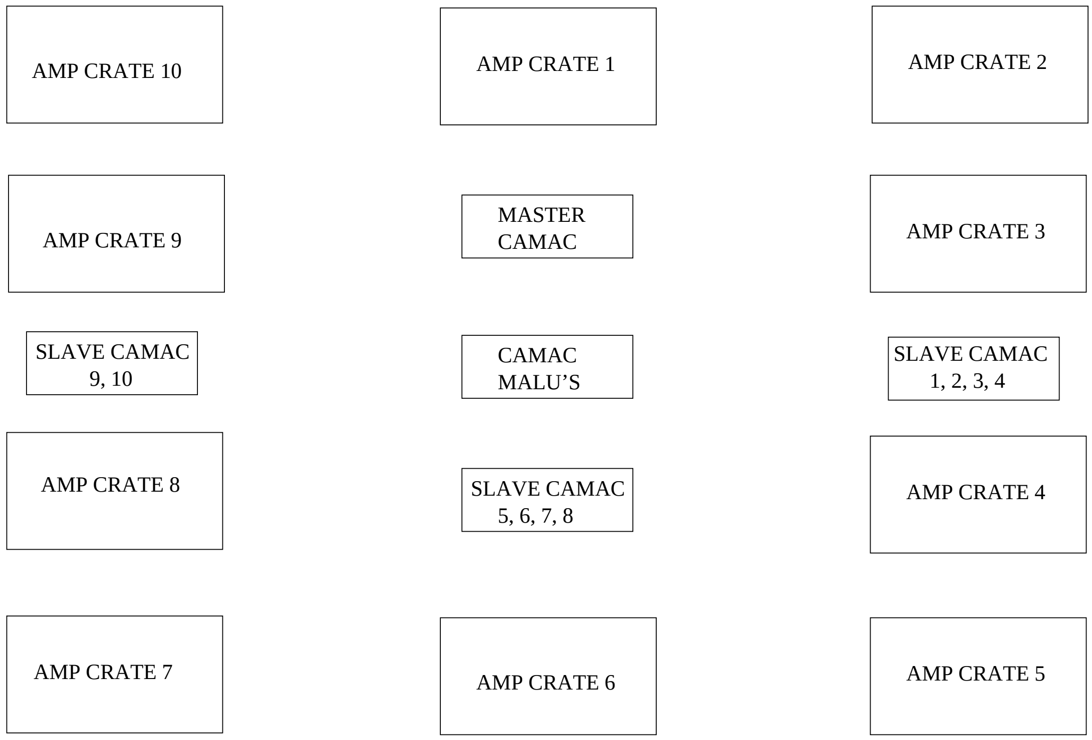

Figure 1: Layout of Data Acquisition System

The contents of the CAMAC crates are as follows:

MASTER CAMAC CRATE	SLAVE CAMAC CRATE
3 DATA STACKs 2 FEEDs (each handles 2 DATA STACKS) CATCH STARBURST SCALER	4 TDCs (2 only in third crate) TAIL FIACRE MALUs (number dependent on expt set-up)

Table 1: Crate Configurations

3 Signal Propagation

3.1 Amplifiers

The amplifier discriminator is triggered by the leading edge of the (differentiated) pre-amplifier pulse. This discriminator pulse is sent to the logic circuits (to be described later). In the usual set-up, the discriminator pulse is also fed directly back via a short lemo cable into the trigger input, on the front panel of the amplifier, and a 2.2μs

AMPLIFIER CRATE
32 Amplifiers (16 modules) 2 16 Channel WAGs 2 16 Channel CATs

Table 2: Amplifier Crate Configuration

trigger pulse results. (Alternatively, a more customized design is sometimes used. For example, the discriminator pulse from the PSD energy signal can be buffered and fed into the trigger input of not only the PSD energy amplifiers, but also the four associated corner amplifiers).

If the discriminator pulse is "accepted", as described in the next subsection then a MultiPlicity Pulse (MPP) is returned to the amplifier. A trigger signal in coincidence with an MPP pulse will produce a gate, the width of which is controlled by the amplifier setup and monitor software, which in turn enables the peak detect circuits. The internal gate signal can be viewed at an output on the front panel. The output voltage of the amplifier is then sampled and held at the peak value until a "clear" signal is given (see Figure 2).

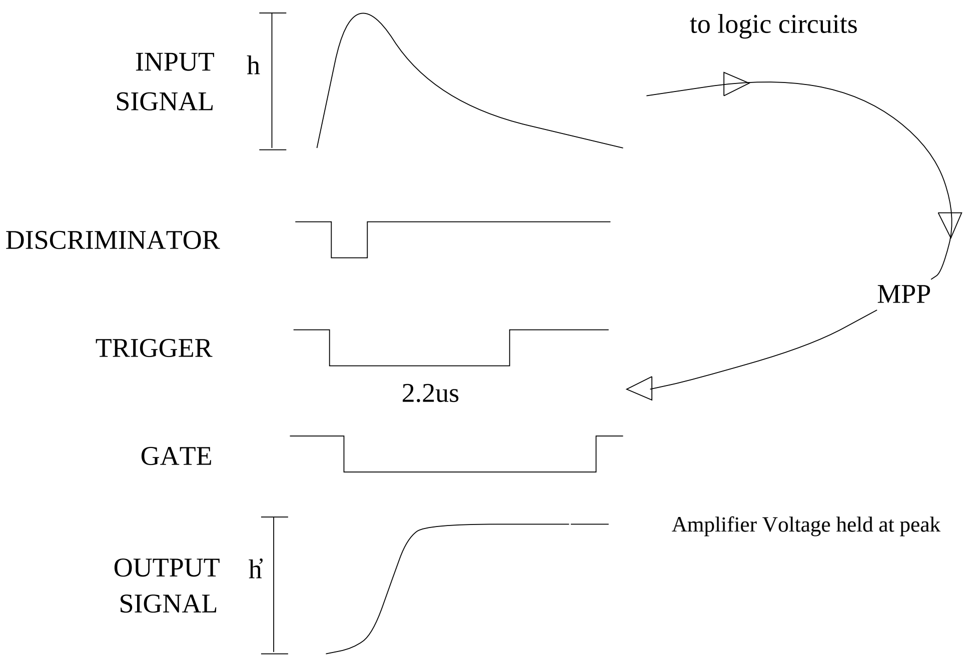

Figure 2: Signal Production within Amplifiers

3.2 MPP Production

The discriminator pulse from the amplifier is sent to a Walk and Accept Generator (WAG) unit. The WAG stretches discriminator pulse to form an 800ns WALK pulse. The WALKs from all the signals for the event occurring in the same amplifier crate are sent to the Multiplicity Unit (MALU) associated with that crate.

The MALU produces an output pulse which is proportional to the number of over-lapping WALK pulses; this defines the multiplicity for the amplifier crate. The MALU thresholds can be set to the required multiplicity e.g. for strip detector signals, one signal from each end should arrive at once, so the multiplicity is set to greater than 1, by setting the threshold between -100mV and -150mV. Only a minimum level of multiplicity can be set on the MALUs.

The signals from the MALUs are passed via the MIXER units (OR gates) into the three Time and Amplitude Interface Logic units (TAIL) located within the "slave" CAMAC crates. It is the TAIL units which, in response to the MIXERs, send the 4.5μs MPP pulse to all the amplifier crates. Any WALK signals entering the WAGs within the next 4.5μs will be accepted as part of the event.

(NB The MPP pulse was lengthened from 1μs to 4.5μs, for the April 1998 runs, so that all the PSD position signals would be coincident within this time interval.)

3.3 Stage 1

The MPP pulse, as well as being sent to all the amplifiers, is also sent to the TDCs (which are set to "ready" and start counting) and the WAGs.

Once the WAGs receive the MPP, they produce ACCEPT signals for every channel with an MPP and WALK overlap. These are subsequently used to enable the peak detect in the CATs.

The TAIL unit sends a pulse to the CAT (Convert Amplitude to Time, c.f. TAC) 8μs after the MPP (it is the TAIL unit which controls the timing within Stage 1). The leading edge of this pulse signals the CAT to ramp down from 0V at a rate proportional to the peak voltage from the amplifier output. The trailing edge of this TAIL signal (i.e.16μs after the MPP) causes the CATs to ramp up at a fixed rate. The time between the end of the TAIL pulse and the zero intercept is converted by the CATs into a logic pulse, the length of which is proportional to the energy signal from the amplifier. The WALK (which gives timing information) is multiplexed with this energy dependent time logic pulse. In this way, both timing and energy information are contained within successive pulses on one time-logic output (see Figure 3).

The multiplexed time-logic pulse is sent to the multi-hit TDCs which record the time of each rising edge. The first and second rising edges give information about the

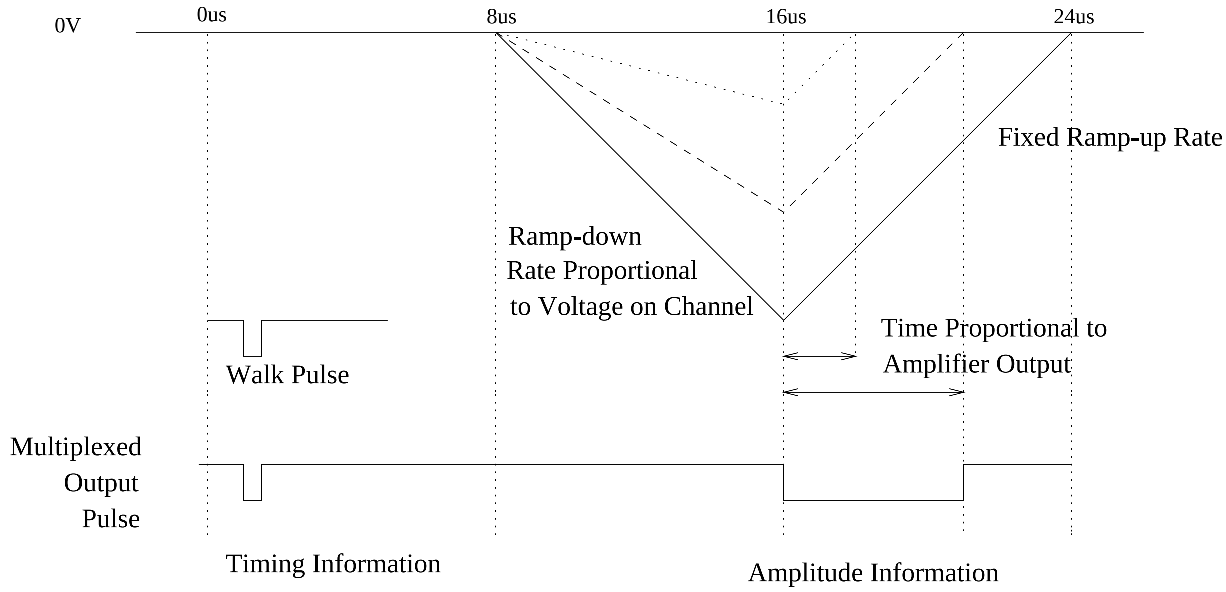

Figure 3: Time-Logic Pulse Production within CATs

timing and the amplitude of the pulse, respectively. Another 8μs later, the TAILs send a signal to the TDCs switching them out of "acquire" mode and into "read-out" mode. The TAILs also send a pulse to the FIACREs to bring them into "ready" mode.

3.4 Stage 2

Once the FIACREs are set to ready, they read the data from the TDCs via the CAMAC backplanes. The FIACREs perform a number of tests on the data before passing it on to the DATA STACKs. Firstly, they test that there are only two hits in the TDC data per channel (i.e. one timing and one amplitude). They also check that the time signal comes within the first 8μs and that the energy lies between 16 and 24μs. The FIACREs then remove 16μs from the amplitude signal and changes the TDC address from a local CAMAC bin address into a Global DA address, or parameter number.

For each channel, the FIACRE sends four data words to the DATA STACKs; absolute channel number, time, absolute channel number + 1, amplitude. Finally, the FIACRE sends a signal to the CATCH to tell it that there is data in the DATA STACKs.

3.5 Stage 3

The CATCH, which is located in the "master" CAMAC crate, sends data from the DATA STACKS to the F2VB (fast memory). The STARBURST unit aids in this process.

The STARBURST counts the number of words to be sent to the F2VB and adds this number to its running total. It then produces a “header word” which looks like FFFF followed by 16 bits which indicates the number of data words are in the event. The DATA STACKs then “dump” the data to the F2VB.

Once the running total gets close to 8000, the STARBURST adds “FFFF0000” to the data to show “end-of-block”. The STARBURST also sends a signal to the CATCH which in turn sends a signal to the F2VB to inform it of the end-of-block.

At this point, control of the DATA STACKs is returned to the CATCH, and the transfer of data resumes.

Once all the data has been passed to the memory, the CATCH sends a signal to the 3 TAILs, which subsequently send out signals to the amplifier crates to re-set all the amplifiers.

4 Additional Information

There are a number of CAMAC units, the details of which have been excluded from the description above for reasons of clarity. These units are mainly concerned with the control of crates or of other CAMAC units. This section will describe these units and the part that they play in the data flow.

4.1 Amplifier Crate Terminal Unit

The mail purpose of the terminal units is as crate controllers for the amplifier crates. They control the transfer of data across the backplane and provide an interface to the “strobe”, “busy” and “clear” signals into and out of the amplifier crate (via lemo connectors). The MPP signal is sent by the TAILs to the terminal unit which then passes it along the backplane to the amplifiers.

4.2 MIXER

The MIXER units can be used to “customise” the initial fast trigger at the input stage to the TAILs. There are three MIXER units, which can be linked together or used independently. The MALUs are read by the MIXER which sends the data to external logic circuits which can impose additional criteria other than the minimum multiplicity which is required by the MALUs. In this way, it is possible to reduce the dead-time by only accepting events which are more likely to be of interest at this early stage, rather than later by the main trigger.

4.3 FEED

The FEED controls the flow of data between the FIACREs and the DATA STACKs. The FEED is in turn controlled by the CATCH. Each FEED has two entirely separate halves and can therefore be used to interface two DATA STACKs.

4.4 Crate Controller

As the TDCs and the FIACRE units use the CAMAC crate backplane to communicate, it is important that the flow of data across the backplane is monitored. The crate controller has a dual purpose, to control the flow of data across the backplane and as an interface between the CAMAC crate and MIDAS.

5 Second-Level Trigger

The "accept" pulse from the WAG as well as being sent to the CAT, is also sent to the trigger link panel. This is where the data acquisition system is interfaced with the second-level trigger system. In simple terms, this second-level trigger system identifies coincidences between different detectors within the array, and within individual telescopes. This information is sent to fast NIM logic electronics where different event types identified by the XILINX trigger can be selected. In the case that the event is not of the required type, a "clear" signal is sent to the Data Acquisition. The "clear" signal fed to the NIM electronics is generated automatically by the MPP pulse. If the event fulfills the trigger requirements, then the "clear" is inhibited and the Data Acquisition is allowed to finish processing the event.

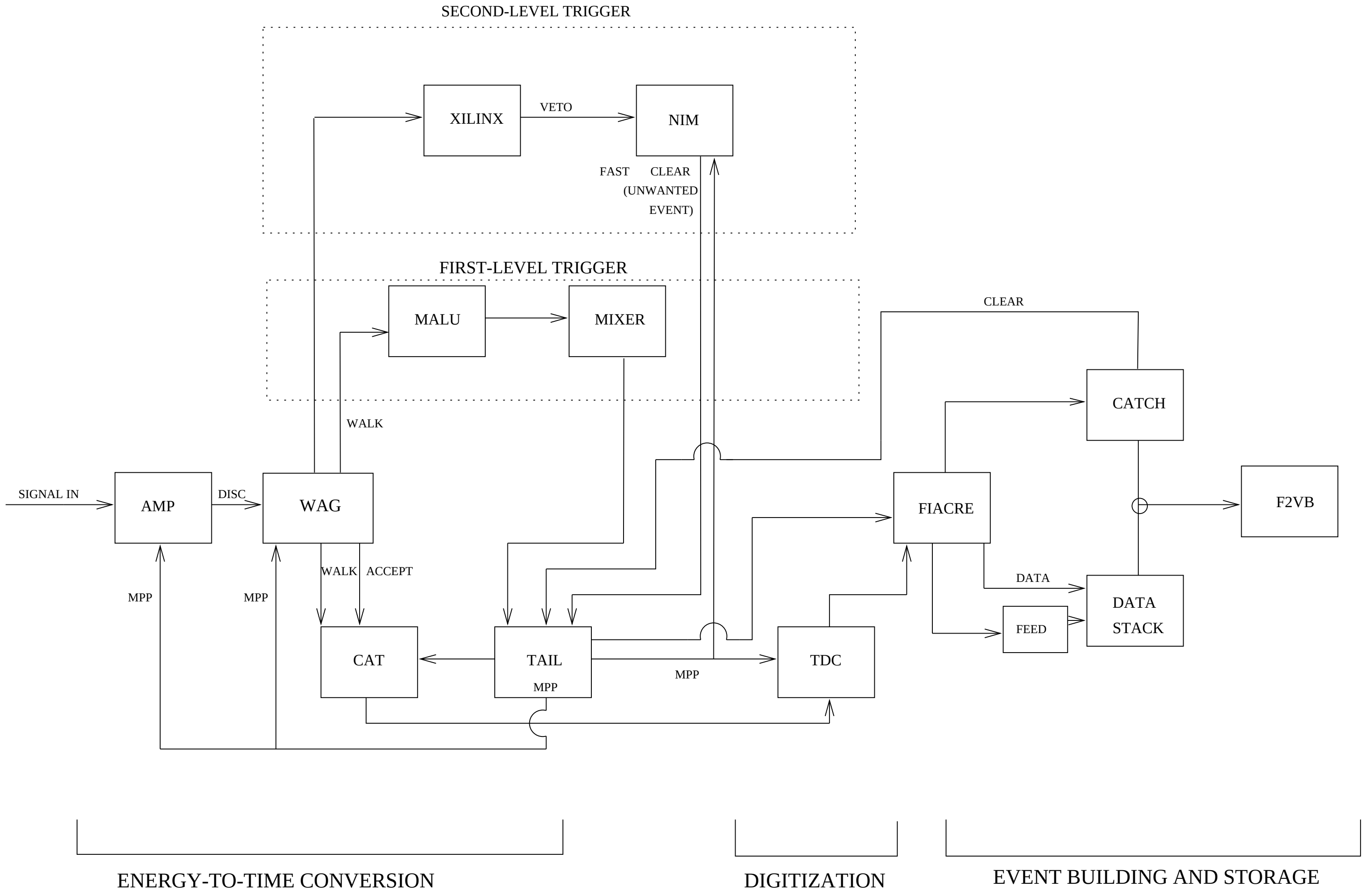

Figure 4: Simplified Block Diagram of Signal Propogation through Data Acquisition System