CH/Tech/93/11

Data Acquisition

Interim Improved Data Flow

Author: R.A. Hunt

Date: 15 December 1993

CHARISSA

Intermediate Scheme to improve Data flow

In the current scheme the GEC Emulator controls the output of data blocks from the Read and Store RS module using programmed instructions. This is an inefficient method compared with the original Direct Memory Access used at Daresbury and restricts the processing time available for on-line analysis.

The scheme outlined here is an intermediate proposal which involves a minimum change to both existing hardware and software.

It simply shunts the present Camac serial link by a fast autonomous ECL link and places each block of data directly within the VME crate adjacent to the Emulator.

A single width module FETCH has been designed which detects when the RS is waiting to output a block of data and then automatically issues a stream of read instructions through Camac to read the block. Each word is buffered and then sent via a fast ECL data-way FERA to a data stack HSM 8170 within the VME crate.

In normal operation a FERA transfer will take a fraction of the Camac cycle time so that burst transfer rates of 1.0 MHz could be obtained without the need for additional buffering within the FETCH module.

The FETCH module requests a Camac Read operation for each Synch Request issued by the RS. General control of the RS remains with the Emulator and the LAM signal which is now used to signal both read and errors requests will be masked so that only error calls are indicated at program level.

Each transfer is handled by an autonomous request for access to the Camac data-way followed by a request for a write to the VME store. If the VME store is unable to accept data before the next Camac request appears then this is signalled as a Clogged Link condition. The existing Clogged RS will continue to indicate when the store overloads but now the second clogged indication will show where the clogging occurs.

The present D/A scheme may be extended beyond 128 channels by using the feature of the MORE bit which selects which of the two 64 word CNAF command lists are used in the RS module. With the MORE bit set to 'ONE' every command in the first list is fixed to be an identical read from the Data Stack. With the MORE bit set to 'ZERO' the second list is active and contains the address of all associated Camac reads eg TDCs and Pattern Registers

This means that the data stack defines the limit of 256 ADC channels while the second list of 64 CNAF commands defines the limit of associated devices. Thus a maximum transfer would use header blocks 25, 26, 27 and 28 with the MORE bit set to 'ONE' followed by block 29 with the MORE bit set to 'ZERO'

To extend the present array from 128 to 192 channels additional hardware would be required at the Trigger Interface. Also the control program within the Event Control module must be modified to make three calls to the RS module. In the first two calls headers 25 and 26 would carry the MORE bit equal to 'ONE' and the third call 27 would have the MORE bit set to 'ZERO'.

This development should only be regarded as a temporary fix which would improve the current situation and could be ready for use by Easter 1994. The readout of the large array requires a completely new method of working which takes advantage of the new TDCs. It is proposed that in this scheme the Read and Store function is distributed over several 128 channel groups and all data is shifted into a fast FERA format immediately it has been processed within its group.

This scheme will use Starburst processors to aid the recognition and packaging for each data block. It will also be a convenient point at which we might consider changing the format away from the current header hit-word into a content/address form similar to that used for Eurogam.

Schedule and Costs

The prototype FETCH module will be built in January in parallel with the production of the prototype amplifier array. It would then be evaluated using a mockup link ready for a demonstration early in March prior to shipping on the 12th March.

The extension of the current array will require an addition of 64 channels to the Trigger Interface along with some local work at Canberra installing cabling and testing. The EC unit will also require a new program to be burnt in and checked. Once this has been proved at Oxford it is simply a matter of replacing a single chip 15 by 30 millimetres on site at Canberra.

The cost of building a FETCH module is estimated at £1500. The Trigger Interface extension is normally priced at £3000 but using some existing components its final cost is estimated at £1000. Edinburgh have a spare Trigger Interface which was used to support their work at Daresbury and if this could be obtained it could be shipped immediately to Canberra.

R Hunt 15.12.93