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Data Acquisition

Plans to Test Prototype System

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Outline of Prototype and Test Program

General

It is proposed that a 32 channel prototype of the new large array is available for test in Canberra for Easter 94. This should enable the users to assess the features of this system before a final decision is taken about the features which should appear in the final design.

A prototype has been constructed to allow a variety of test modes which include a basic mode where the 32 amplifiers may be operated as an extension of the existing array.

Two dual height Euro crates accomodate the 32 channels. Each crate contains 16 amplifiers and interface pairs along with three common positions which terminate the pairs and provide a convenient connection point for associated modules eg Silena ADCs, LeCroy TDCs .

In the basic mode a user may connect bipolar analogue signals from each amplifier along with related discriminator signals and take these directly to the Silena ADC and standard NIM logic. This allows the 32 channels to be used as additional channels in the existing array.

In a full test mode the amplifier interface or AIM will produce a pattern of WALK signals derived from the discriminator triggers along with a series of analogue/time conversions. These signals are then used to drive both a Multiplicity and TDC unit.

Various combinations have been anticipated between these two arrangements so that users may operate the prototype in a mixed transfer mode and obtain a comparision between the existing system and its proposed replacement.

Amplifiers AMPs

Each amplifier is identical to a current amplifier but with additional control features which allow a user to set fine gain, discriminator level and pole zero level.

These controls use non volatile circuits which may set a potentiometer by up/down pulses within a dynamic range of 100 values. All control circuits operate in conjunction with the manual controls on the front panel and may be viewed as internal trimmer controls which allow the user to set parameters locally by screwdriver or plug in panel. A control interface module terminates all control selection and this will be used to connect remote control for the amplifiers. The key analogue signals within each amplifier may be selected for display and again this option is designed for both local and remote operation.

Bipolar and unipolar signals at each amplifier output are taken to an associated interface module AIM by rear coaxial cables along with a discriminator signal. The analogue bipolar signal and discriminator signal are also available at the front panel of each amplifier.

Amplifier Interface modules AIMS

The amplifier interface module AIM is mounted directly above each amplifier and receives two analogue signals bipolar and unipolar along with a discriminator signal. The analogue signals are either processed by a peak sense circuit with sample/hold features or an integrator again with sample/hold. These circuits are arranged on sub boards which plug into the main AIM board.

The peak sense circuit is a Silena sub circuit which accepts a positive peak input from the bipolar output of the amplifier and for a maximum 10 volt peak input will hold a 3 volt positive level at its output. A fixed trimmer is used to set the minimum input level.

The integrator circuit accepts a negative input from the unipolar output of the amplifier and applies this to a Miller integrator. The gain of this integrator which determines the time constant is adjustable and controlled by non volatile potentiometer which is reflected in the feedback resistor ratio. The Miller circuit output is sampled through the gate period and held constant until a common clear resets all channel pairs. The positive output level is designed to match the output of the peak sense circuit at 3 volts maximum

The discriminator signal is first converted to ECL levels and then passed to a front panel socket which may be wired to group signals so that any discriminator signal will trigger associated channels.

The returned discriminator signal is used to trigger a WALK signal which is used to obtain the multiplicity trigger MAP and also to set the ACCEPT condition whenever a MAP is coincident with a WALK.

Along with the WALK signal the discriminator also fires a dual time period which is used to define a gate period. The first portion of the gate 2 usec is arranged to begin integration as soon as posssible and if the ACCEPT signal is received then the gate extends over the second period which is adjustable from 2 to 20 usec by a remote controlled resistance similar to that already described for the amplifier. Where the ACCEPT signal is not set then the second period is used to ensure that the integrator is fully discharged before accepting a further pulse.

Every event generates a tail pulse which is used to mark the two states of pile-up. First where the pulse is accepted and then a second pulse occurs to distort the amplifier's response or secondly where an accepted pulse occurs inside the tail of an earlier single event.

Once the analogue input has been processed and held following the gate period then a dual slope convertor is used to change its amplitude into a time period TIME. The beginning of this conversion is closely controlled by a common RUNDOWN time period which defines the charge period of Miller circuit. The following RUNUP period is proportional to amplitude and the TIME out put is the sum of both RUNDOWN and RUNUP periods. By combining the TIME signal with the WALK signal it is possible to compress the time of arrival and amplitude of a channel event into one channel of a multi-hit TDC.

The WALK/TIME signal is used to both provide the multiplicity and also the TDC input. This signal appears as an ECL balanced pair drive on each AIM module output and is taken to a termination module which connects through stripline cables to the TDC and Multiplicity unit.

The ACCEPT and PILE-UP patterns are also available as balanced pair ECL signals from each AIM. The ACCEPT pattern is identical to the hit word pattern in the existing array and will be used to control the readout of data from the TDC and construction of an event block. The PILE-UP pattern is simply inserted into the event block as two sixteen bit words.

Production Schedule

All 32 AMPs have been built and tested with their associated control logic. The 32 AIMs and associated circuits are now in a production stage which should yield the printed circuits by the first week in January and the finished units ready for test by 12th February. Testing the prototype has been estimated to take four weeks and our target would be to ship the equipment to Canberra on the 12th March.

In addition to the basic 32 channels various other modules are required to be built in parallel to support the test program. Three types of termination module are required Silena Driver, Time/Multiplicity Driver and Control Interface. We also need a portable control panel for setting the various parameters. Priority will be given to producing a Silena Driver which will enable the integrator performance to be tested together with the two control modules. The production of these support modules will be fitted around the schedule to produce the basic 32 channel block and also to produce the FETCH module ,described in separate note, which is essential if we are to improve the performance of the GEC Emulator.

It is difficult to predict how much of the ancillary equipment will be ready for the shipping deadline since we shall give first priority to the production of the basic 32 channel unit and any slippage in manufacturing ,outside of our control, will cut into the four weeks which have been allowed for final test before despatch.

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