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Electronics

Charissa Amplifier Development

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CHARISSA AMPLIFIER DEVELOPMENT.

Present Scheme

In the current scheme each main amplifier produces an analogue pulse proportional to energy input along with a digital discriminator pulse which indicates when the input crosses a preset threshold level. The discriminator pulse is used to generate a walk period, usually set at 500ns, which when combined with other walk signals will produce a multiplicity pulse. It is this multiplicity pulse which marks the beginning of an event and generates a common gate period.

The common gate period is adjusted to include the range of analogue signals from the whole array and is usually set at about 5 microseconds. These analogue signals are then converted by a set of Silena 4418 ADCs which are opened by the common gate signal. The trailing edge of selected walk signals form inputs to LeCroy TDCs where they indicate the relative position of those channel signals within an event.

The common gate scheme is suitable for energy signal inputs with a defined peak whose amplitude is proportional to the energy but it does not give an ideal response where the energy is distributed unevenly within the event period. This situation can occur with strip line detectors which give a spread of energy over a gate period dependant on the position of the particle impact within the line.

There are also problems of space and cost in simply enlarging the present scheme to meet future requirements along with the problem of monitoring and controlling such large arrays.

Outline of Proposed Scheme.

In the new scheme each main amplifier will be supported by a channel control unit which is mounted adjacent to the amplifier and provides both the signal conditioning and control of amplifier parameters. The main amplifier will produce both a unipolar analogue pulse and a digital discriminator signal when the pulse is above a set threshold.

This digital signal will start the channel control which will generate a walk period and a local gate period. The experimenter then has the choice of either a Silena type sample/hold circuit or an Integrator circuit to process the analogue signal. Discriminator outputs from each amplifier may be combined at the channel control input so that a pair of channels may be triggered by either of their associated amplifiers.

Since each amplifier now generates a local gate, then it must also recognize when it is to be included within an event. This has been done by generating a walk period and using this to window a common multiplicity signal. A coincidence between the multiplicity and walk signals will set an accept condition so that the amplifier will continue to integrate for preset gate period. Where an amplifier fails to detect a multiplicity pulse then it will clear the integrator at the end of its walk period. Thus the amplifier will now provide both walk and gate period locally.

The common multiplicity signal is generated by combining all multiplicity signals in a LeCroy 4532 Majority Logic Unit.

Charge to Time Conversion

In this scheme each analogue pulse is converted to a period of time. The leading edge marks the relative position of the discriminator signal in relation to the common multiplicity signal while its duration is proportional to the amplitude of the analogue pulse.

Thus the instant of the leading edge gives the time of arrival for the pulse within an event while the relative position of the trailing edge indicates the amplitude of the pulse. By fitting both time and amplitude into a common time period we are able to use a very compact data acquisition system based on the LeCroy 2277 TDC. This unit will accept 32 channels where each channel may contain 16 separate time intervals resolved to 1ns. Thus the proposed array of 256 channels could be fitted into a single Camac crate of 16 single width modules. In practise these channels will be distributed in groups of 64 adjacent to each rack of amplifier and channel control units.

In an earlier proposal it was suggested that the LeCroy MQT200F chip might be used for the time conversion but it was found that gate period for this integrator could not be easily extended to several microseconds and further that the linearity was not comparable to the Silena ADCs in our current array.

In the present design the analogue signal from the amplifier is either processed by a Silena sample/hold circuit or a controlled integrator. Both circuits occupy a sub-board 60 x 35mm which plugs into the channel control unit. The gate period may be varied from 1 to 16 microseconds and also the integration constant may be varied through 16 different settings.

Immediately after the gate period the processed signal will drive a linear ramp down for a preset time period. The depth of the ramp is then proportional to the amplitude of the applied signal. This ramp is then allowed to recover in a linear sweep to its original threshold value at a fixed slope rate.

A dual slope conversion circuit improves both the stability and linearity of the conversion since the factors of RC time constant,drive amplifier gain and threshold setting are all common for both the falling and rising sweep. This circuit has been carefully checked using the Silena input circuit and it was found that its linearity was comparable to the Silena ADCs.

Channel Control Unit

Each channel control unit provides a walk period output which is combined with other channels to give a common multiplicity signal. When an active channel receives this multiplicity signal then it generates an internal accept signal and proceeds to convert the analogue input. Where the multiplicity signal does not overlap the walk period then the channel control automatically clears down ready for the next event.

If the channel has been accepted then it will output a time period immediately after the gate period has ended. This period will have a minimum duration of 4 microseconds equivalent to channel 0 and a maximum of 8 microseconds equivalent to channel 4000.

Each active channel also generates an internal pile-up period and outputs a pile-up signal whenever it goes active while the pile-up period is present.

Timing for the gate and dual-slope circuit is locked into a 100ns delay line clock which starts at the instant the channel control becomes active.

The walk period, gate period and integration rate are all controlled by non volatile memory which may be varied by computer control. This control is also applied to the associated amplifier where it may vary the fine gain, pole zero setting and discriminator level.

Computer Control

Computer control of the amplifier/integrator should both reduce the effort in setting up a large array at the beginning of an experiment and also ease the task of monitoring such an array during a data acquisition phase.

Each channel contains non volatile memory chips in which various key parameters such as gain and time settings are stored. These parameters are automatically loaded when the power is initially applied to the control and may then be varied under computer control.

The non volatile memory is arranged either as an eight bit switch or a digitally controlled potentiometer. In both cases they are controlled serially from an on board processor on each channel control board. This processor is simply an interface between a string of ASCI command words and the particular signals which are used to drive the non volatile memory.

In the case of the amplifier it was arranged for the digitally controlled potentiometers to be simply placed alongside the existing manual controls so that the experimenter could either switch out the computer controlled elements completely or use a combination of manual and remote control. A portable control block has been built to allow the experimenter to bypass the computer and get direct control over the various variables.

On the control channel the gate width, integrate constant and walk width are all controlled by eight bit switch units which are also set through the local computer interface. In addition there are two four channel multiplexers which allow the experimenter to monitor the various internal signals such as analogue signal input, integrate or sample/hold output, walk period, gate period, time period, pile-up and accept conditions. These signals are available at either the two lemo sockets on the channel control or a pair of common lines which may be relayed for remote viewing.

For the remote handling of channel control units all control commands are sent to the crate master position as ASCI word strings and then passed to a selected channel control unit within a crate.

Specification

Various factors have been examined in the design of this proposal and these are listed in an approximate order of their priority.

1. Option to measure charge rather than peak voltage in order to improve the conversion of strip line detector signals.

2. Generation of a local gate for each channel rather than common gate derived from multiplicity logic.

3. Recording of both energy and time relation for every channel.

4. The various parameters of gain, threshold, pole zero, walk and gate period to be either manually or computer controlled.

5. Remote monitoring to be provided for any pair of key signals via a linear multiplexor so that the user may access and adjust an amplifier local to the chamber. Signals would include walk period, gate period, amplifier input, integrator output, time period, accept condition, pile-up period.

There was also a general objective to reduce the space required for the electronics and reduce the cost per channel.

Construction

Although it was originally intended that the modified amplifier along with its associated channel control should be placed on a common board this has not been attempted in the present phase. There are certain advantages in keeping the two designs apart and chief among these is the uncertainty about how a large array might be configured. Also by keeping the amplifier board separate we can conserve the current investment in amplifiers by using a simple modification to add in the necessary control.

The control for the amplifier may be compressed onto a sub-board 35 x 35mm with five wire control from the rear socket. This sub-board is conveniently mounted directly onto the rear of the fine gain potentiometer on existing amplifiers and may be easily switched out of circuit for complete manual operation.

32 new amplifiers have been built with reduced width so that sixteen channels may now be placed across the crate. Again the control sub-board will be fitted in the first 32 channel group and later variations will include the control in a modified printed circuit board.

The amplifier and channel control would be interconnected at the rear and would also receive input signals from the rear. There would be two additional analogue connections which would be common to all integrator and also to the control position. These cables are used to monitor selected signals at the control station and would also be extended out to give remote access to the crate. There are also a number of unused connections in the standard connector at the rear of the two Eurocards and these are used to bring a control highway from the control position.

At the front of each integrator card there are three connectors and two Lemo sockets.

The upper connector is used for Multiplicity In, Clear In, Clear In, Test In, Time Out and Pile-Up Out. All signals are differential ECL and a special link board is used along the front of the crate to ensure that the Time Out connections from each amplifier/integrator are correctly identified at their connection to the TDC. A common Test Input is used to trigger all channels for for calibration checks.

The central connector is only used for individual access to a channel control from either a portable computer or other controller. This access enables an experimenter to make local adjustments to both control and amplifier. During a run this socket is covered by the link board.

The lower connector has a an output which echoes the digital discriminator signal from the amplifier along with a pair of input connections to trigger the channel control. Normally this connector is simply linked so that the digital output triggers the associated channel. As an alternative the second input may be used as a link to other channels. The ECL signals may be connected as an 'intrinsic OR' and this may be used to trigger a pair of strip line channels from either channel or enable a key channel within a telescope to trigger a group of associated channels.

In the prototype design the single front panel of the amplifier board will carry a monitor point for the amplifier input and output along with three key adjustments of coarse gain, fine gain, discriminator level, and pole-zero.

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