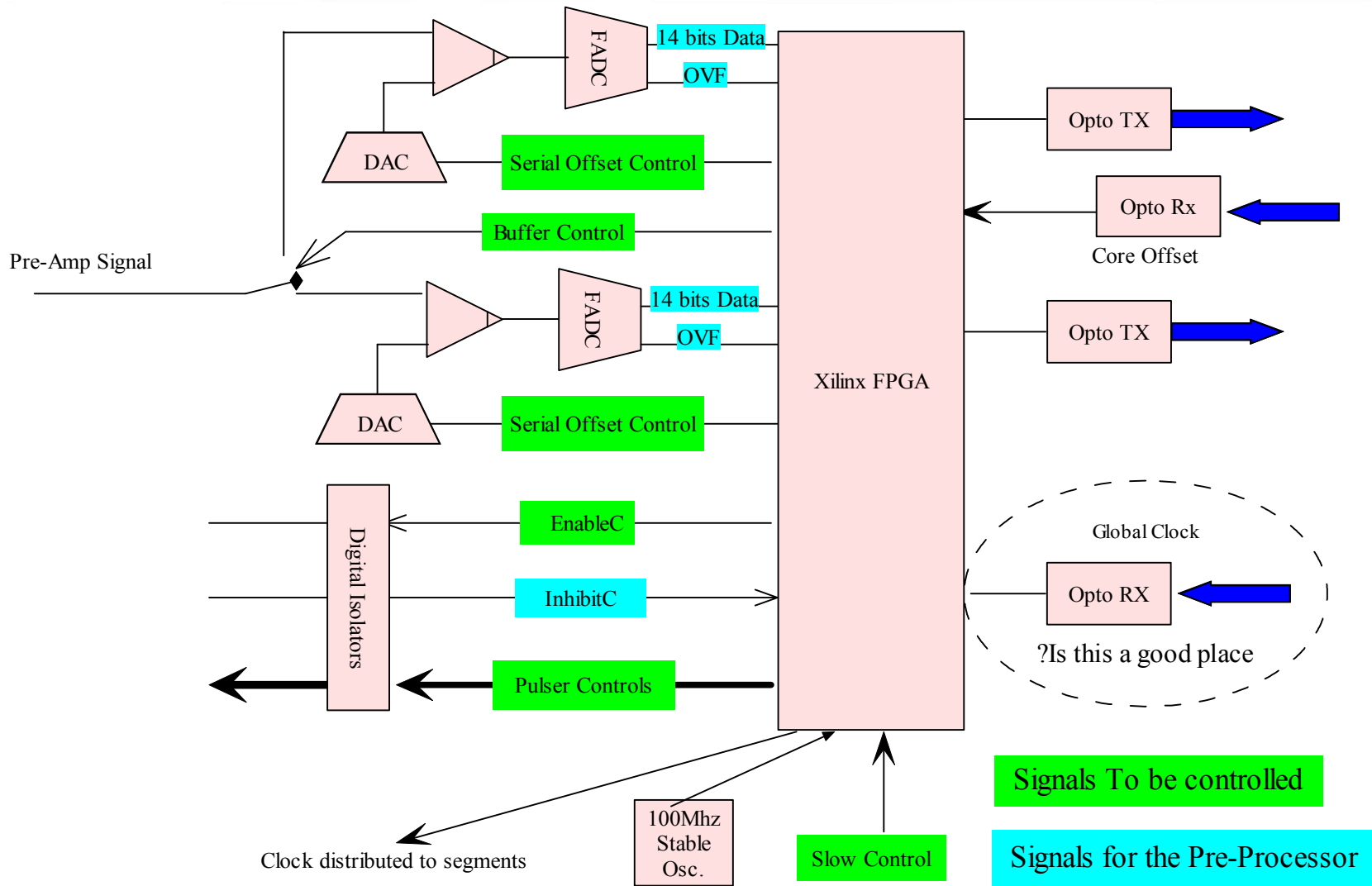
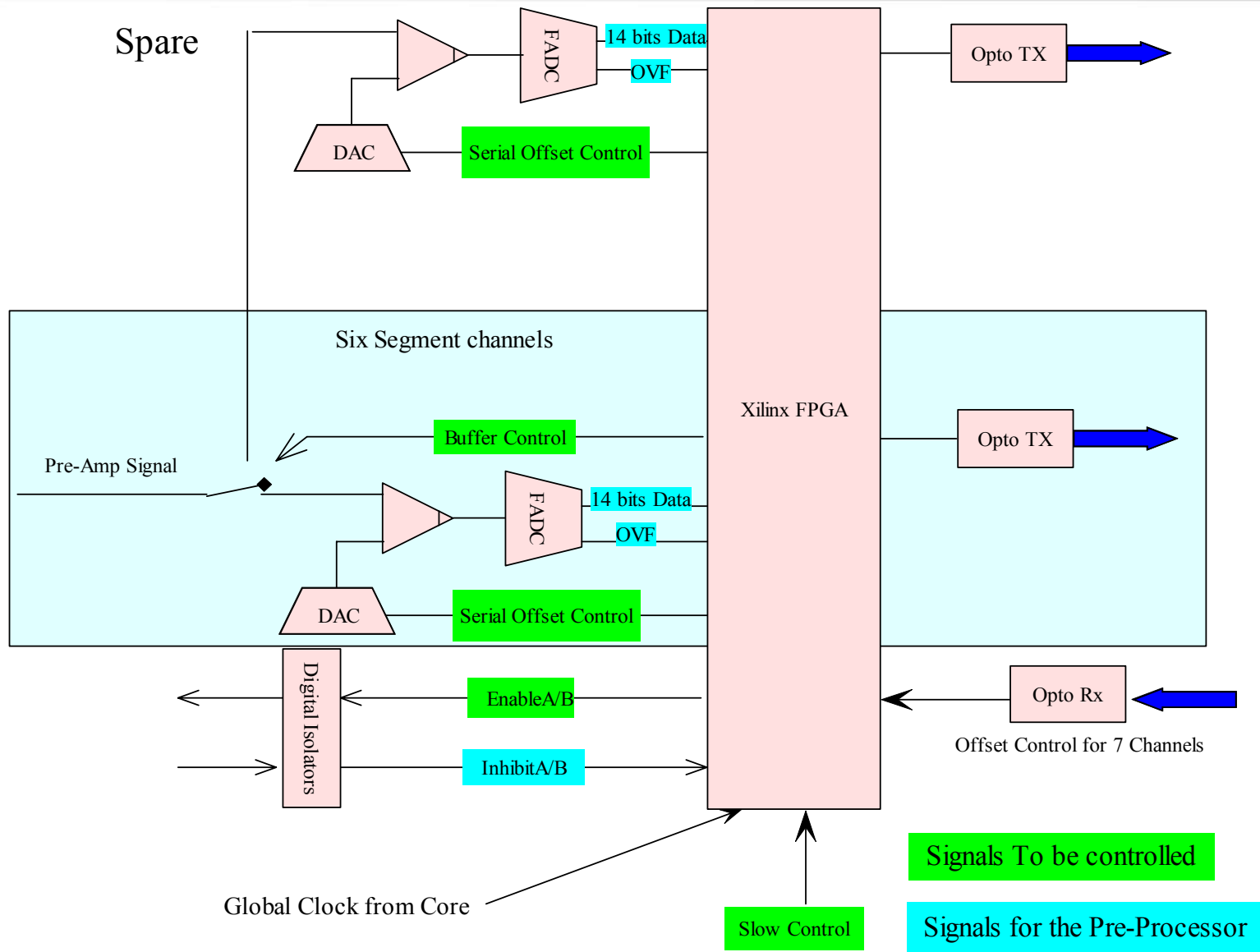


OverView of the Digitiser.

- 37 operational + 7 spare channels
 - Remotely controlled input Offset
 - Input routing to spare channel
 - 100Mhz FADC
 - Xilinx FPGA Serialise, and output as a 2Gb/s data stream.
 - VCSEL Laser transmitter for 6 segments and 1 spare.
 - Laser transmitter for core and 1 spare.
- Control interface to the Detector
- Offset control from Pre-Processor. 1 per 6 +1 spare





Digitiser Interfaces

1. Detector

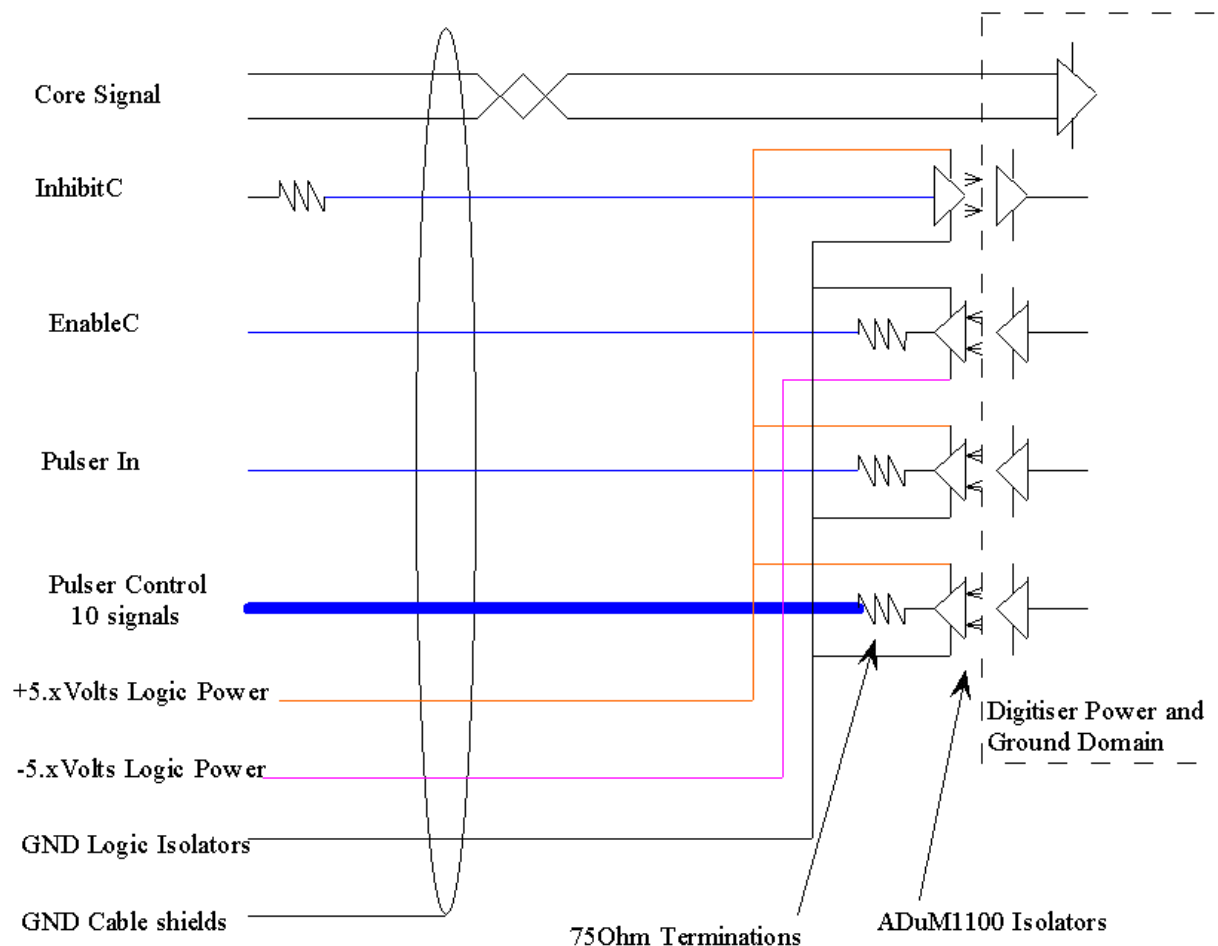
- 37 Differential Analog inputs.
- 36 isolated logic signals.

2. Pre-Processor

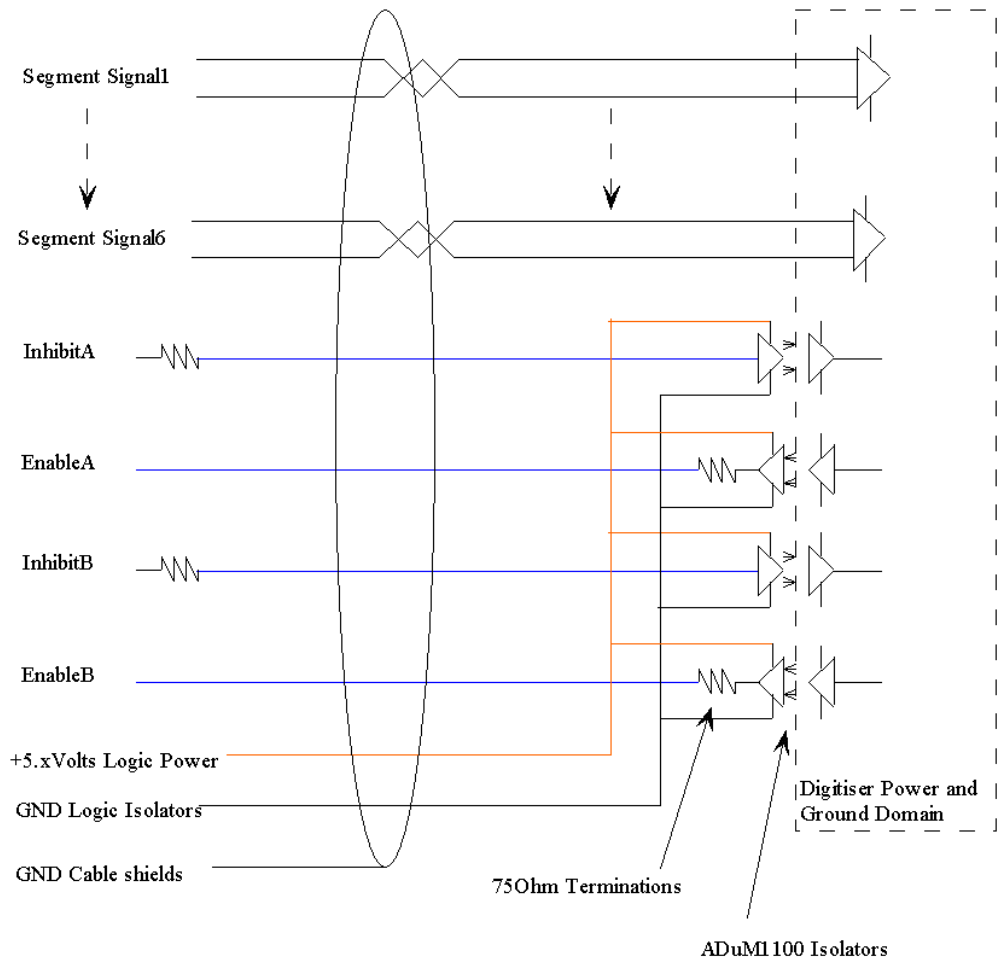
- 53 Fibre optic links

3. Local Monitoring

To Detector Pre-amplifiers. First the Core.

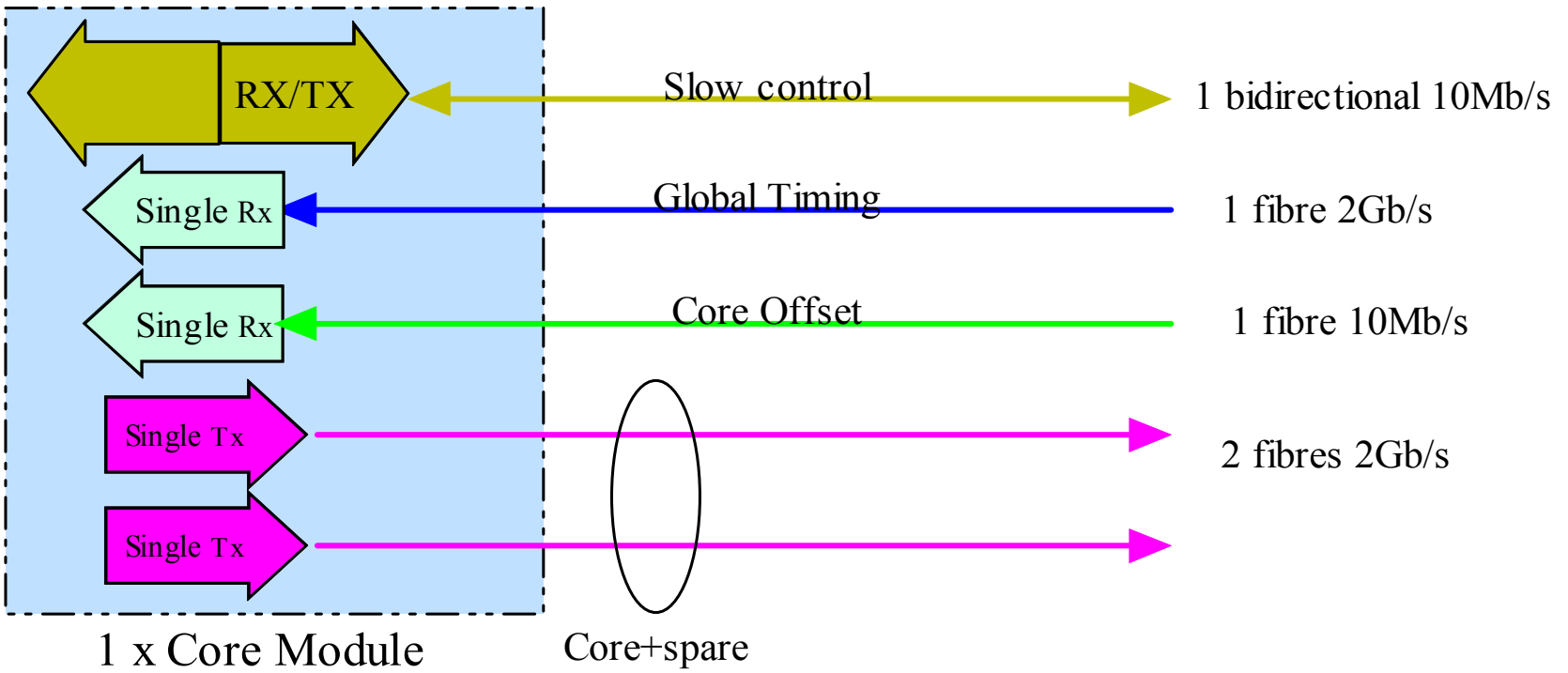


Second the Segments Six per cable



To Pre-Processor

Core + spare and Global connections



Core + spare and Global connections

Core & spare:

16 bits data at 100Mhz serialised, and 8B/10B encoded.

16bits => 20bits => 2Gb/s

Clock is based on Global Clock.

Global Timing:

Transfers the Global Clock.

Transfers timing related signals (synchronise??)

Core Offset control

Sends data to the offset DAC at the Core input.

Slow Control.

Transfers control and status between AGATA control and digitiser. (Via Pre-processor)



Core + spare and Global connections

Questions:

Core + spare : Do we need two optical links?

Global Timing: Is variable Latency a problem in this link.

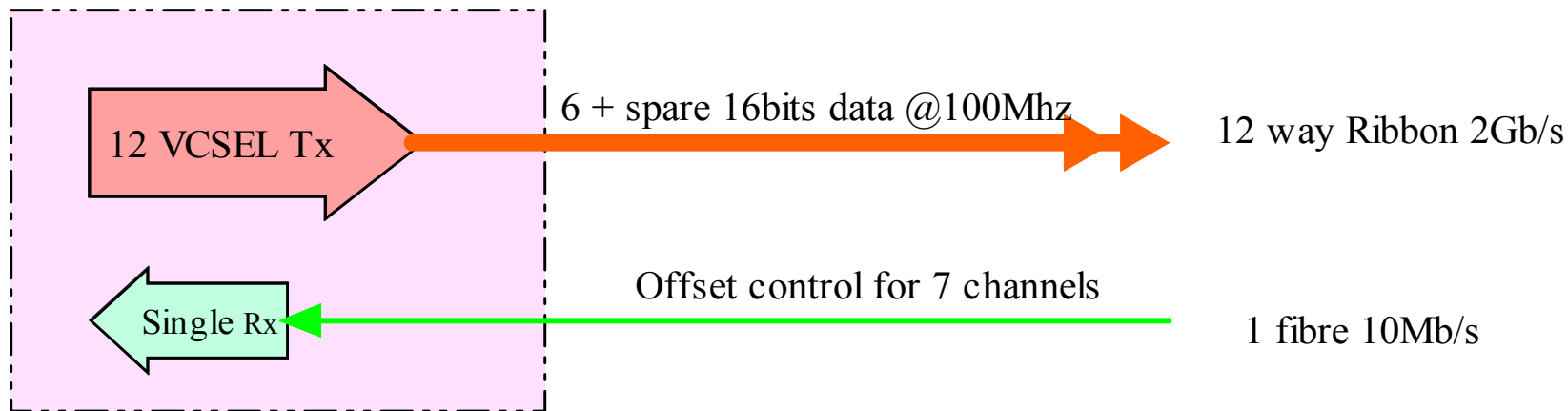
Offset Control : What speed is required. Taking account of latency through digitiser.

1/10/100uS.

Slow Control : Bidirectional, but what speed is needed ?

To Pre-Processor

Six x 6 Segment + spare connections



Segment + spare and Offset connections

Segments & spare:

Same as the Core.

16 bits data at 100Mhz serialised, and 8B/10B encoded. 16bits => 20bits => 2Gb/s

Clock is based on Global Clock.

Channel Offset control

Sends data to the offset DACs at the channel inputs.

Segment + spare and Offset connections

Questions:

Segment + spare : Do we agree on 7 fiber links?

Is variable Latency a problem in these links.

Offset Control : What speed is required. Taking account of latency through digitiser.

1/10/100uS?

Local use only : monitors

- USB : Controls module during test and diagnostics
- Inspection Lines
 - Analog
 - Input signal
 - FADC output via AD9765 DAC
 - Digital
 - Fast NIM

Optical Link trial module. What it contains

- Virtex II Pro XC2VP20 (8 Rocket I/O)
- 2 sockets for TX + 2 sockets for RX
- 2 Rocket I/O to SMA for copper link to demo board
- Clock from Metronome, or local Oscillator
- VME interface for power, control and statistics
- Static RAM for test pattern storage.
- Logic Monitor outputs.
- Analog inspection DAC

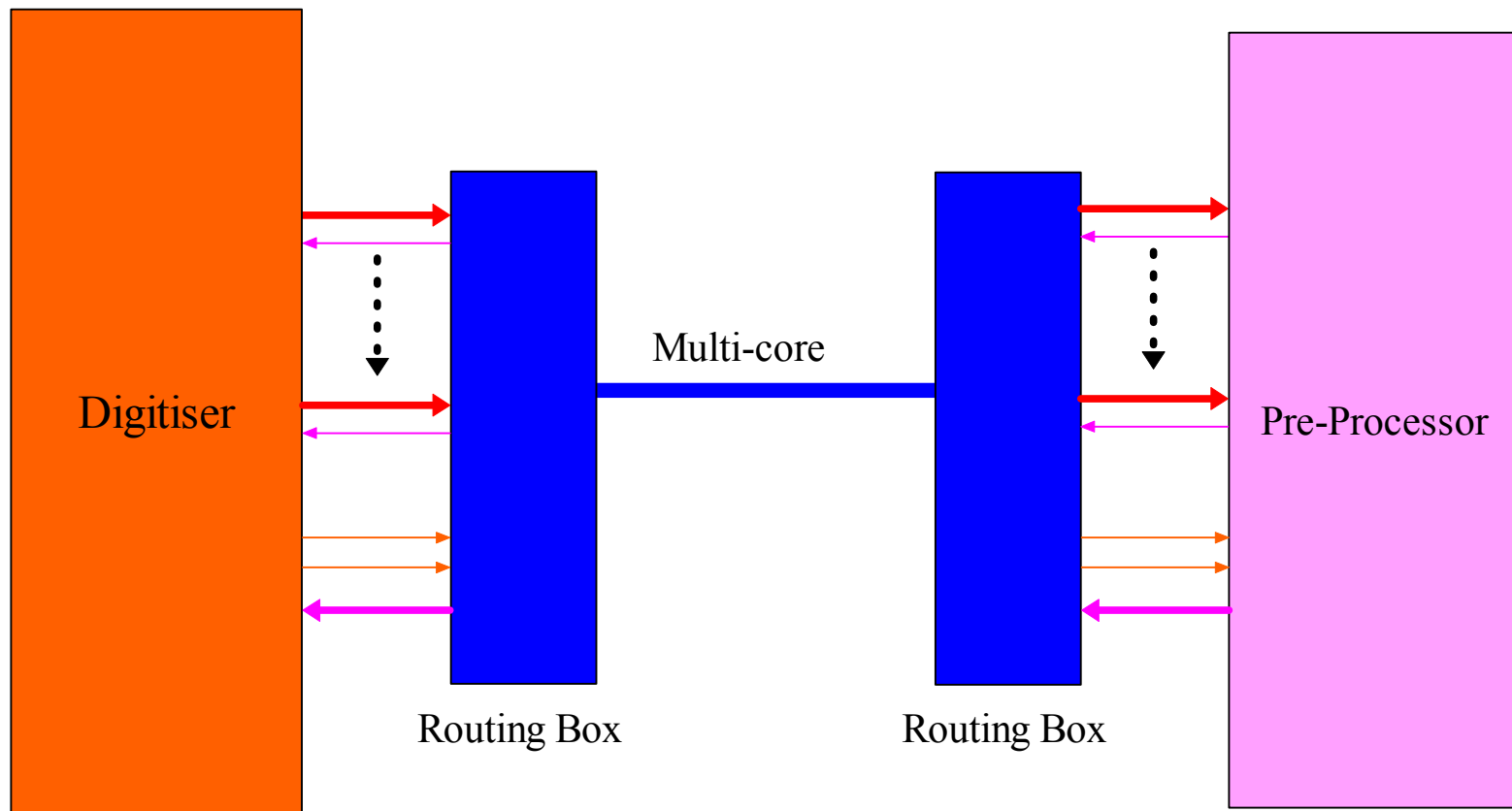
Optical Link trial module. What is tested.

- Link reliability, bit error rate (BER). Long term statistics
- Link Initialisation techniques.
- PCB layout with VCSEL TX on back of board
- Perhaps try link with faster bit rate , clock friendly bit patterns, CRC error check. Use metronome clock interface to check latency, and time drift.

PCB Daresbury, expected July 2004.

Xilinx VHDL IReS.

Using a single Multi-core for the 100 metre connection.



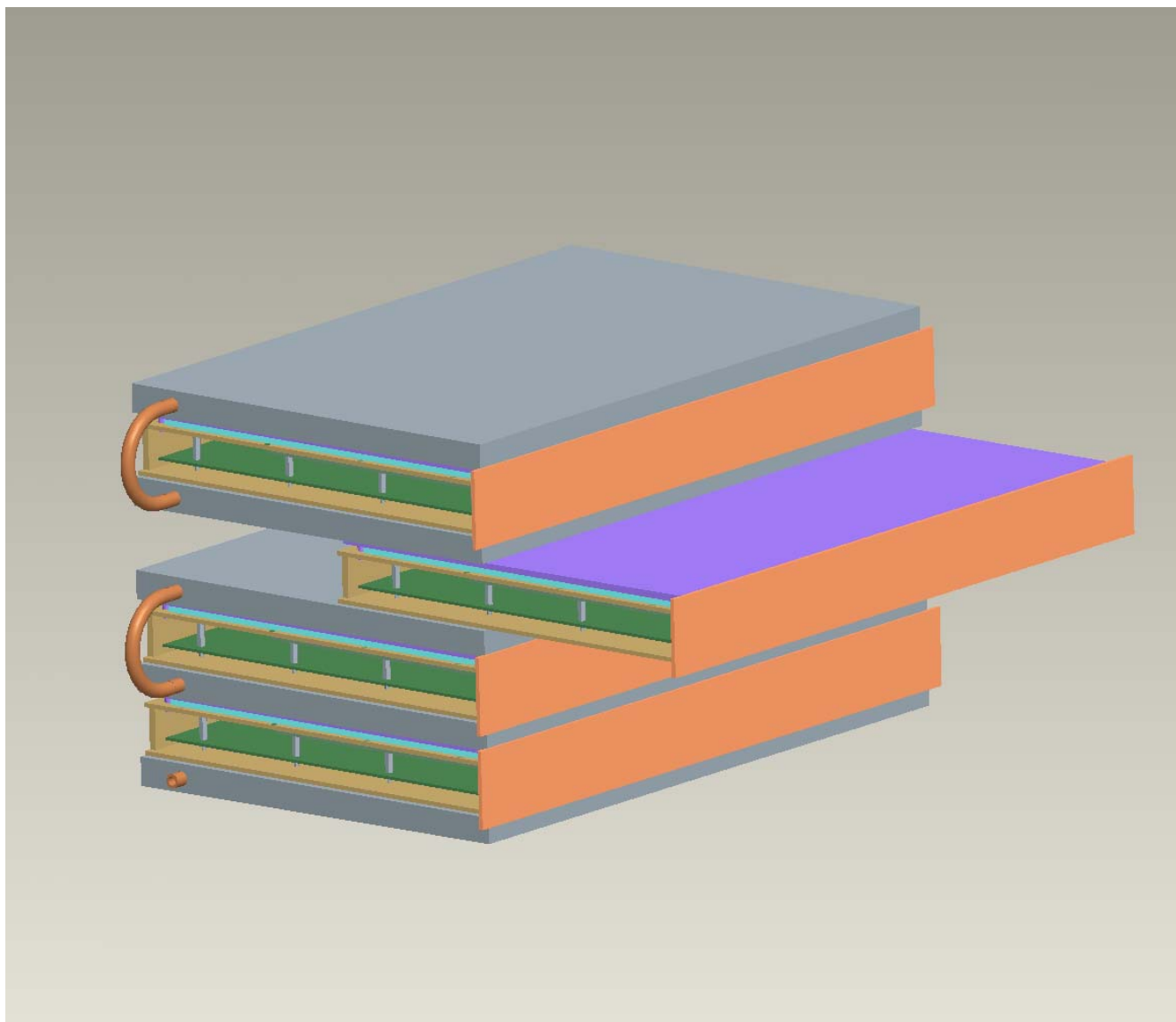
Some Questions:

Detector:

1. Definition of Pulser controls.

Pre-Processor:

1. How can we solve the latency problem ?
2. Do we need a core + spare optical link ?
3. Do we need a protocol to reduce the BER ?
4. What is the best cabling method.
5. What Protocol for the Offset, and Slow links



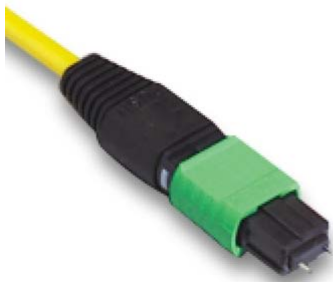
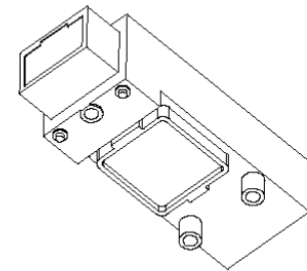
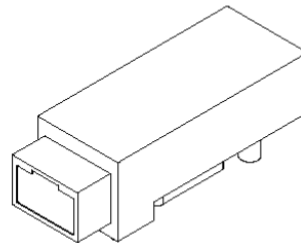


Figure 1 - Isometric Drawings



Xilinx Rocket I/O Embedded Core

