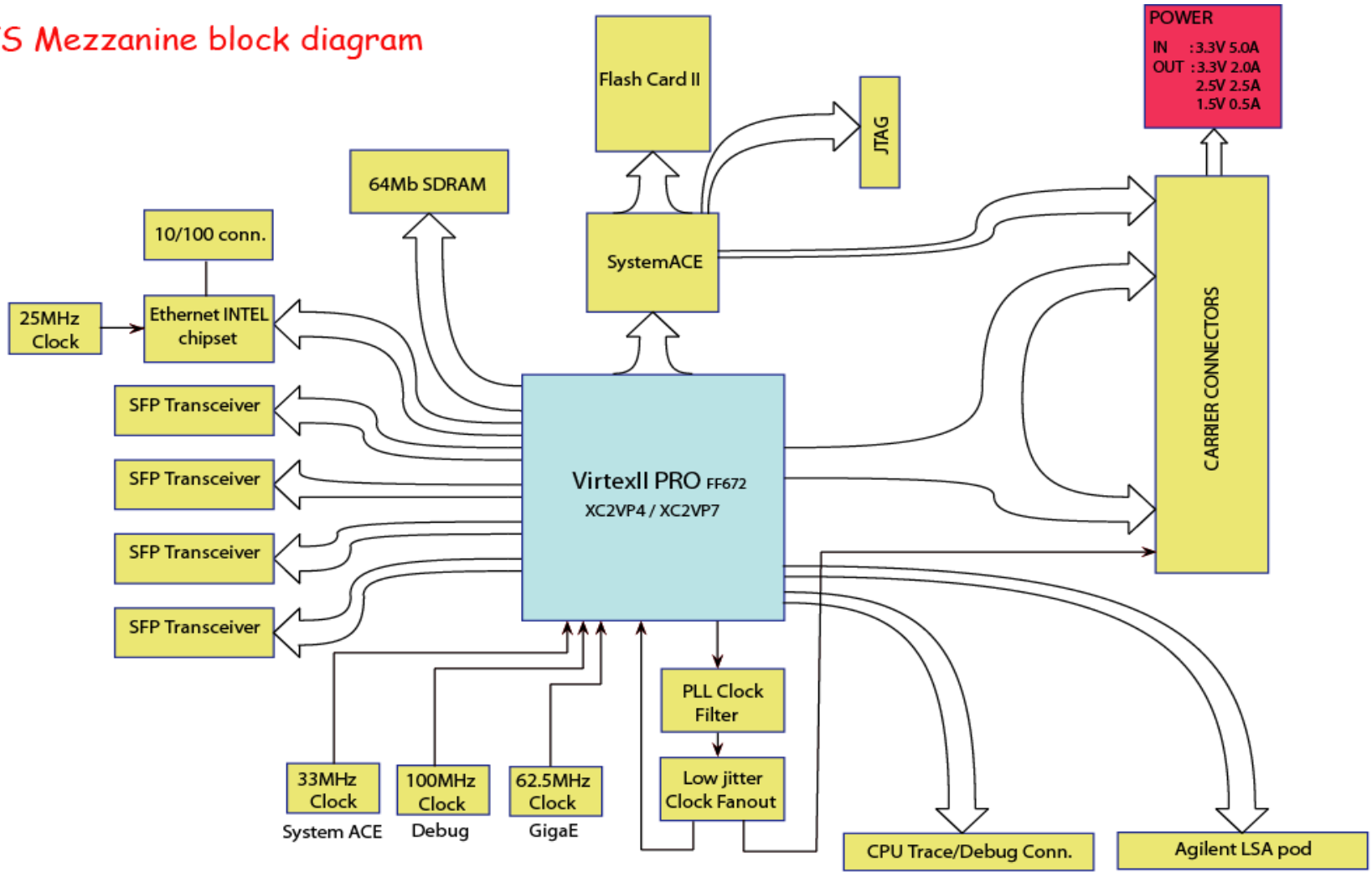


GTS Mezzanine card overview and status

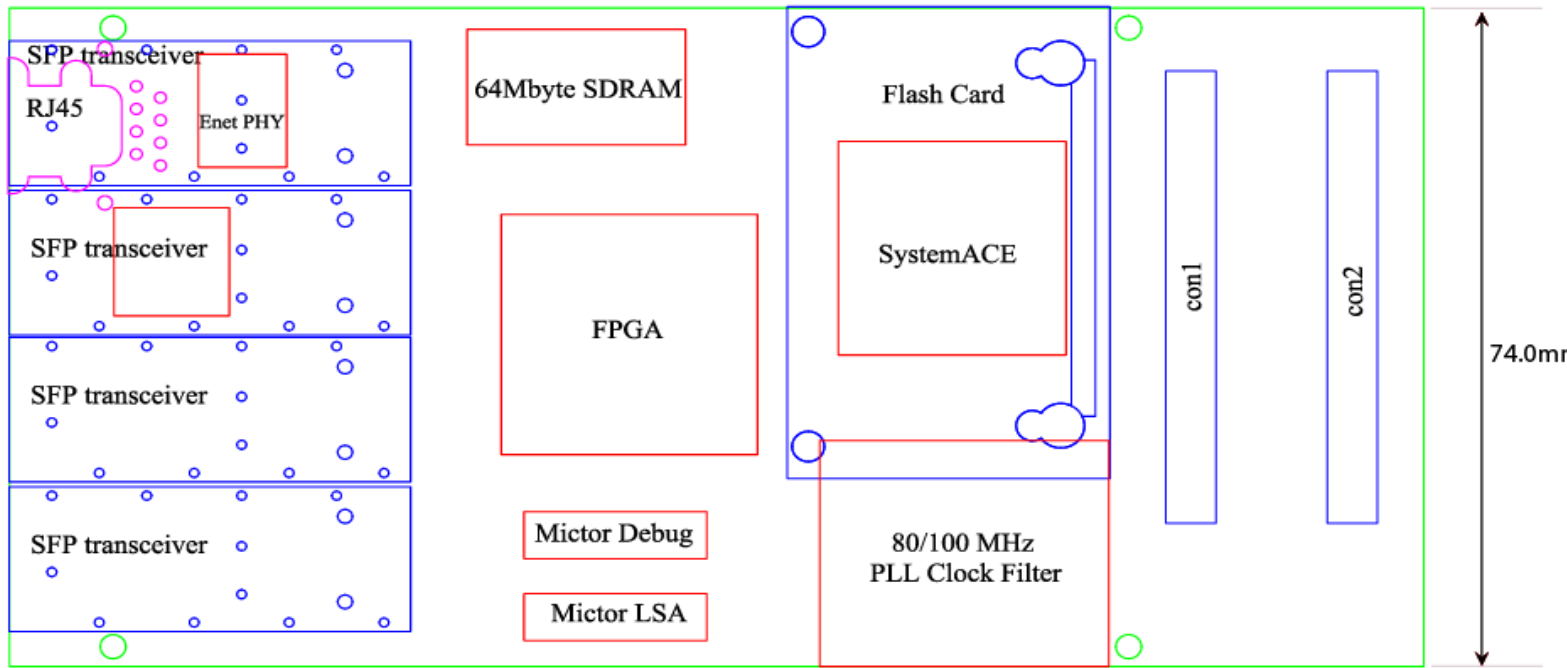
M. Bellato D. Bortolato R. Isocrate
INFN Sezione di Padova

GTS Mezzanine block diagram



GTS Mezzanine PCB Layout

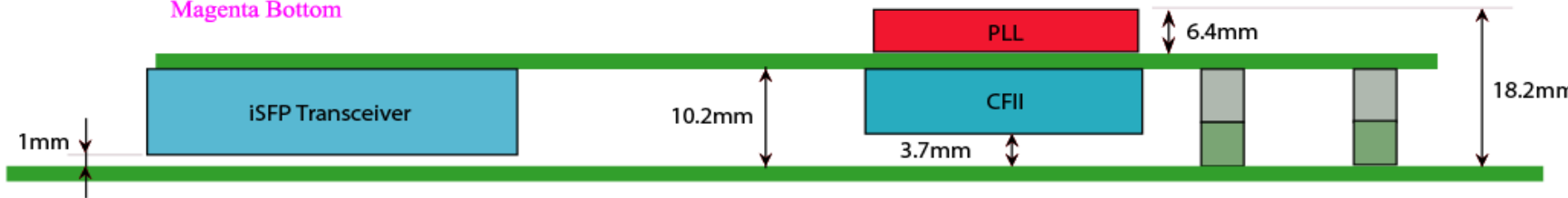
Top view



149.0mm

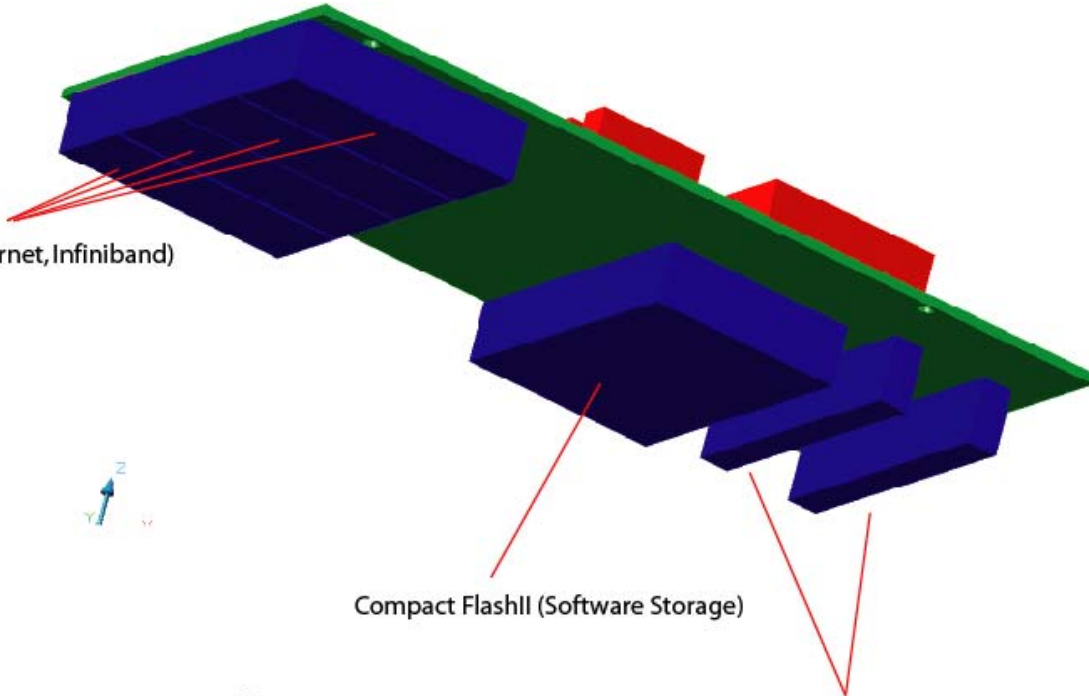
74.0mm

RED Top
BLUE Bottom
Magenta Bottom



GTS Mezzanine Layout

4 iSP Transceivers (Fibre Channel, GigaEthernet, Infiniband)



Compact FlashII (Software Storage)

Carrier connectors (Tyco Mictor)
up to 118 I/O LVCMOS25 or 59 I/O LVDS25/LVPECL25
and JTAG Interface (Fpga program, OS boot)

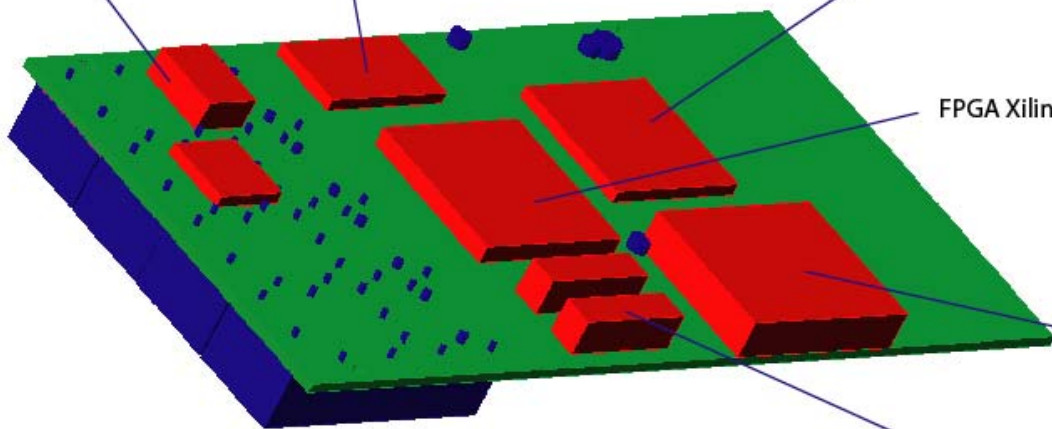
Ethernet 10/100 Phy Layer
64 Mbytes SDRAM

System ACE configurator

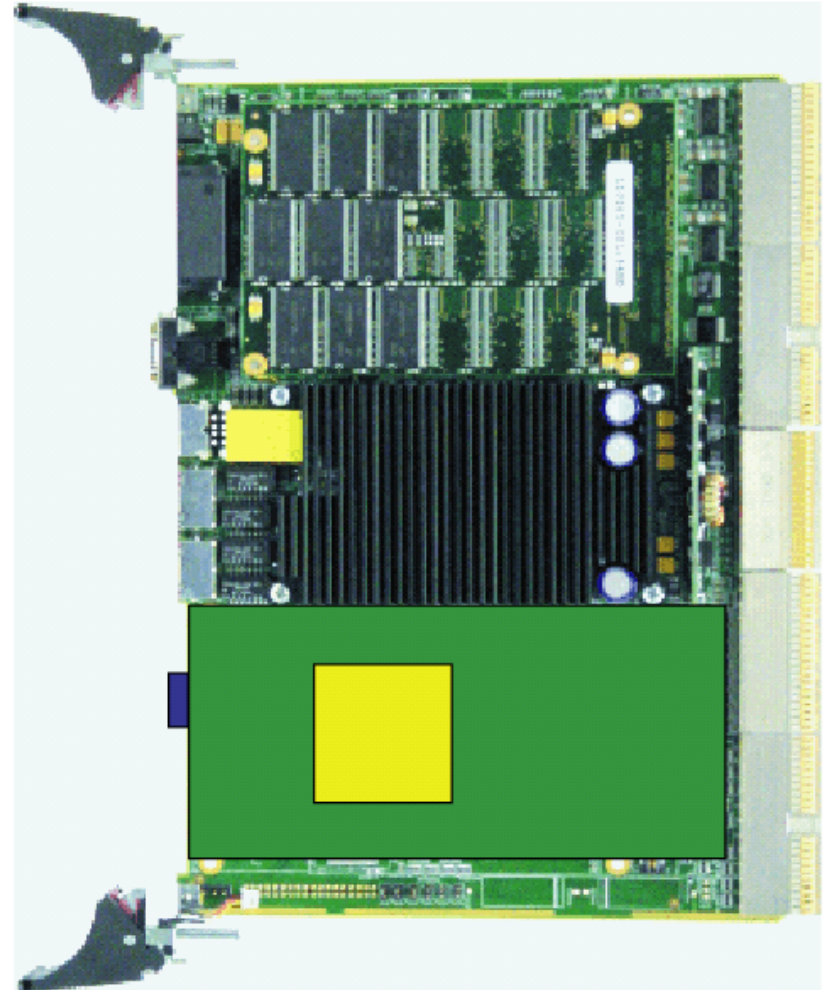
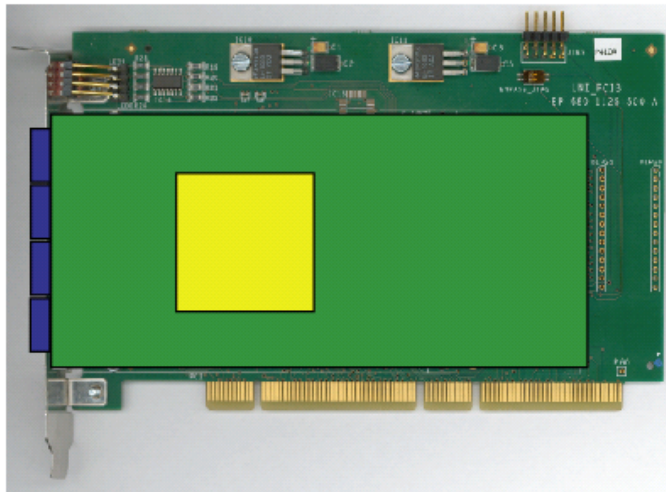
FPGA Xilinx FF672 XC2VP4 or XC2VP7

PLL Clock Filter 80/100MHz

CPU Trace & Debug and Agilent LSA Interfaces

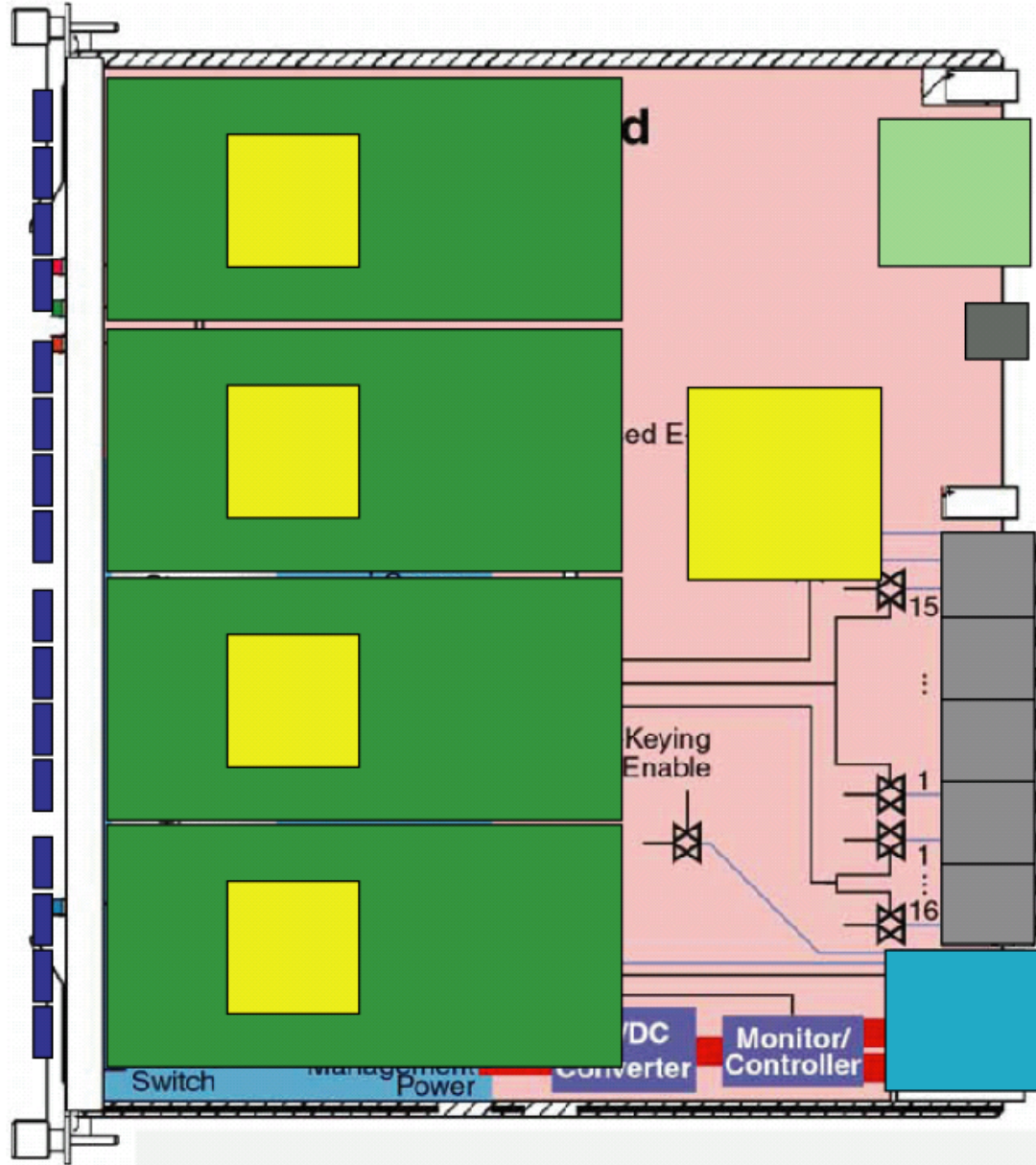


GTS Mezzanine on GIII PCI Card (Test and Debug) and on a cPCI LLP Carrier



GTS Mezzanine on ATCA Fanout board

4x4 SFP Transceivers on
4 GTS Mezzanine Cards



Compact Flash II Card

Ethernet 10/100

Zone1 connectors

-48v Power supply

Keying Enable

DC Converter
Monitor/Controller

Switch
Management Power

GTS Mezzanine Inputs Outputs 1

Front Panel :

up to 4 iSFP Transceiver

1 10/100 Ethernet RJ45 connector (instead of 2 transceiver)

Led for status indications

On board (for debug):

SMA clock injector

Mictor connectors for trace and debug of CPU and for Agilent LSA

On carrier connectors : Two 114 pin Mictors that include :

1 differential clean clock output (LPECL33 80/100MHz Jitter <60ps rms)

13 Fpga I/O (LVTTTL25)

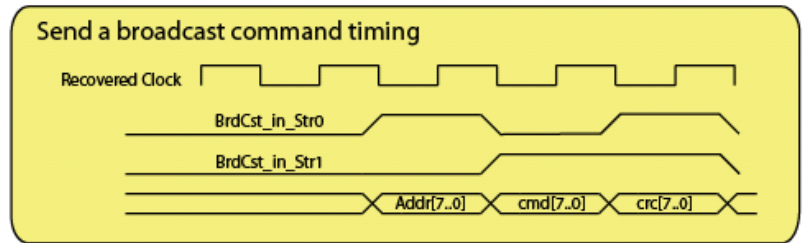
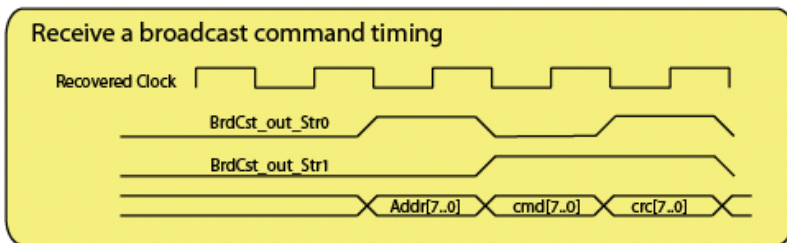
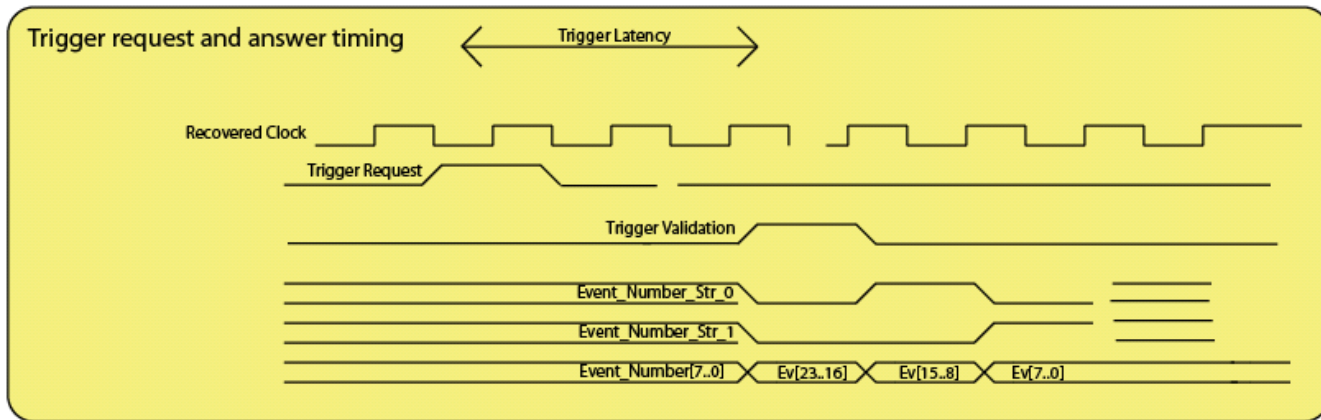
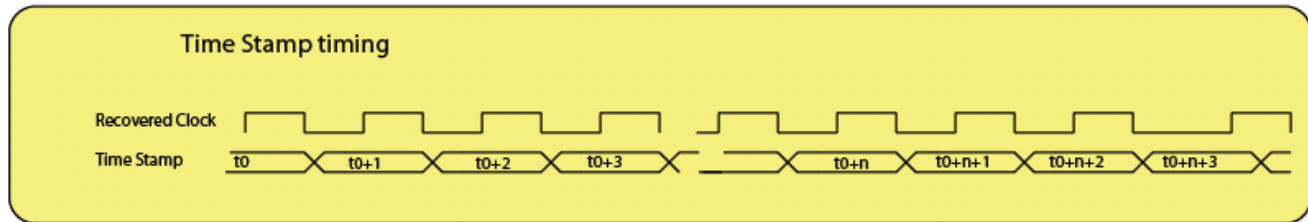
10 Dedicated pins for JTAG interface and SysAce management

128 Fpga I/O (LVTTTL25) or 64 FPGA Differential I/O (LVPECL25 , LVDS25)

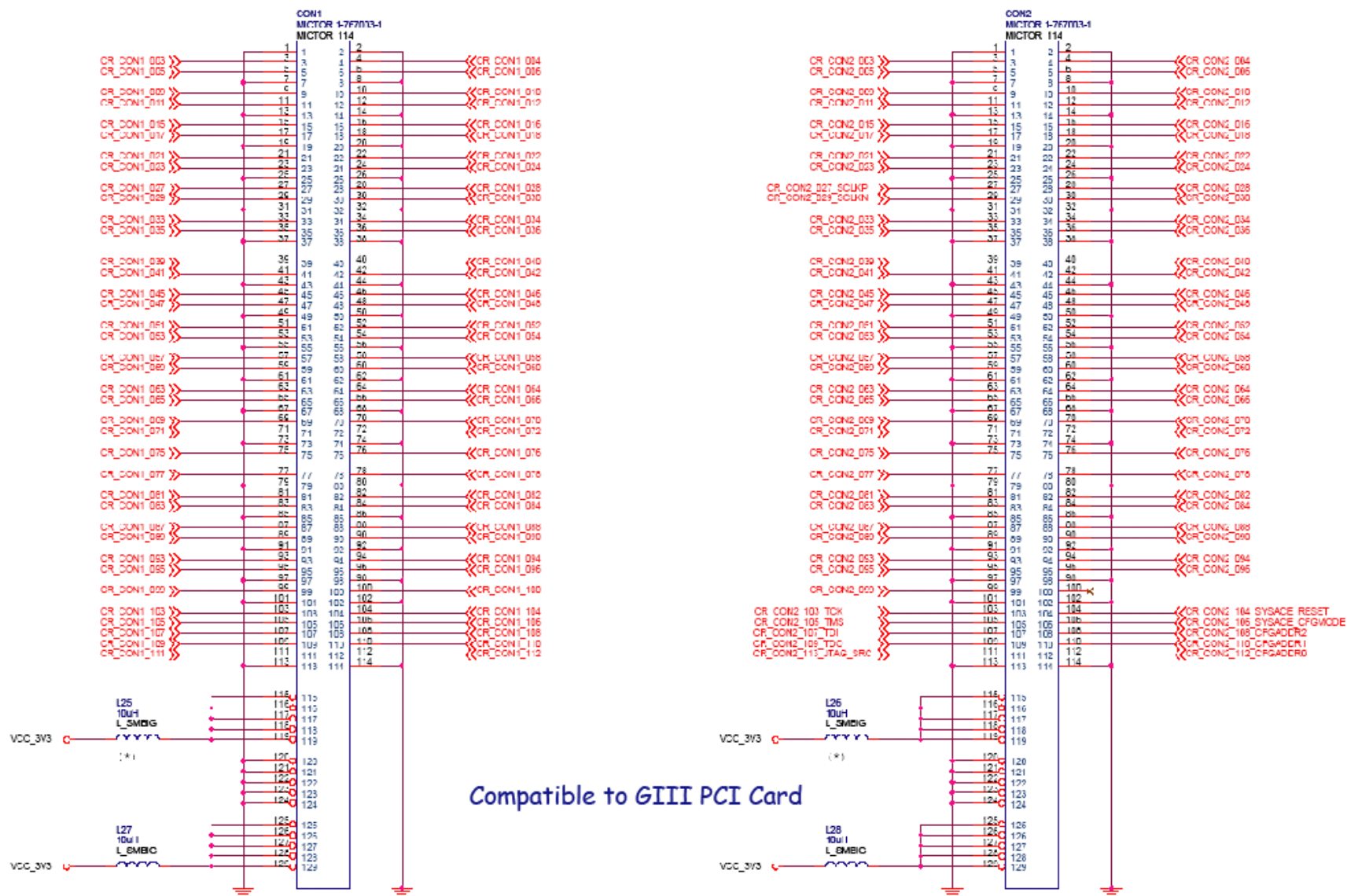
Power Supply :

3,3 volt 5A max 16.5Watt (16pin @ 3,3v , 8pin @ GND)

GTS Mezzanine data exange protocol



GTS Mezzanine to Carrier Connectors



GTS Mezzanine Inputs Outputs 2

Signal Name	Pins	Level	Comments
Time_Stamp [47..0]	48	LVTTTL25	Time stamp
Clean_Clock	2	LVPECL33	Clean Clock 80/100MHz jitter cyle-cycle <60ps rms
Trigger_Request	1	LVTTTL25	
Trigger_Validation	1	LVTTTL25	
BackPressure	1	LVTTTL25	Low latency backpressure command
Event_number [7..0]	8	LVTTTL25	Event TAG associate with validation
Event_Number_Str_0	1	LVTTTL25	Strobe (see Timing diagram)
Event_Number_Str_1	1	LVTTTL25	
Bcast_in [7..0]	8	LVTTTL25	Commands TO GTS
Bcast_in_Str_0	1	LVTTTL25	Strobe (see Timing diagram)
Bcast_in_Str_1	1	LVTTTL25	
Bcast_out [7..0]	8	LVTTTL25	Commands FROM GTS
Bcast_out_Str_0	1	LVTTTL25	Strobe (see Timing diagram)
Bcast_out_Str_1	1	LVTTTL25	
JTAG_Port	4	LVTTTL25	JTAG port for the FPGA
JTAG_Src	1	LVTTTL25	Only for debug (on carrier always 0)
SysAce_Reset	1	LVTTTL25	
SysAce_Cfgmode	1	LVTTTL25	Only for debug (on carrier always 0)
SysAce_CfgAddr [2..0]	3	LVTTTL25	flash card software selection
Ethernet_P0_P		?TBD?	
Ethernet_P0_N		?TBD?	WARNING !! High power analog signals
Ethernet_P1_P		?TBD?	cannot be routed on PCB
Ethernet_P1_N		?TBD?	
LTX971BUS	22	LVTTTL25	Ethernet Port chipset
Master_Reset_0	1	LVTTTL25	Four type of synchronous reset are defined
Master_Reset_1	1	LVTTTL25	
System_Error_0	1	LVTTTL25	Four type of error condition are defined
System_Error_1	1	LVTTTL25	
Power_3V3	4		
Power_2V5	4		
Power_GND	4		
Total # of pins		133/153	

