GTS Mezzanine card overview and status

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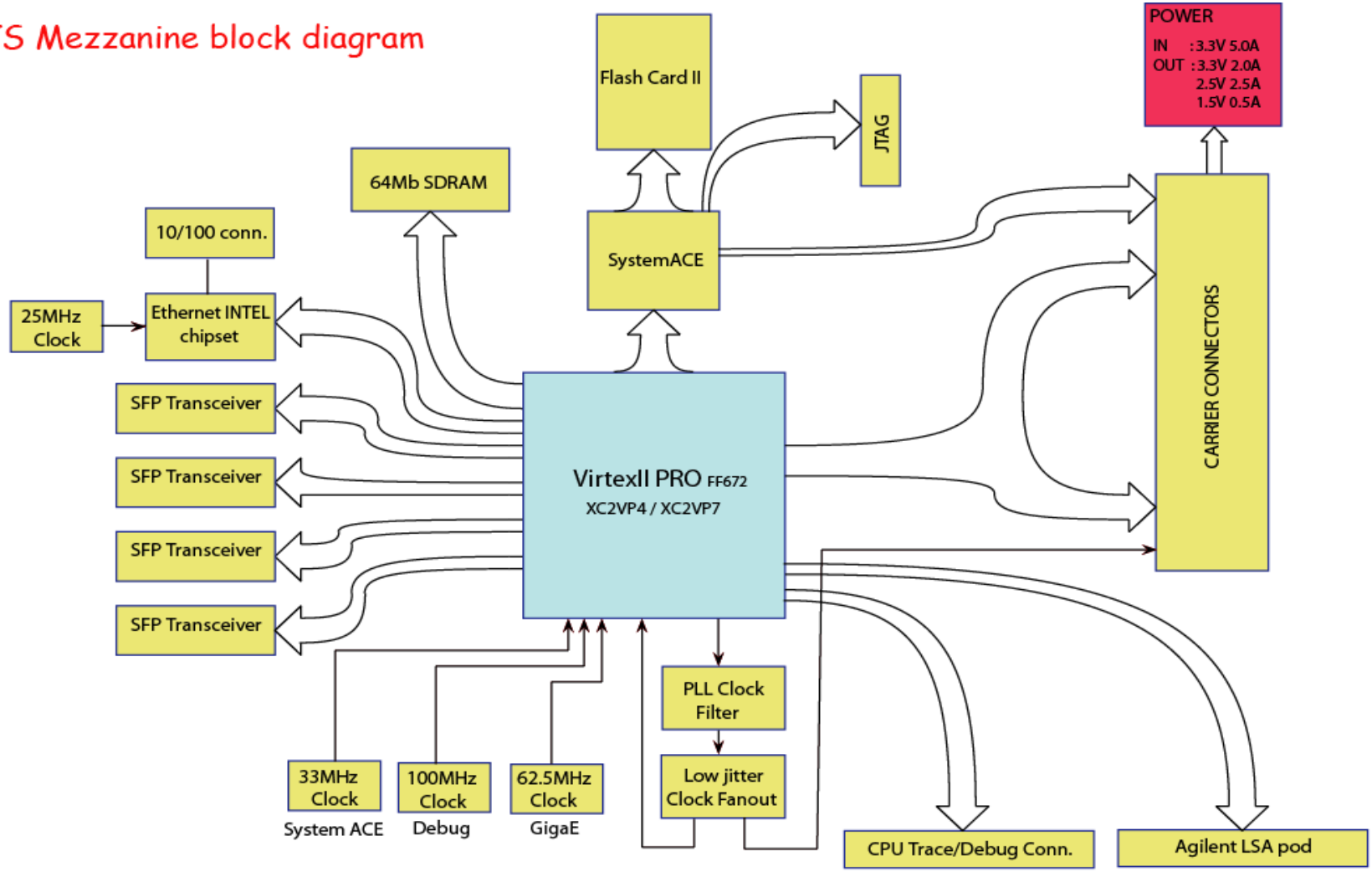
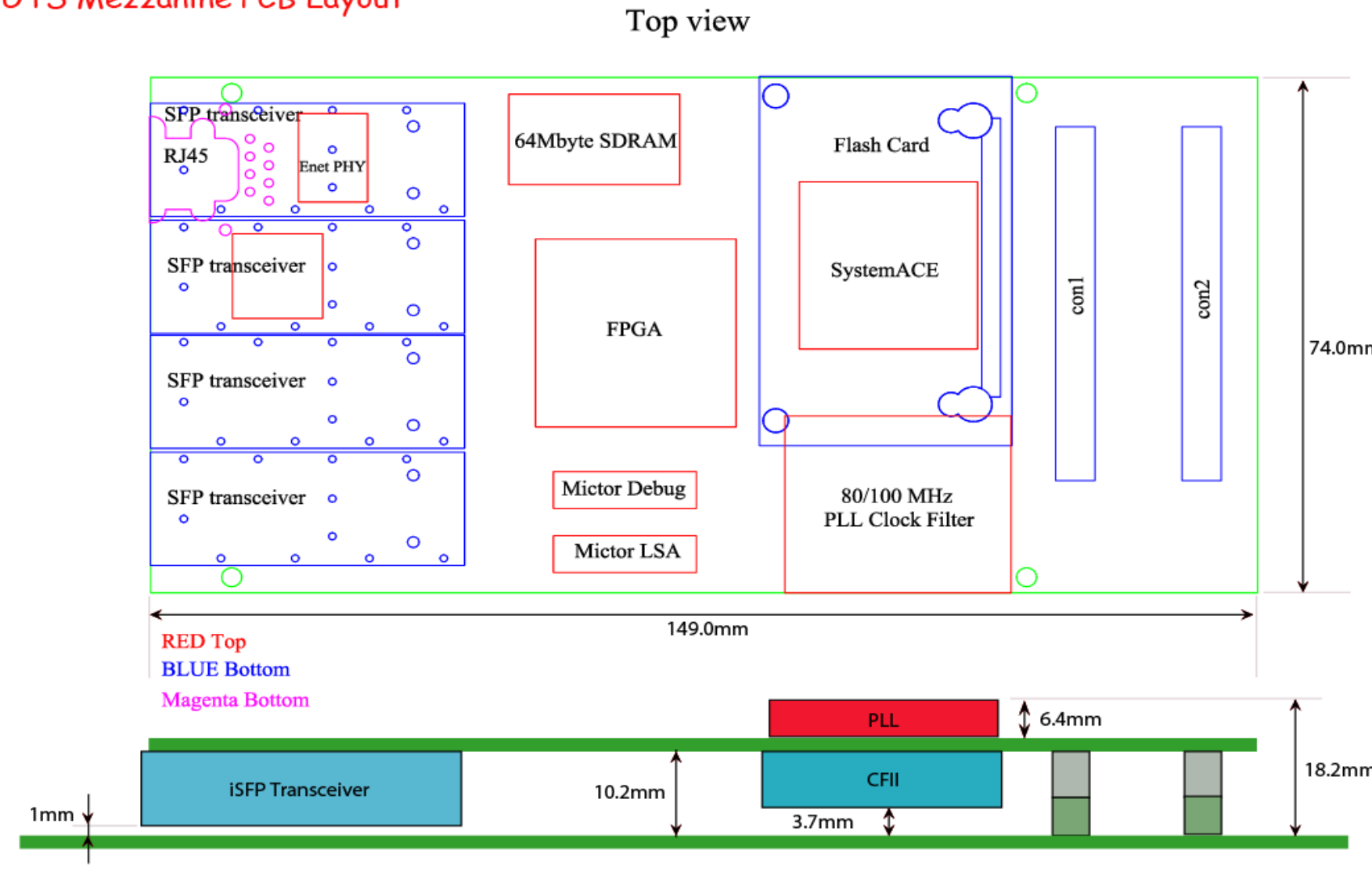
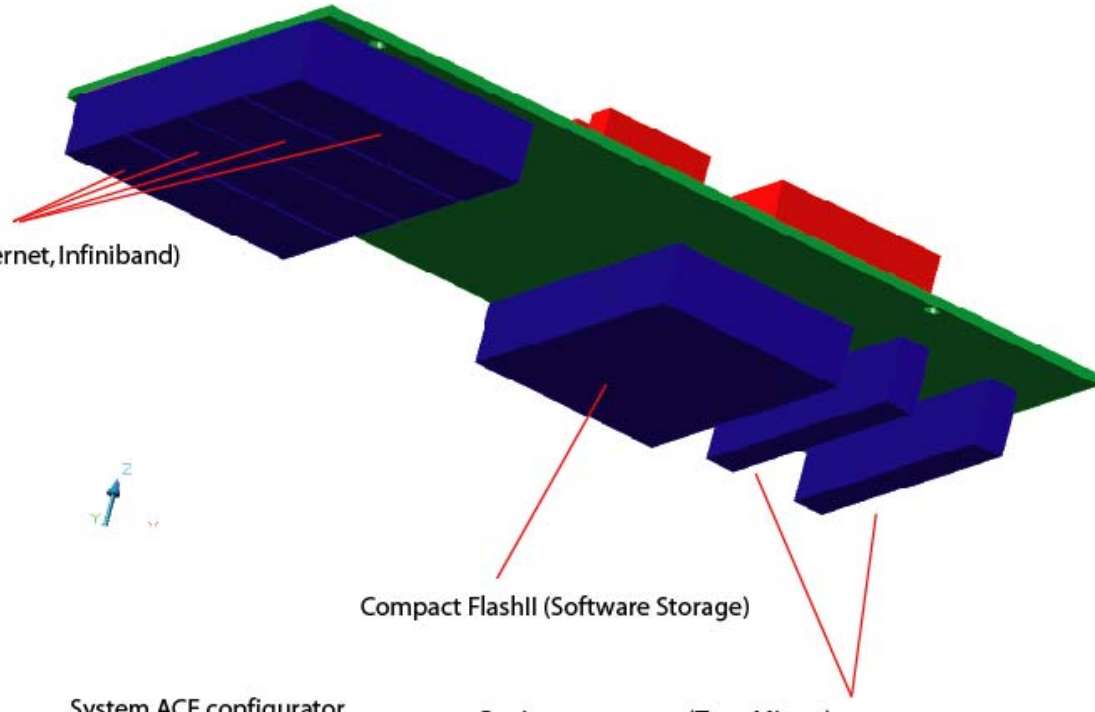
GTS Mezzanine block diagram

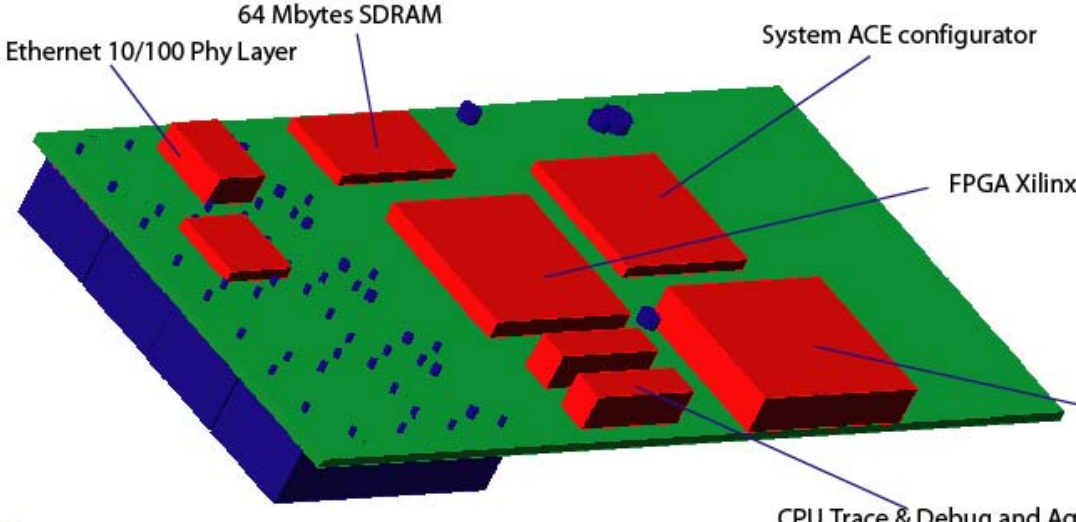


GTS Mezzanine PCB Layout

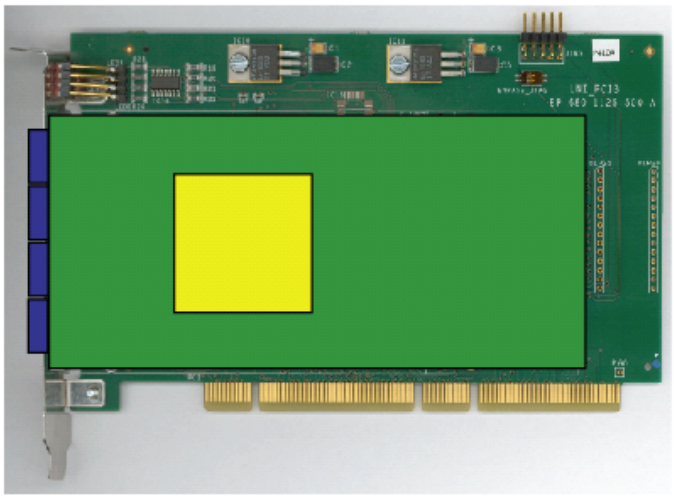


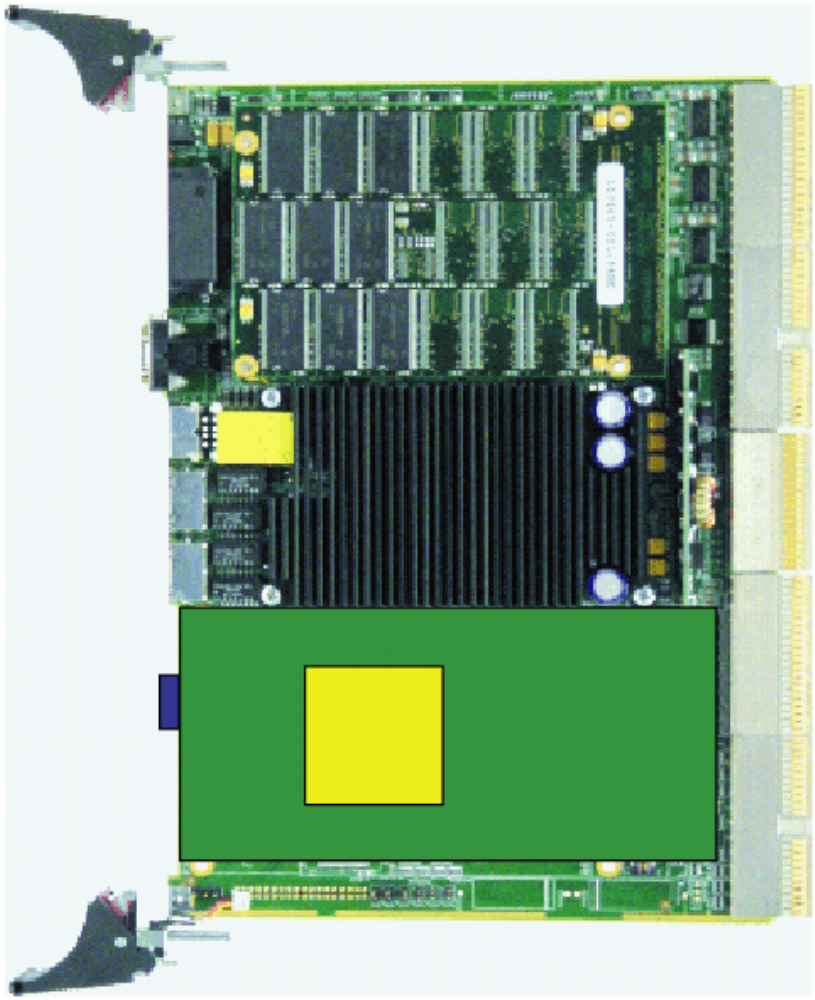
GTS Mezzanine Layout





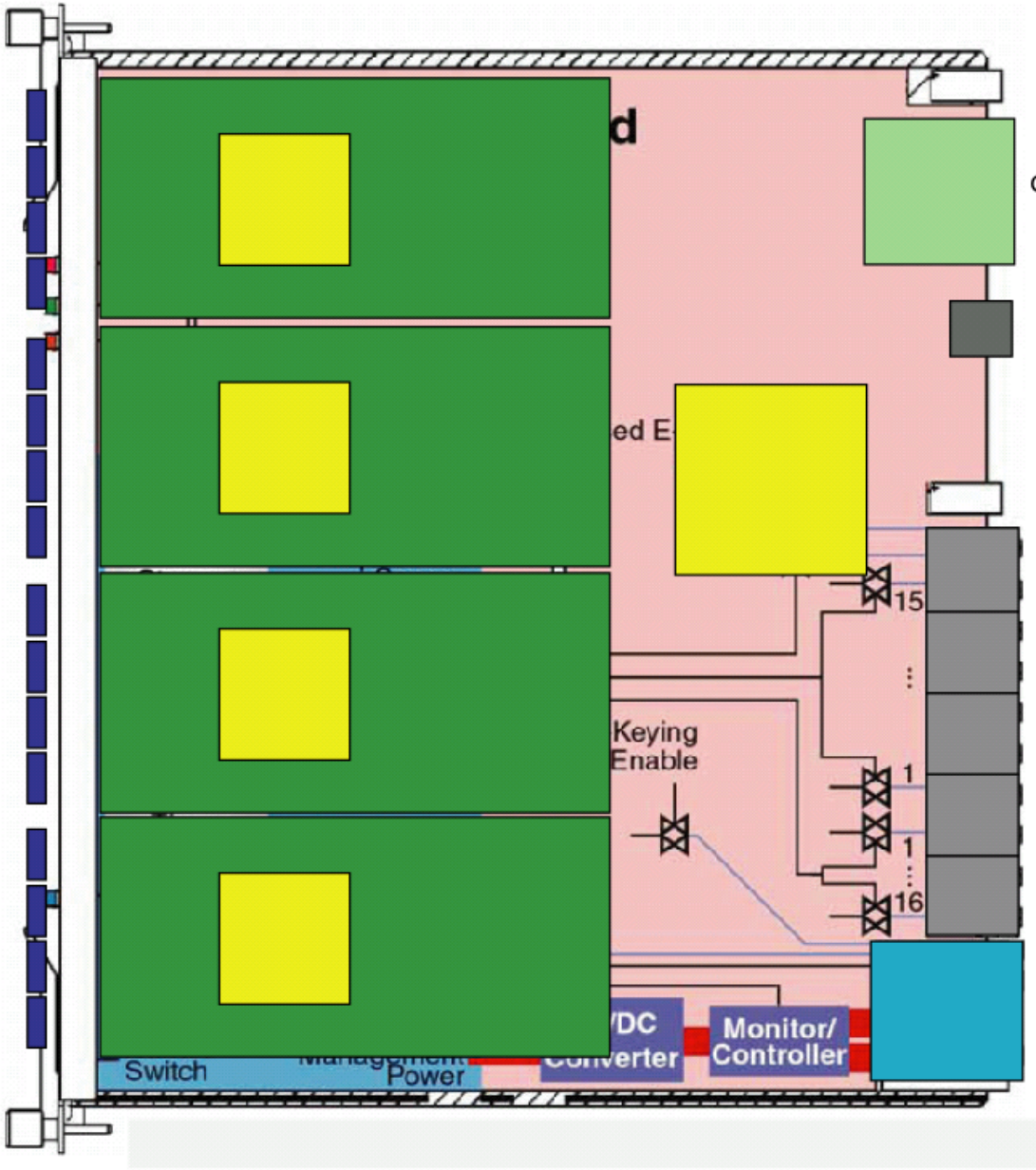
GTS Mezzanine on GIII PCI Card (Test and Debug) and on a cPCI LLP Carrier





GTS Mezzanine on ATCA Fanout board

4x4 SFP Transceivers on
4 GTS Mezzanine Cards



GTS Mezzanine Inputs Outputs 1

Front Panel :

up to 4 iSFP Transceiver

1 10/100 Ethernet RJ45 connector (instead of 2 transceiver)

Led for status indications

On board (for debug):

SMA clock injector

Mictor connectors for trace and debug of CPU and for Agilent LSA

On carrier connectors : Two 114 pin Mictors that include :

1 differential clean clock output (LPECL33 80/100MHz Jitter <60ps rms)

13 Fpga I/O (LVTTL25)

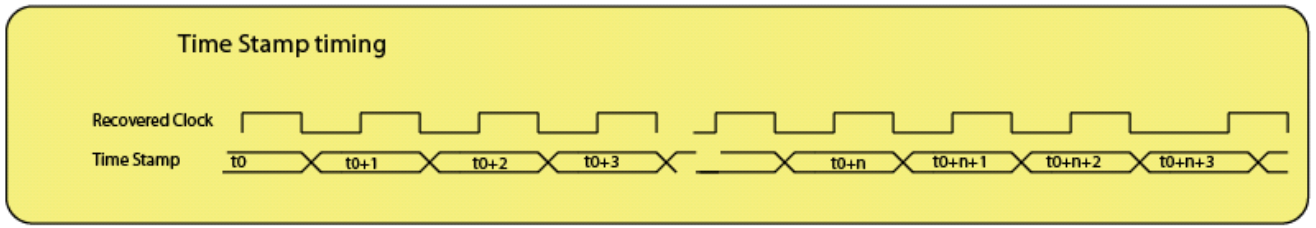
10 Dedicated pins for JTAG interface and SysAce management

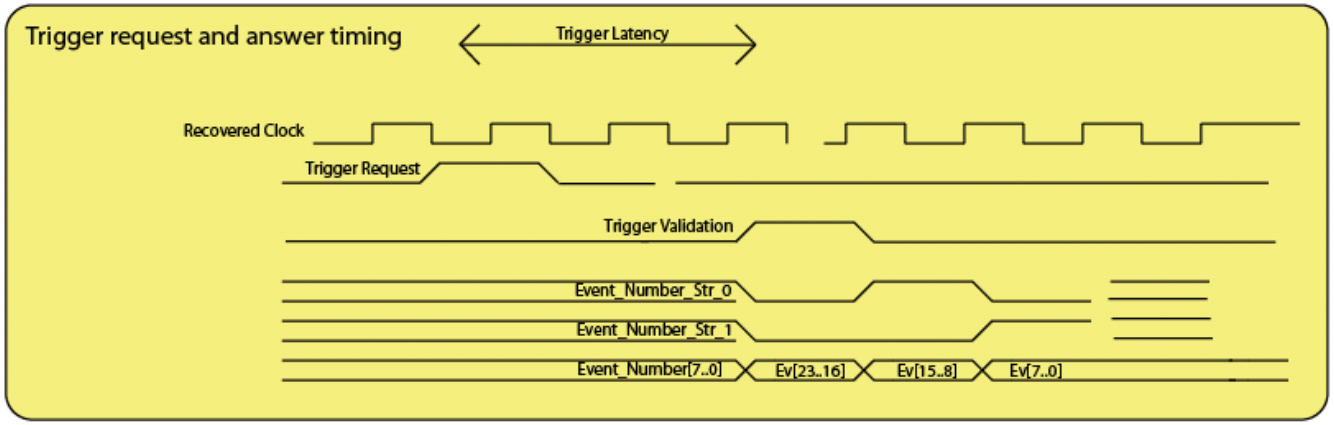
128 Fpga I/O (LVTTL25) or 64 FPGA Differential I/O (LVPECL25 , LVDS25)

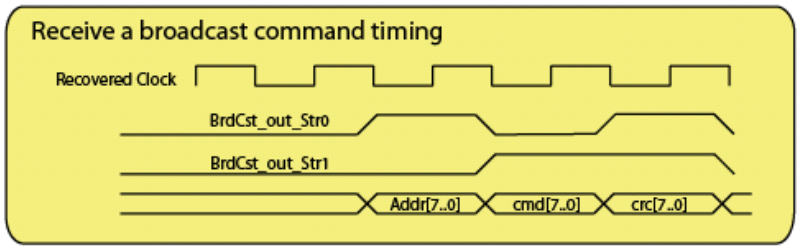
Power Supply :

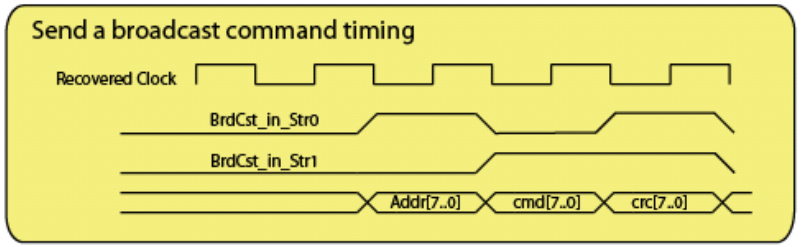
3,3 volt 5A max 16.5Watt (16pin @ 3,3v , 8pin @ GND)

GTS Mezzanine data exange protocol

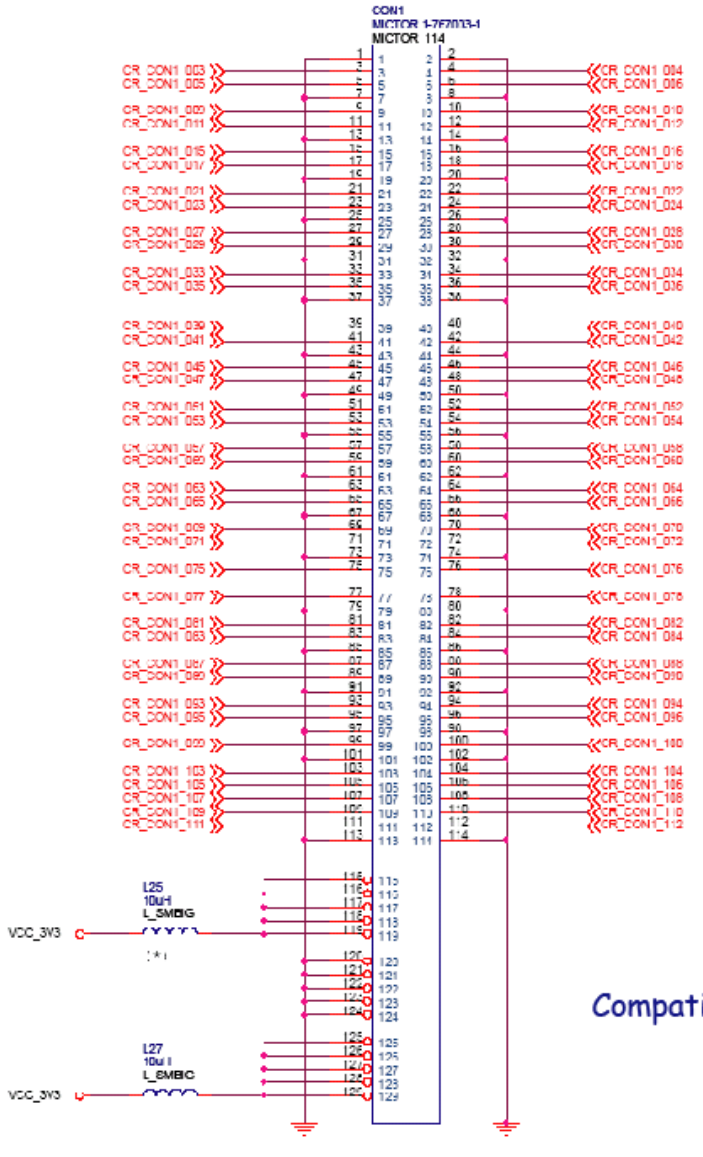


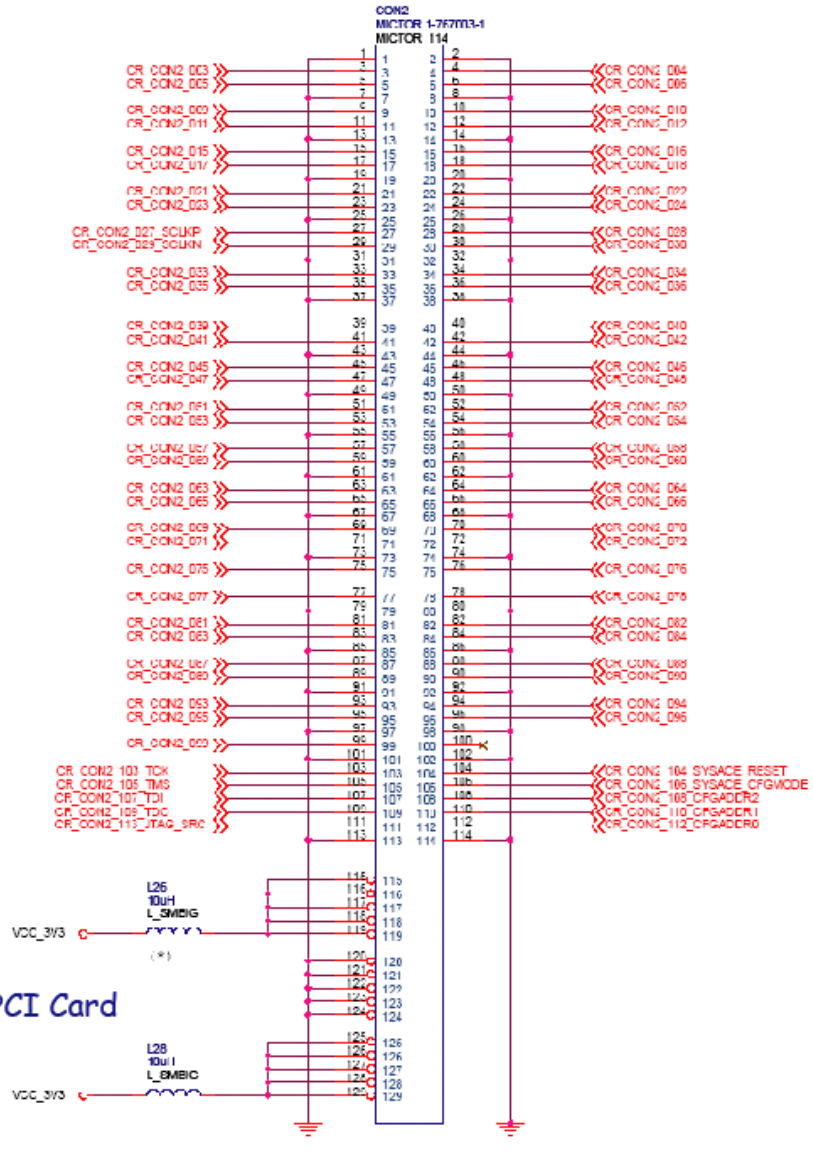






GTS Mezzanine to Carrier Connectors





Compatible to GIII PCI Card

GTS Mezzanine Inputs Outputs 2

Signal Name	Pins	Level	Comments
Time_Stamp [47..0]	48	LVTTL25	*Time stamp*
Clean_Clock	2	LVPECL33	*Clean Clock 80/100MHz jitter cyle-cycle <60ps rms*
Trigger_Request	1	LVTTL25	
Trigger_Validation	1	LVTTL25	
BackPressure	1	LVTTL25	*Low latency backpressure command*
Event_number [7..0]	8	LVTTL25	*Event TAG associate with validation*
Event_Number_Str_0	1	LVTTL25	*Strobe (see Timing diagram)*
Event_Number_Str_1	1	LVTTL25	
Bcast_in [7..0]	8	LVTTL25	*Commands TO GTS*
Bcast_in_Str_0	1	LVTTL25	*Strobe (see Timing diagram)*
Bcast_in_Str_1	1	LVTTL25	
Bcast_out [7..0]	8	LVTTL25	*Commands FROM GTS*
Bcast_out_Str_0	1	LVTTL25	*Strobe (see Timing diagram)*
Bcast_out_Str_1	1	LVTTL25	
JTAG_Port	4	LVTTL25	*JTAG port for the FPGA*
JTAG_Src	1	LVTTL25	*Only for debug (on carrier always 0)*
SysAce_Reset	1	LVTTL25	
SysAce_Cfgmode	1	LVTTL25	*Only for debug (on carrier always 0)*
SysAce_CfgAddr [2..0]	3	LVTTL25	*flash card software selection*
Ethernet_P0_P		?TBD?	
Ethernet_P0_N		?TBD?	*WARNING !! High power analog signals*
Ethernet_P1_P		?TBD?	*cannot be routed on PCB*
Ethernet_P1_N		?TBD?	
LTX971BUS	22	LVTTL25	*Ethernet Port chipset*
Master_Reset_0	1	LVTTL25	*Four type of synchronous reset are defined*
Master_Reset_1	1	LVTTL25	
System_Error_0	1	LVTTL25	*Four type of error condition are defined*
System_Error_1	1	LVTTL25	
Power_3V3	4		
Power_2V5	4		
Power_GND	4		
Total # of pins		**133/153**	