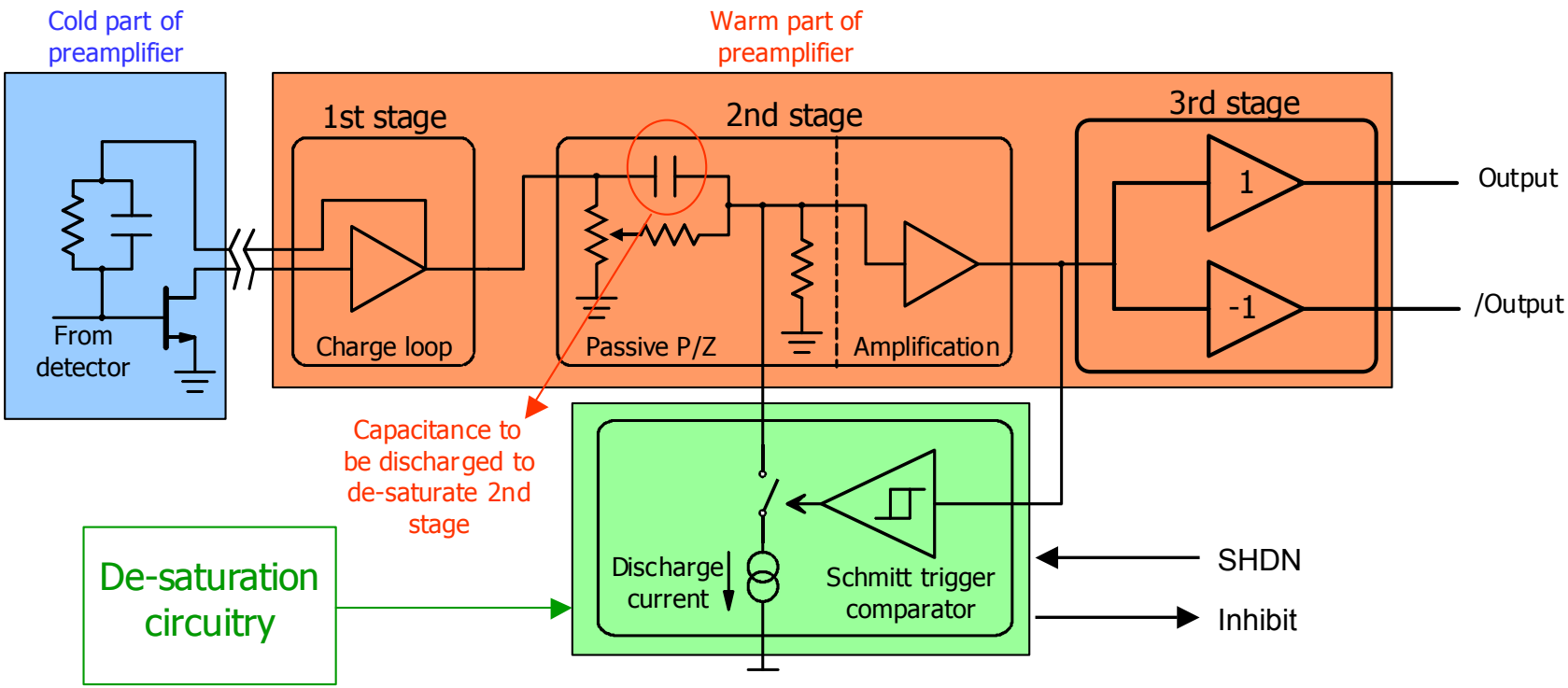
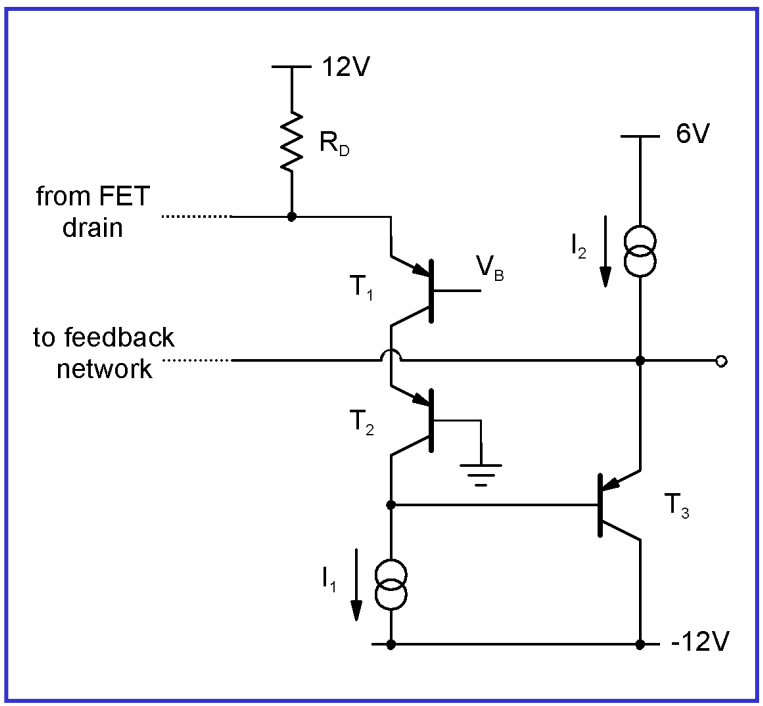
AGATA preamplifiers & interfaces

A. Pullia - AGATA LLP Interfaces meeting, Orsay 24 March 2004

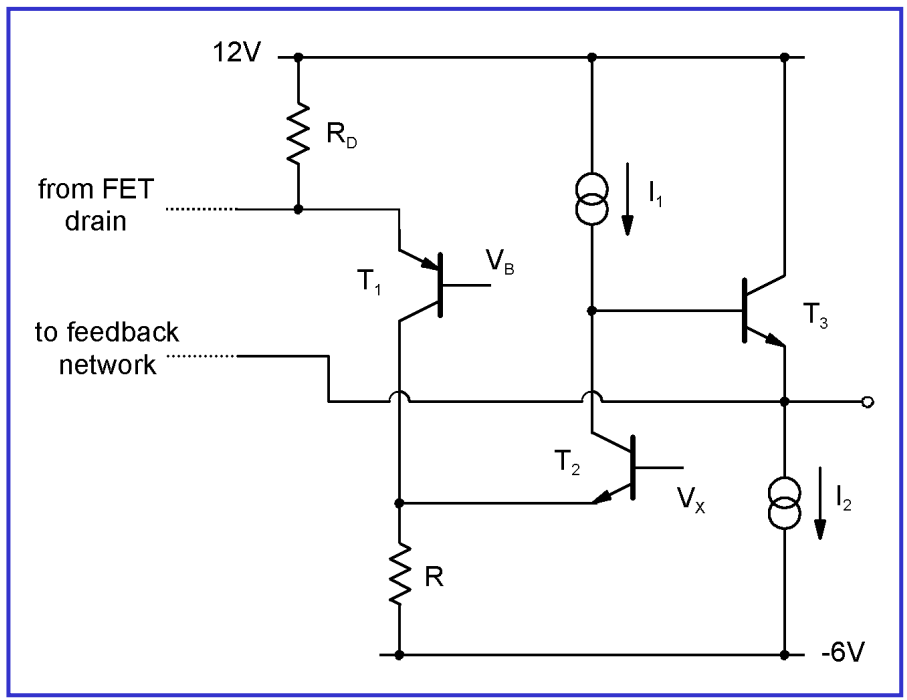
Preamplifier architecture



First-stage structure

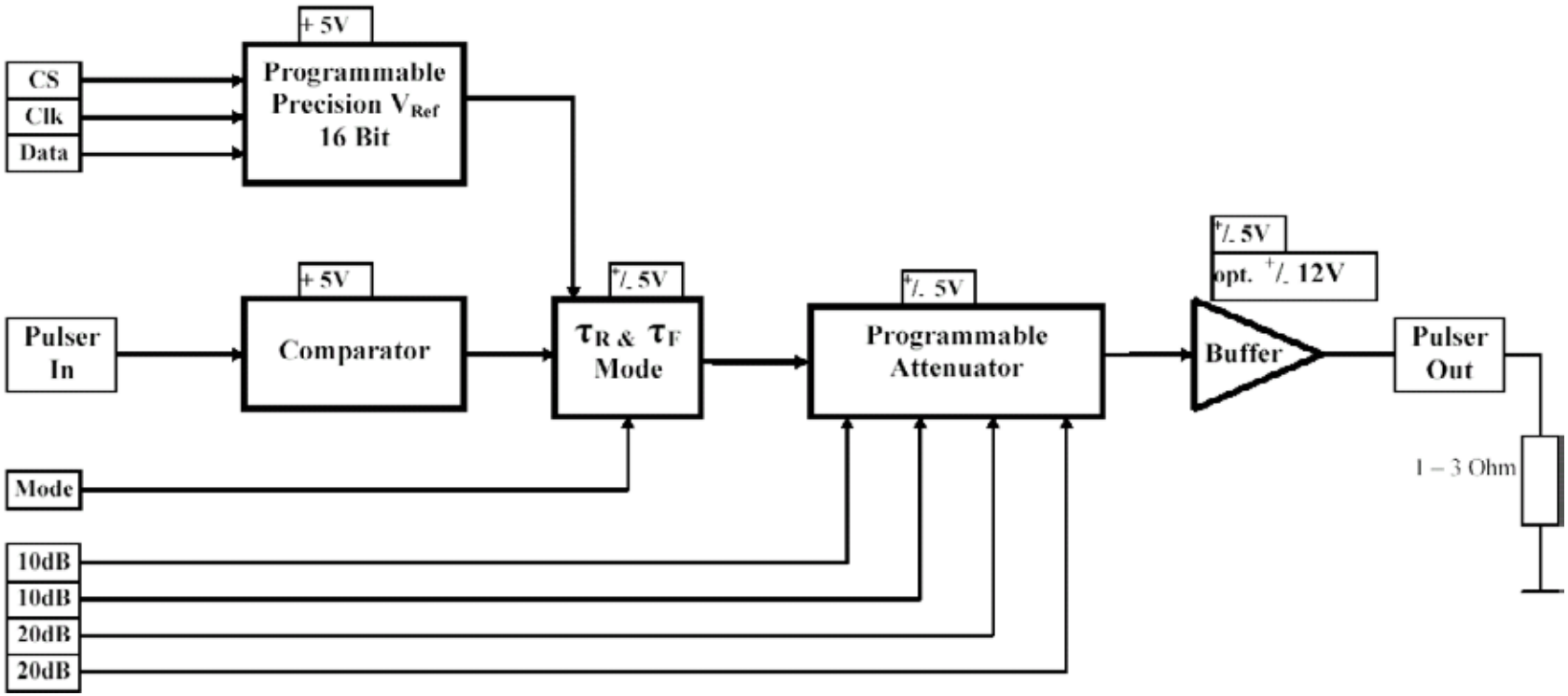


Segment-preamplifier first stage

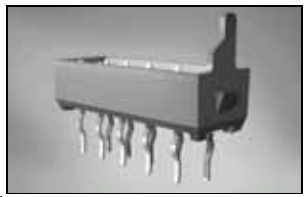


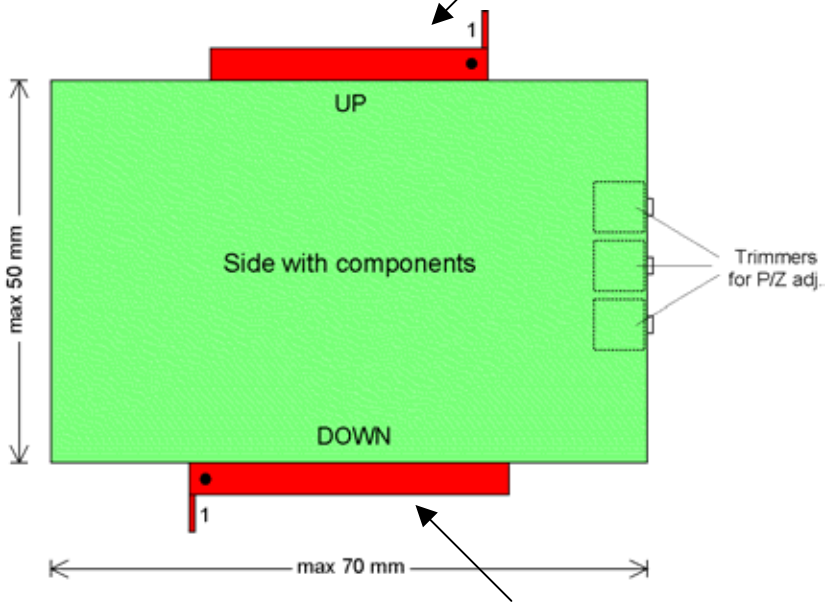
Core-preamplifier first stage

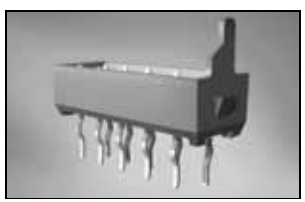
Built-in pulser structure

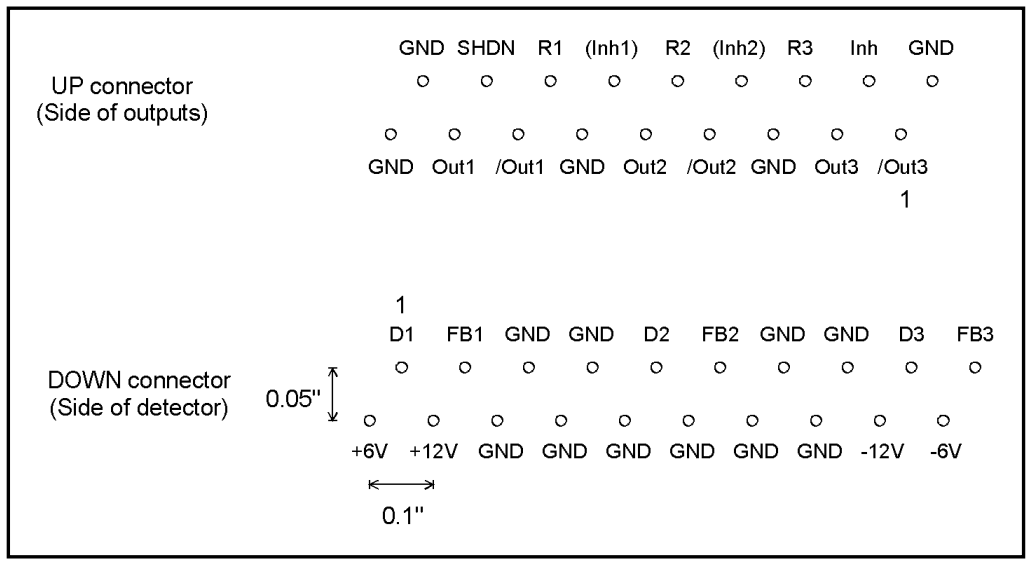


Size and pinout - segment preamps

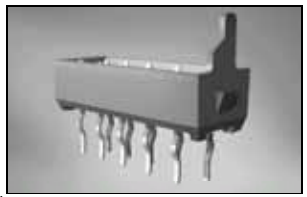


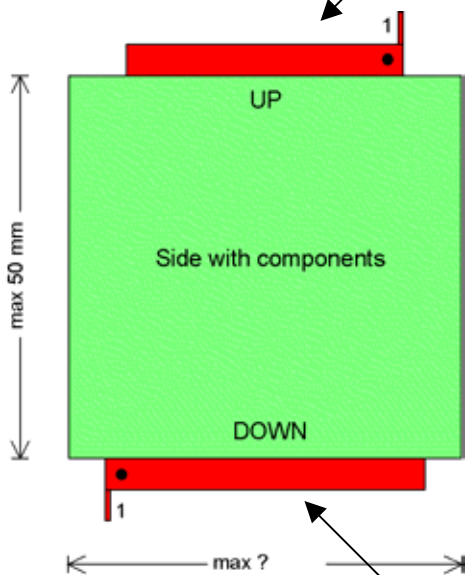


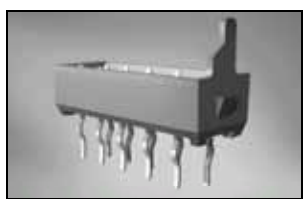




Size and pinout – core preamp & pulser







UP connector
(Side of outputs)

Clk	DIN	MODE	AT20	AT10	GND	EN_PS	GND	SHDN
/CS	Pulser In	GND	AT20	AT10	out	/out	GND	Inh

1

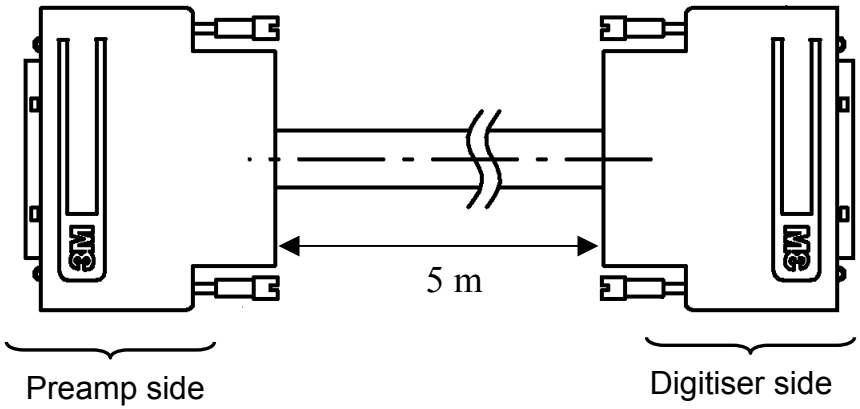
DOWN connector
(Side of detector)

0.05"

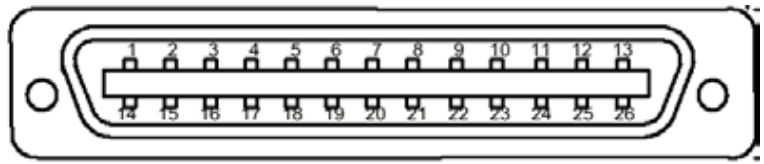
1 S	GND	GND	GND	GND	GND	GND	GND	FB	D
GND	+6V	+6V	+12V	+12V	-12V	-12V	-6V	-6V	GND

0.1"

Cables & interface specifications



MDR 26-via male connector



Pin/twisted-pair association

Preamp side	*Digitiser side*	*Cable name*	*Preamp side*	*Digitiser side*	*Cable name*	*Preamp side*	*Digitiser side*	*Cable name*	*Preamp side*	*Digitiser side*	*Cable name*
1	1	shield	17	10	pair 3+	8	19	pair 7-	24	3	pair 10+
14	14	shield	5	22	pair 4-	21	6	pair 7+	12	15	pair 11-
2	25	pair 1-	18	9	pair 4+	9	18	pair 8-	25	2	pair 11+
15	12	pair 1+	6	21	pair 5-	22	5	pair 8+	13	13	shield
3	24	pair 2-	19	8	pair 5+	10	17	pair 9-	26	26	shield
16	11	pair 2+	7	20	pair 6-	23	4	pair 9+			
4	23	pair 3-	20	7	pair 6+	11	16	pair 10-			

Signals in a segment cable

Type	*Name*	*Source*	*Type / format*	*Q.ty*	*Position*
Analog	Segment	Preamp	Analog signal / 1 differential pair	6	Pairs 1 to 6*
Digital	SHDN_A	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 7+
	SHDN_B	Digitiser	Logic Level/ +5.x V = High, GND = Low	1	Pair 7-
	Reserved	-	For future expansion	1	Pair 9
	Inh_A	Preamp	Digital signal / +5.x V = High, GND = Low	1	Pair 10**
	Inh_B	Preamp	Digital Signal / +5.x V = High, GND = Low	1	Pair 11***
Power	+5.x V	Preamp	Supply for Logic Isolators	1	Pair 8+
	GND	Preamp	Ground	1	Pair 8-
	GND	Preamp	Cable shields & Supply for Logic Isolators	4	pins 1,13,14,26

*Pair i+ is positive swing, pair i- is negative swing, with i=1, 2,...,6

**Pair 10- swings dynamically, pair 10+ is tied to common ground, i.e. to pins 1,13,14,26

***Pair 11+ swings dynamically, pair 11- is tied to common ground, i.e. to pins 1,13,14,26

One cable serves 6 segment preamplifiers (or 2 triple preamplifiers: e.g. preampA tied to segments 1 2 3, and preampB tied to segments 4 5 6).

Signals in the core+pulser cable

Type	*Name*	*Source*	*Type / format*	*Q.ty*	*Position*
Analog	Core	Preamp	Analog signal / 1 differential pair	1	Pair 1*
Digital	AT10	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 2+
	AT10	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 2-
	AT20	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 3+
	AT20	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 3-
	Clk	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 4+
	MODE	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 4-
	DIN	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 5**
	/CS	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 6**
	SHDN_C	Digitiser	Logic Level / GND= High, -5.x V = Low	1	Pair 7+
	EN_PS	Digitiser	Logic Level / +5.x V = High, GND = Low	1	Pair 7-
	Pulser In	Digitiser	Digital Signal / +5.x V = High, GND = Low	1	Pair 8**
	Reserved	-	For future expansion	1	Pair 9
	Inh_C	Preamp	Digital Signal / GND = High, -5.x V = Low	1	Pair 10**
Power	+5.x V	Preamp	Supply for Logic Isolators	1	Pair 11+
	-5.x V	Preamp	Supply for SHDN_C Isolator	1	Pair 11-
	GND	Preamp	Cable shields & Supply for Logic Isolators	4	Pins 1,13,14,26

*Pair 1+ is positive swing, pair 1- is negative swing

**Pair i+ swings dynamically, pair i- is tied to common ground, i.e. to pins 1,13,14,26

One cable serves the core preamplifiers and the built-in pulser

Complete signal list

Type	*Name*	*Source*	*Type / format*	*Quantity*
Analog	Segment	Preamp	Analog signal / 1 differential pair	36
	Core	Preamp	Analog signal / 1 differential pair	1
Digital	Inh_A	Preamp	Digital Signal / +5.x V = High, GND = Low	6
	Inh_B	Preamp	Digital Signal / +5.x V = High, GND = Low	6
	Inh_C	Preamp	Digital Signal / GND = High, -5.x V = Low	1
	SHDN_A	Digitiser	Logic Level / +5.x V = High, GND = Low	6
	SHDN_B	Digitiser	Logic Level / +5.x V = High, GND = Low	6
	SHDN_C	Digitiser	Logic Level / GND = High, -5.x V = Low	1
	AT10	Digitiser	Logic Level / +5.x V = High, GND = Low	2
	AT20	Digitiser	Logic Level / +5.x V = High, GND = Low	2
	EN_PS	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	MODE	Digitiser	Logic Level / +5.x V = High, GND = Low	1
	Clk	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
	DIN	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
	/CS	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
	Pulser In	Digitiser	Digital Signal / +5.x V = High, GND = Low	1
Power	+5.x V	Preamp	Supply for Logic Isolators except for Inh_C	7
	-5.x V	Preamp	Supply for Inh_C Isolator	1
	GND	Preamp	Cable shields & Supply for all Logic Isolators	28

Note: all Digital Signals and Logic Levels across the interface will be isolated at the Digitizer using the Analog Devices part ADuM1100.

Signal description

Segment
Differential Analog signal pair. -2.5 V to +2.5 V.

Core
Differential Analog signal pair. -2.5 V to +2.5 V.

Inh_A, and Inh_B
Active High
(set dynamically by preamplifiers A and B)
This is a digital signal (TTL) that will be pulled up if any of the preamplifiers in triples A and B is undergoing a fast reset. It will be pulled down as soon as the fast reset is over. This can be used to inhibit acquisition of false events due to a reset transient. A source termination on the preamp side will be used. Please put no termination resistor on the receiver side to avoid half splitting of the TTL signal. The analog levels for InhibitAB are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the receiver side.

Inh_C
Active High (set dynamically by core preamplifier)
This is a digital signal (TTL) that will be pulled up if the core amplifier is undergoing a fast reset. It will be pulled down as soon as the fast reset is over.
This can be used to inhibit acquisition of false events caused by a reset transient. A source termination on the preamp side will be used. Please put no termination resistor on the receiver side to avoid half splitting of the TTL signal.
The Analog levels for InhibitC are -5.x V (low) (coming with the cable) and detector GND (high). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the receiver side. The isolator in this case works also as a voltage translator.
The width of this signal can be used to estimate the amplitude of the energetic event that caused the saturation. Hence this signal should be tied to a precise counter (with the highest possible clock frequency).

SHDN_A, and SHDN_B

Active High Logic Level.
Switches off fast reset mechanism in triple preamplifiers A and B.
If this is pulled up the fast reset mechanism will be permanently switched off. If this is pulled down the fast reset mechanism will automatically work in each of the six preamplifiers when needed.
This should not be handled dynamically by the Digitiser. The analog levels for SHDN_A, SHDN_B are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

SHDN_C

Active High Logic Level.
Switches off fast reset mechanism in the Core preamplifier.
If this is pulled up the fast reset mechanism will be permanently switched off. If this is pulled down the fast reset mechanism will automatically work when needed.
This should not be handled dynamically by the Digitizer. The analog levels for SHDN_C are -5.x V (low) (coming with the cable) and detector GND (high). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

AT10

Active High Logic Level.
Attenuates pulser amplitude by 10dB.
The analog levels for AT10 are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

AT20

Active High Logic Level.
Attenuates pulser amplitude by 20dB.
The analog levels for AT10 are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

EN_PS

Active High Logic Level.
Switches on the Power Supply of built-in Pulser. If this is pulled up the built-in pulser circuitry is biased. If this is pulled down the Pulser Power Supply is set to 0V. This permits to save power when the Pulser is not used.
This should not be handled dynamically by the Digitiser. The analog levels for EN_PS are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

MODE

Logic Level.
Selects the shape of built-in Pulser. If this is pulled up the built-in pulser provides a positive exponential decay. If this is pulled down the built-in pulser provides a square wave.
The analog levels for EN_PS are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

Clk, DIN, /CS

Digital Signals (Clock, Data In, Chip Select) used to set the pulser fine gain.
These signals implement a simple, low-frequency, 3-wire interface through which the 16-bit input of DAC AD5542 from Analog Devices is supplied, which sets the fine gain of the pulser. The maximum clock frequency is 25MHz but it is advisable to use a substantially lower frequency (e.g. 1 MHz). The protocol of this interface can be found on the data sheet of AD5542. It is advisable to use only large numeric values (in the range from 50 to 100% of the full scale) for fine-gain corrections. Otherwise the long-term stability of the pulser could worsen significantly. Use instead AT10 and/or AT20 for coarse-gain setting. The analog levels for Clk, DIN, /CS are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the digitiser side.

Pulser In

Active High Digital Signal.
This is a digital signal (TTL) that will be pulled up to generate a positive transition of the pulser and down to reset it, or generate a negative transition edge (depending on setting of MODE).
The analog levels for Pulser In are detector GND (low) and +5.x V (high) (coming with the cable). So please use such Power Supply voltages on the isolator on the cable side. Use instead the receiver 0V 5V PS levels on the receiver side.

+5.x V

Power supply provided by the preamplifiers for the Logic isolators except for the core Inhibit. The actual value will range between +5 and +6 V.

-5.x V

Power supply provided by the core preamplifier for the Logic isolator for the core Inhibit. The actual value will range between -5 and -6 V.

GND

All grounds, including the internal shieldings are to be connected at the preamplifier side and should not be connected to the digitiser's ground.

FUTURE UPGRADE

In a future version the spare twisted pairs could be used as a serial transmission link (lvds) from the receiver to the triples/core preamplifiers (using a microcontroller to receive and distribute the signals).
This link could be used to set the P/Z fine adjustment of the triples/core preamplifiers.

IMPORTANT NOTES:

1) All detector GND's carried to the receiver along the cable must be connected at the receiver end to the cable shields found on pins 1, 13, 14 and 26 of the MDR connector.
2) All digital signals transmitted from the receiver to the detector should enter the cable through a source series termination resistor of 75 Ohms. Instead, no termination resistor should be put at the detector side to avoid half splitting of the TTL signal (with the possible exception of signal "Pulser In", which could be received through a 75 Ohm resistor and a Schmitt-Trigger comparator).
3) All Logic Levels (see column "Format" in Complete Signal List) should be bypassed to ground with 1uF capacitors either at the transmitter or at the receiver sides.