AGATA – Digitiser – Segment – FADC, Laser, and spare software interfaces.

Front panel LEDS

0. Unlit : Top BREF clock DCM locked
1. Unlit : Shifter clock DCM locked
2. Unlit : Slow interface DCM locked.
3. Unlit : Counter bit 27 = '1'
4. Unlit : Counter bit 26 = '1'
5. Unlit : Counter bit 25 = '1'
6. Unlit : Reset true
7. Unlit : Module Control bit 3 = '1' ;

Control Register – 0

0. Laser Enable : set to enable laser
1. Laser Disable : set to disable laser
2. Laser Resetn : clear to reset Laser
3. Operates LED 7.
4. shdn_a : controls pre-amp signal
5. shdn_b : controls pre-amp signal
6. Set to 1 to select front panel sync
7. Enable Inhibit signals to be transmitted.
8. RAM test enable
9.
10.
11.
12. Set to 1 to reset the Sprom and re-read all the contents into RAM
13.
14. '1' = Enable counter to 4 digital laser spares :- lsp0 to counter(1) etc.
15.

Status Register - 1

0. Laser Faultn : If '0' then Laser is signalling fault.
1.
2.
3.
4. RAM test passed
5. RAM test failed
6. RAM test in progress
7.
8. TX1 Polarity setting
9. TX2 Polarity setting.
10. TX3 Polarity setting.
11. TX4 Polarity setting.
12. TX5 Polarity setting.
13. TX6 Polarity setting : default is true as this channel needs it.
14. Slow Interface DCM Lock signal state '1' = locked

15. Top BREF DCM Lock signal state ‘1’ = locked

DAC inspection line A - 2– 16 bits R/W

Bits 0 to 3 select the channel to output

DAC inspection line B - 3

Bits 0 to 3 select the channel to output

Inspection Line enables - 4

0. Enable buffer for DAC 1
1. Enable buffer for DAC 2
2. Enable buffer for analogue inspection.

Spare control Register – 5

Bits 0 to 2 select the destination and source of the spare channel. The firmware will select the correct analog and digital routing.

Channel Global Control – 7

0. Gain select for channel 1
1. Gain select for channel 2
2. Gain select for channel 3
3. Gain select for channel 4
4. Gain select for channel 5
5. Gain select for channel 6
6.
7.
8. Buffer enable Channel 1 – connects the ADC outputs to the FPGA
9. Buffer enable Channel 2 – connects the ADC outputs to the FPGA
10. Buffer enable Channel 3 – connects the ADC outputs to the FPGA
11. Buffer enable Channel 4 – connects the ADC outputs to the FPGA
12. Buffer enable Channel 5 – connects the ADC outputs to the FPGA
13. Buffer enable Channel 6 – connects the ADC outputs to the FPGA
14.
15.

Analog Inspection selection – 8

Bits 0 to 3 select the channel to output

Spare communications signal status – 9

0. Spare signal 0
1. Spare signal 1
2. Spare signal 2
3. Spare signal 3
4. Spare signal 4
5. Spare signal 5
6. SC_reset
7.

Logic Inspection line source select – 10

Bits 0:7 select source for output 0
Bits 8 : 15 select source for output 1

Source table

0	SYNC from the core board
1	SYNC_fp
2	Inhibit_A
3	Inhibit_B
4	Offset_optical_signal
5	LED counter bit 1 = 25Mhz

Firmware recognition code – 15

Bits 0 to 3 : Year
Bits 4 to 7 : Month
Bits 11 to 8 : C for core, 0 for segment
Bits 12 to 15 : E for experimental version.

ADC Channel 1 registers – 0x0000 0010

Status – 0

No bits allocated

Control – 1

Bits 0 to 1 Input phase adjust choice.

Rocket Status – 2

0. TXBUFFERR
1. TXKERR 0
2. TXKERR 1
3. TXRUNDISP 0
4. TXRUNDISP 1

Rocket Control – 3

0.
1.
2.
3.
4.
5.
6. Reset the Rocket I/O module
7.
8. Inhibit the Rocket I/O module
9. TXCHARISK 0
10. TXCHARISK 1
11. TXCHARDISPVAL 0
12. TXCHARDISPVAL 1
13. TXCHARDISPMODE 0
14. TXCHARDISPMODE 1
15. Power down the Rocket I/O module

Set to 0x7c00 for alignment, and then 0 to transmit data.

Test – Data Source Select – 4

0. Test enable when set to ‘1’
1. Source select bit 0 00 = Ramp, 01 PRNG, 10 & 11 0xDEAD
2. Source select bit 1

Test – Insert Error – 5

0. Insert 1 error when set to ‘1’

ADC Channel 2 registers – 0x0000 0020

The same structure as for channel 1

ADC Channel 3 registers – 0x0000 0030

The same structure as for channel 1

ADC Channel 4 registers – 0x0000 0040

The same structure as for channel 1

ADC Channel 5 registers – 0x0000 0050

The same structure as for channel 1

ADC Channel 6 registers – 0x0000 0060

The same structure as for channel 1

ADC Channel 7 registers – 0x0000 0070

The same structure as for channel 1

Offset DACs – 0x0000 0080

DAC control – 0

Bits 0 to 2 : select channel to be ramped
Bit 8 : '0' = normal operation. '1' = Ramp full 16 range 1 change per 2us. Full sweep approx 140ms.

Channel 1 Offset – 1

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV
Range is

Channel 2 Offset – 2

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Channel 3 Offset – 3

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Channel 4 Offset – 4

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Channel 5 Offset – 5

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Channel 6 Offset – 6

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Channel 7 Offset – 7

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Laser spare1 rocket I/O registers – 0x0000 0090

Status – 0

No bits allocated

Control – 1

No bits allocated

Rocket Status – 2

0. TXBUFFERR
1. TXKERR 0
2. TXKERR 1
3. TXRUNDISP 0
4. TXRUNDISP 1

Rocket Control – 3

0.
1.
2.
3.
4.
5.
6. Reset the Rocket I/O module
7.
8. Inhibit the Rocket I/O module
9. TXCHARISK 0
10. TXCHARISK 1
11. TXCHARDISPVAL 0
12. TXCHARDISPVAL 1
13. TXCHARDISPMODE 0
14. TXCHARDISPMODE 1
15. Power down the Rocket I/O module

Set to 0x7c00 for alignment, and then 0 to transmit data.

Test – Data Source Select – 4

0. Test enable when set to ‘1’
1. Source select bit 0 00 = 0xF00D, 01 0xC01D, 10 & 11 0xDEAD
2. Source select bit 1

Laser spare2 rocket I/O registers – 0x0000 00A0

The same structure as for Laser spare1

Serial prom – 0x0000 0800 to 0x0000 0FFF

The contents of the serial proms in the digitiser is specified in the document : "Digitiser Serial Prom definitions"

Copy of the prom – 0x0000 0800 to 0x0000 087F

Bits 0 to 7 : data from the prom having been read and copied into internal BRAM at power up.
Bits 8 to 15 : always 0x00.

Control register - 0x0000 0880

Bit 0 : 1 => reset "last failed" bit.
Bit 7 : 1 => serial prom is enabled for write.
0 => serial prom is write protected.

Status register – 0x0000 0881

Bit 0 : 1 => interface is busy .
Bit 1 : 1 => a write has been requested .
Bit 2 : 1 => All the data has been read into the RAM.
Bit 3 : 1 => last sprom interface request failed. This can be due simply to the interface being busy when a request was made. During a write sequence internal to the prom it will not respond to any requests.

Snapshot – 0x0001 0000 to 0x0001 7FFF.

Offset 0 : Control register
Bit 0 : Start snapshot when set to '1'. To repeat write '0' then '1'
Bit 1 : Trigger select. '0' = SYNC pulse. '1' = Sync_fp input.
Offset 0x1000 to 0x1FFF : ADC value captured for channel 1.
Offset 0x2000 to 0x2FFF : ADC value captured for channel 2.
Offset 0x3000 to 0x3FFF : ADC value captured for channel 3.
Offset 0x4000 to 0x4FFF : ADC value captured for channel 4.
Offset 0x5000 to 0x5FFF : ADC value captured for channel 5.
Offset 0x6000 to 0x6FFF : ADC value captured for channel 6.
Offset 0x7000 to 0x7FFF : ADC value captured for channel 7.
Warning : It takes about 3.5 minutes to read back *all* the data for one channel.

SRAM – 0x0001 8000 to 0xFFFF FFFF.

Address is mapped directly to the SRAM address bus.
SRAM data is 16 bits wide.
SRAM address is 19 bits .
So to read location 0 in the RAM access address 0x0008 0000.