Core controls - LEDs and status

Front panel LEDS

0. Unlit : Top BREF clock DCM locked
1. Unlit : Laser input clock DCM locked
2. Unlit : Slow interface DCM locked. Runs from the onboard crystal.
3. Unlit : Shifter clock DCM locked
4. Lit : Sync signal is detected and in the right place in time.
5. Unlit : Counter bit 25 = '1'
6. Unlit : Reset true
7. Unlit : Module Control bit 3 = '1' ;

Global control and status registers – 0x0000 0000

Control Register – 0

0. Laser Enable : set to enable laser
1. Laser Disable : set to disable laser
2. Laser Resetn : clear to reset Laser
3. Operates LED 7.
4. shdn_c : controls pre-amp signal
5. Laser RX enable : set to enable the receiver part of the Laser
6. Laser SQ enable : set to enable the ?????? part of the laser .
7.
8. Reset other DCMs to allow lock after connect the optical link
9. Set to 1 to enable the inhibit signal to be transmitted.
10.
11. Set to 1 to reset the Trigger Block logic.
12. Set to 1 to reset the Sprom and re-read all the contents into RAM
13. Set to 1 to enable the RAM test.
14.
15.

Status Register - 1

0. Laser Faultn : If '0' then Laser is signaling fault.
1. Laser Signal Detect :
2. Sync OK
3.
4. RAM test passed
5. RAM test failed
6. RAM test in progress
7.
8. TX1 Polarity setting
9. TX2 Polarity setting.
10. Control Clock select from Spartan
11.
12. Shifter clock DCM Lock signal state '1' = locked
13. Laser clock DCM Lock signal state '1' = locked

14. Slow Interface DCM Lock signal state '1' = locked
15. Top BREF DCM Lock signal state '1' = locked

DAC inspection line A - 2

Bits 0 to 3 select the signal to output
- 1 : ADC of channel 1.
- 2 : ADC of channel 2.
- 8 : A_w_out signal from the Trigger block.
- 9 : cfd_signal from the Trigger block

DAC inspection line B - 3

Bits 0 to 3 select the channel to output.
- 1 : ADC of channel 1.
- 2 : ADC of channel 2.
- 8 : A_w_out signal from the Trigger block.
- 9 : cfd_signal from the Trigger block

Inspection Line enables - 4

0. Enable buffer for DAC 1
1. Enable buffer for DAC 2
2. Enable buffer for analogue inspection.

Channel Global Control – 7

0. Gain select for channel 1 – used as a spare output
1. Gain select for channel 2 – used as a spare output
2.
3.
4.
5.
6.
7.
8. Buffer enable Channel 1 – connects the ADC outputs to the FPGA
9. Buffer enable Channel 2 – connects the ADC outputs to the FPGA

Analog Inspection selection – 8

0. Set to select channel 1
1. Set to select channel 2

Outputs are to be mutually exclusive.

Spare communications signal status – 9

0. Spare signal 0
1. Spare signal 1
2. Spare signal 2
3. Spare signal 3
4. Spare signal 4
5. Spare signal 5
6. SC_reset

RX Rocket I/O General Status – 10

0. rxok input 0
1. rxok input 1
2. comfort – input 0
3. comfort – input 1
4. aligned - input 0
5. aligned – input 1

SYNC control – 11

0. Phase select bit 0 – set to select a 5ns shift in the sync pulse out to the digitiser
1. Phase select bit 1

SYNC status – 12

0. '1' = Sync OK

Clock Control – 13

0.	Global Clock Delay Bit(0)	10ps
1.	Global Clock Delay Bit(7)	1,150ps
2.	Global Clock Delay Bit(6)	575ps
3.	Global Clock Delay Bit(5)	290ps
4.	not an effective bit	
5.	Global Clock Delay Bit(3)	70ps
6.	Global Clock Delay Bit(2)	35ps
7.	Global Clock Delay Bit(1)	15ps
8.	Global Clock Delay Bit(8)	2,300ps
9.	Global Clock Delay Bit(9)	4,610ps
10.	Global Clock Delay Bit(10)	Cascade – no effect
11.		
12.		
13.		
14.		

Pre-amp Pulser control – 14

0. AT10_D(0)
1. AT10_D(1)
2. AT10_D(2)
3. AT10_D(3)
4.
5.
6.
7. Mode
8. PS_EN
9.
10.
11. Enable the internal pulser
12. Internal pulser rate bit 0.
13. Internal pulser rate bit 1.
14. Internal pulser rate bit 2.

15.

Pulser rate map :-
0 => 100Hz, 1 => 200Hz,
2 => 400Hz, 3 => 800Hz,
4 => 1600Hz, 5 => 3200Hz ,
6 => 6400Hz, 7 => SYNC pulse.

Pre-amp Pulser DAC fine Gain setting – 15

Bits 0 to 15.

ADC Channel 1 registers – 0x0000 0010

Status – 0

No bits allocated

Control – 1

Bits 0 to 1: Input phase adjust choice.

Rocket Status – 2

0. TXBUFFERR
1. TXKERR 0
2. TXKERR 1
3. TXRUNDISP 0
4. TXRUNDISP 1
5.
6.
7.
8. RX Ok. Set if the received data is aligned.
9. No RX loss of sync. Set if Data is in sync.
10. Set if SYNC pulse is OK from digitizer internal distribution to this channel.
11. Set if SYNC pulse is OK from Rocket I/O received data.

Rocket Control – 3

0. Rocket I/O Loopback mode bit 0 : Selects Internal Parallel loopback
1. Rocket I/O Loopback mode bit 1 : Selects Serial Loopback
2.
3.
4. Start receive test
5. Receiver error reset??
6. Reset the Rocket I/O module
7. Reset the RX part.
8. Inhibit the Rocket I/O module
9. TXCHARISK 0
10. TXCHARISK 1
11. TXCHARDISPVAL 0
12. TXCHARDISPVAL 1
13. TXCHARDISPMODE 0
14. TXCHARDISPMODE 1
15. Power down the Rocket I/O module

Set to 0x7c00 for alignment, and then 0 to transmit data.

Test – Data Source Select – 4

0. Test enable when set to ‘1’
1. Source select bit 0

2. Source select bit 1 : "00" = Ramp, "01"= PRNG, "10"= 14bit ramp, "11" = 0x00## where ## are bits 15 to 8 of this register.

Bits 15 to 8 are the "id" used in test mode "11".

Test – Insert Error – 5

0. Insert 1 error when set to '1'. Sends 0xF00D

RX status – 6

0. rxcommadet
1. rxrealign
2. rxnotintable 0
3. rxnotintable 1
4. rxlossofsync 0
5. rxlossofsync 1
6. rxdisperr 0
7. rxdisperr 1
8. rxcharisk 0
9. rxcharisk 1
10. rxchariscomma 0
11. rxchariscomma 1
12. rxbuffstatus 0
13. rxbuffstatus 1
14. rxrundisp 0
15. rxrundisp 1

RX current data – 7

Bits 15 to 0: Data word received from the Rocket I/O port.

RX error count – 8

Bits 15 to 0 : report the errors when a test ramp is being transmitted and loop back is enabled.

Expected SYNC delay LSW – 9

Bits 15 to 0: Bits 15 to 0 of the sync limit check word. Default is 0xFFFF

Expected SYNC delay MSW – 10

Bits 15 to 0: Bits 31 to 16 of the sync limit check word. Default is 0

SYNC error – 11

Bits 15 to 0: The count of the number of times the SYNC pulse to SYNC pulse delay is not equal to the expected. Only counts if SYNC pulses are present.

Last SYNC to SYNC difference LSW – 12

Bits 15 to 0: Bits 15 to 0 of the sync difference counter. Counts the number of clocks between successive SYNC pulses.

Last SYNC to SYNC difference MSW – 13

Bits 15 to 0: Bits 31 to 16 of the sync difference counter. Counts the number of clocks between successive SYNC pulses.

SYNC width – 14

Bits 7 to 0: Count of the number of clocks the SYNC pulse is true.

RX – SYNC error - 15

Bits 15 to 0: The count of the number of times the SYNC pulse to Rocket I/O received SYNC pulse delay is not equal to the expected. Only counts if SYNC pulses are present.

ADC Channel 2 registers – 0x0000 0020

The same structure as for channel 1

RX – Rocket I/O receiver channel 1 – 0x0000 0030

Status – 0

16. rxcommadet
17. rxrealign
18. rxnotintable 0
19. rxnotintable 1
20. rxlossofsync 0
21. rxlossofsync 1
22. rxdisperr 0
23. rxdisperr 1
24. rxcharisk 0
25. rxcharisk 1
26. rxchariscomma 0
27. rxchariscomma 1
28. rxbuffstatus 0
29. rxbuffstatus 1
30. rxrundisp 0
31. rxrundisp 1

Current Received data value – 1

Bits 0 to 15 : Current value from the receive channel

Control – 2

0. Start receive ……

Error counter – 3

Bits 0 to 15 are the current value of the test error counter.

RX – Rocket I/O receiver channel 2 – 0x0000 0040

Same registers as for channel 1

TOT TX/RX channel 1 Registers – 0x0000 0050 to 0x0000 0056

Status – Offset 0x0

Read Only

0. TOT Rx Busy

Control Mode – Offset 0x1

Read/Write

0: Enable TOT Tx
1: Enable TOT Rx (where loopback implemented for channel)
2: TOT Tx test mode

Control Pulse – Offset 0x2

Always zero on read

0: *test_valid* (initiates transmission of test data from TOT Tx).
4: Reset TOT Tx (and Rx if implemented for this channel).

Test Data LSB – Offset 0x3

Read/Write

0–15: Lower 2 bytes of test data to transmit from TOT Tx.

Test Data MSB – Offset 0x4

Read/Write

0–15: Upper 2 bytes of test data to transmit from TOT Tx.

Data Rx LSB – Offset 0x5

Only implemented for channel with loopback logic
Read Only

0–15: Lower 2 bytes of most recent data received at TOT Rx.

Data Rx LSB – Offset 0x6

Only implemented for channel with loopback logic
Read Only

0–15: upper 2 bytes of most recent data received at TOT Rx.

TOT TX/RX channel 2 – 0x0000 0060 to 0x0000 0066

Details as per TOT TX/RX channel 1.

Offset DACs – 0x0000 0080

DAC control – 0

Bits 0 to 2 : select channel to be ramped
Bit 8 : '0' = normal operation. '1' = Ramp full 16 range 1 change per 2us. Full sweep approx 140ms.

Channel 1 Offset – 1

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Channel 1 Offset – 2

Bits 0 to 15 : DAC setting changes when written. LSB is ???mV

Trigger Block – 0x0000 0090 – for detailed explanation of operation refer to separate documentation

Trigger Enable – 0

Bits 0: <= '1' to enable, <= '0' to disable

Differentiation Constant – 1

Bits 0 to 4 : Differentiation constant value.

Integration Constant – 2

Bits 0 to 4 : Integration constant value.

Trigger type – 3

Bits 0 to 1 : 0 =>

Threshold – 4

Bits 0 to 13 : signed threshold , + 8192 to – 8192.

Force Trigger– 5

Bits 0: <= '1' to enable, <= '0' to disable

Slope – 6

Bits 0: <= '1' to negative, <= '0' to positive

CFD Trigger Delay – 7

Bits 0 to 2.

CFD Trigger Gain – 8

Bits 0 to 1: "00" => ½ , "01" => ¼ , "10" => 1/8 , "11" => 1/16

CFD Trigger Shift – 9

Bits 0 to 3.

Rectify – 10

Bits 0 to 15.

Trigger Block Identifier – 12

Bits 0 to 15 : Read only => 0xD12C (“Disc” sort of ☺)

Software Record – 0x0000 00A0

Module Record

Bits 0 to 15 : All bits read/write.

SYNC period control – 0x0000 00B0

These two words are used by the sync recognition firmware to determine the expected
delay between two successive sync pulses. Default (on power-up) is 0x0000FFFF.

SYNC period LSW – offset 0

Bits 0 to 15: All bits read/write.

SYNC period MSW – offset 1

Bits 0 to 15: All bits read/write.

SYNC missed counter – offset 2

Counts every time there is no SYNC pulse when expected.
Bits 0 to 15: All bits read only.

Average ADC values – 0x0000 0100

Runs a 16 value average collection of data for all the ADCs when started by writing to this location. Process takes about 3 uS to complete.

ADC1 average – offset 96

ADC2 average – offset 97

Rocket I/O channel 0 rx_current average – offset 98

Rocket I/O channel 1 rx_current average – offset 98

Logic Inspection control – 0x0000 0110

Selection register Record

Bits 0 to 7 : select signal for Logic Inspection Line 0
Bits 8 to 15 : select signal for Logic Inspection Line 1

Selection on both lines is as follows :

0 : Sync pulse
1 : Sync from the front panel
2 : inh_ch1 from the pre-amp
3 : inh_ch2 from the pre-amp
4 : Pulse from the internal generator that is sent to the pre-amp to generate a detector pulse.

Serial prom – 0x0000 0800 to 0x0000 0FFF

The contents of the serial proms in the digitiser is specified in the document : "Digitiser Serial Prom definitions"

Copy of the prom – 0x0000 0800 to 0x0000 087F

Bits 0 to 7 : data from the prom having been read and copied into internal BRAM at power up.
Bits 8 to 15 : always 0x00.

Control register - 0x0000 0880

Bit 0 : 1 => reset "last failed" bit.
Bit 7 : 1 => serial prom is enabled for write.
0 => serial prom is write protected.

Status register – 0x0000 0881

Bit 0 : 1 => interface is busy .
Bit 1 : 1 => a write has been requested .
Bit 2 : 1 => All the data has been read into the RAM.
Bit 3 : 1 => last sprom interface request failed. This can be due simply to the interface being busy when a request was made. During a write sequence internal to the prom it will not respond to any requests.

SRAM – 0x0000 1000 to 0xFFFF FFFF.

Address is mapped directly to the SRAM address bus.
SRAM data is 16 bits wide.
SRAM address is 19 bits .