Pattern Generator Software interface for the random pulser version.

The 16 channel pulse generator can create analog positive or negative tail pulses for use when testing data acquisition systems. Each channel has a pulse generator and a pseudo random sequence (PRS) state machine. The pulse from the channel is either at a regular rate or controlled by the PRS. The pulse height can be controlled by the PRS as well giving 16 steps or fixed by setting a register.

The PRS uses a linear feedback shift register (LFSR) to define the delay between pulses.

Control of the module is via the VME A16/D16 address space.

Offsets : 0 => 15 control the pulse generators' signal height when the sequencer is not running.

0. Height bit 0
1. Height bit 1
2. Height bit 2
3. Height bit 3

Offsets : 16 => 31 are used to load the LFSR seed value for random pulse generation.

Bits 0 => 14 are written to bits 0=>14 of the 25 bit LFSR. Each different value programmed here will cause the LFSR to start from a different point in the 2^{25} long sequence.

Bits 0 => 8 are written into the 9 bit LFSR used for the pulse height generator.

Offset : 32 each bit triggers a channel to output a single pulse when changed from false to true unless the PRS system is running.

Offset : 33 each bit controls the output pulse polarity of a channel. True gives a positive pulse and false gives a negative pulse.

Offset : 34 Board control register.

0. Sequencer select. Set to true to use the all PSRs to generate the timing and pulse height.
1. Sequencer start. Set to true to select all the PSRs for control of the pulse outputs.
2. Sequencer step. Not used in this design.
3. Sequencer reset. Set to true to reset all the PSRs.
4. Rate bit 0 : '0' = bit selected
5. Rate bit 1: '0' = bit selected
6. Rate bit 2: '0' = bit selected
7. Rate bit 3: '0' = bit selected
8. Rate bit 4: '0' = bit selected
9. Rate bit 5: '0' = bit selected
10. Rate bit 6: '0' = bit selected
11. Rate bit 7: '0' = bit selected

The 8 bit rate word is used to select how many of the outputs of the LFSR are used to determine the delay between pulses. Rate bit 0 selects LFSR bit 4 …. Etc. The lower four bits of the LFSR are always used. So the maximum delay varies between 1.15uS and 205.15uS.