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* Clock and Event Counter Module *
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VERSION Ø.2
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☛ Standard: VXI-C : same module for both ends Transmit (Tx) / Receive(Rx).

☛ Absolute Clock : 1 loadable time counter and 8 time registers (1by channel)
48 bits @100 MHz
TCXO stability : 1ppm
1 comparator register (48 bits) for VME interrupt (IRQ1..7).

Each tagging (time counter -> time register$_n$) will be local (NIM input-LEMO ØØ) or remote (one twisted pair in each serial link cable). These inputs will receive signals with good timing (FT for example) and will be equipped with programmable delay lines to compensate for wire and electronic delays (9bits / 1ns step => 500ns).

3 time counter start sources: soft (register control bit), VXI TTLTRG stop/go* line or front panel NIM input.

☛ Event counter: 32 bits clocked by a TTLTRG backplane signal (VAL3 for example) or via front panel NIM input (LEMO 00 connector)

This counter will be incremented with the back edge of this signal and a comparison will be made on the front edge to check the synchronisation with EXOGAM event number (4 lsb's available on the VXI P2 connector).

☛ Serial links: 6 Tx channels controlled directly by the link ports of the DSP (ADSP-21062 / Analog Devices)

2 Tx channels controlled by the DSP and programmable logic.

The first channels (0..5) will be used for high speed (f_{dsp}) short distance (20-30 m) transfer and the last channels (6..7) will have programmable transfer frequency to provide valid data for link up to 100 meters.

The first channel will have a double function to be also a receiver: TxØ/Rx.

☛ VME Readout modes:
All the information will be readable with VME
- single cycle
- DT32 block transfer.

☛ More technical information:

The PCB connectors used will be stacked 2x15 points MDSM connectors from ITT-Cannon (MDSM-30PE-Z10-VR22). They have good EMI shielding and are especially designed to save space on VME/VXI front panel. The cable used (shielded twisted pair) and the cable connectors are also supplied by ITT-Cannon.

Each Tx serial link carrying differential ECL signals has 7 twisted pairs used as follow:

- LCLK (out)
- LDATA<3..0> (out)
- RTAGn (in)
- LACK/OPT (in)

(When channel Ø is configured as receiver (Rx), naturally the same signals are in opposite way)

The information transmitted on channel n will be 96 bits:

- 1 x 48 bits data word (channel n clock value)
- 1 x 48 bits data word (32 bits event number + 16 bits control word)

The 16 bits control word could be a checksum.

As each link port is double-buffered (96 bits max), the acknowledge signal (LACK) is optional and could be used, for example, as a RETRY signal if there is an error in the received data stream.

Data readout.

Data will only be included in event by event readout when there is an event in the system where the clock module is located. However, data can be generated every time the event number is incremented and then stored locally in a buffer until they can be transmitted in the next event which is read in the clock module's local system. The selection of this "read always" mode is controlled by software. The alternative is "read only when hit" mode which relies on receiving a Tag input before putting data in the buffer. ("Read" in the names of these 2 modes of operation refers to reading and storing the event number when it is clocked (and the clock value), not backplane readout.)

The "read always" mode makes data merging in the event builder considerably simpler because all input data streams have a complete sequence of event numbers with no gaps. Any missing events are clearly errors. "Read only when hit" mode produces less data but requires a more complex search through input data buffers due to the gaps in the event number sequence. It is inherently less secure in that there is no way to distinguish between an event missing because of an error and an event that never existed for physics reasons.

The last NIM output signals "TEST1" and "TEST2" (LEMOØØ) will be used to examine the exact timing of the tagging inputs, to view other internal signals on a scope or to trigger other module's inputs.

A 16 points auxiliary output connector (ECL diff.) using the same signals as serial links could be used with standard ribbon cable to interface one other module (VME board with SHARC PMC ...).